100331

100331 Low Power Triple D Flip-Flop

TEXAS
INSTRUMENTS

Literature Number: SNOS116

N *National Semiconductor*

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100331
Low Power Triple D Flip-Flop

General Description

The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9153601

Logic Symbol

DS100300-1
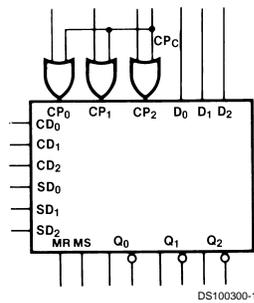
Pin Names	Description
CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0-Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP

DS100300-2

24-Pin Quad Cerpak

DS100300-3

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Logic Diagram

SD$_0$ D$_0$ CP$_0$ CD$_0$ SD$_1$ D$_1$ CP$_1$ CD$_1$ SD$_2$ D$_2$ CP$_2$CP$_C$ CD$_2$

D CP   D CP   D CP

S$_D$ C$_D$ S$_D$ C$_D$ S$_D$ C$_D$

MS

MR

Q$_0$ $\overline{Q}_0$ Q$_1$ $\overline{Q}_1$ Q$_2$ $\overline{Q}_2$
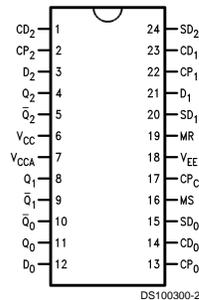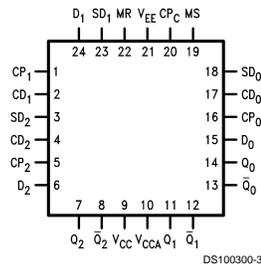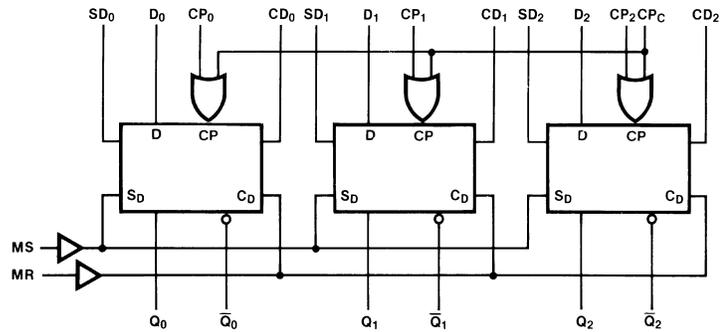
DS100300-5

Truth Tables

Synchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D$_n$	CP$_n$	CP$_C$	MS SD$_n$	MR CD$_n$	Q$_n$(t + 1)
L	⟋	L	L	L	L
H	⟋	L	L	L	H
L	L	⟋	L	L	L
H	L	⟋	L	L	H
X	L	L	L	L	Qn(t)
X	H	X	L	L	Qn(t)
X	X	H	L	L	Qn(t)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
⟋ = LOW to HIGH Transition

Asynchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D$_n$	CP$_n$	CP$_C$	MS SD$_n$	MR CD$_n$	Q$_n$(t + 1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T$_{STG}$)	–65˚C to +150˚C
Maximum Junction Temperature (T$_J$)	
Ceramic	+175˚C
Pin Potential to	
Ground Pin (V$_{EE}$)	–7.0V to +0.5V
Input Voltage (DC)	V$_{EE}$ to +0.5V
Output Current	
(DC Output HIGH)	–50 mA
ESD (Note 2)	≤ 2000V

Recommended Operating Conditions

Case Temperature (T$_C$)	
Military	–55˚C to +125˚C
Supply Voltage (V$_{EE}$)	–5.7V to –4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version
DC Electrical Characteristics

V$_{EE}$ = –4.2V to –5.7V, V$_{CC}$ = V$_{CCA}$ = GND, T$_C$ = –55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T$_C$	Conditions		Notes
V$_{OH}$	Output HIGH Voltage	–1025	–870	mV	0˚C to +125˚C	V$_{IN}$ = V$_{IH}$ (Max) or V$_{IL}$ (Min)	Loading with 50Ω to –2.0V	(Notes 3, 4, 5)
		–1085	–870	mV	–55˚C			
V$_{OL}$	Output LOW Voltage	–1830	–1620	mV	0˚C to +125˚C			
		–1830	–1555	mV	–55˚C			
V$_{OHC}$	Output HIGH Voltage	–1035		mV	0˚C to +125˚C	V$_{IN}$ = V$_{IH}$ (Min) or V$_{IL}$ (Max)	Loading with 50Ω to –2.0V	(Notes 3, 4, 5)
		–1085		mV	–55˚C			
V$_{OLC}$	Output LOW Voltage		–1610	mV	0˚C to +125˚C			
			–1555	mV	–55˚C			
V$_{IH}$	Input HIGH Voltage	–1165	–870	mV	–55˚C to +125˚C	Guaranteed HIGH Signal for all Inputs		(Notes 3, 4, 5, 6)
V$_{IL}$	Input LOW Voltage	–1830	–1475	mV	–55˚C to +125˚C	Guaranteed LOW Signal for all Inputs		(Notes 3, 4, 5, 6)
I$_{IL}$	Input LOW Current	0.50		µA	–55˚C to +125˚C	V$_{EE}$ = –4.2V V$_{IN}$ = V$_{IL}$ (Min)		(Notes 3, 4, 5)
I$_{IH}$	Input HIGH Current		240	µA	0˚C to +125˚C	V$_{EE}$ = –5.7V V$_{IN}$ = V$_{IH}$ (Max)		(Notes 3, 4, 5)
			340	µA	–55˚C			
I$_{EE}$	Power Supply Current	–130	–50	mA	–55˚C to +125˚C	Inputs Open		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at –55˚C, +25˚C, and +125˚C, Subgroups, 1, 2, 3, 7 and 8.

Note 5: Sampled tested (Method 5005, Table I) on each manufactured lot at –55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7 and 8.

Note 6: Guaranteed by applying specified input condition and testing V$_{OH}$/V$_{OL}$.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions		Notes
		Min	Max	Min	Max	Min	Max				
f_{max}	Toggle Frequency	400		400		400		MHz	Figures 2, 3		(Note 10)
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	Figures 1, 3		
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns			
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	CP_n, CP_C = L	Figures 1, 4	(Notes 7, 8, 9)
t_{PLH} t_{PHL}		0.50	2.40	0.60	2.10	0.50	2.50		CP_n, CP_C = H		
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	0.70	2.70	0.80	2.60	0.80	2.90	ns	CP_n, CP_C = L		
t_{PLH} t_{PHL}		0.70	2.90	0.80	2.80	0.80	3.10		CP_n, CP_C = H		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20	1.40	ns	Figures 1, 3, 4		
t_s	Setup Time D_n	1.00		0.80		0.90			Figure 5		(Note 10)
	CD_n, SD_n (Release Time)	1.50		1.30		1.60		ns	Figure 4		
	MS, MR (Release Time)	2.50		2.30		2.50					
t_h	Hold Time D_n	1.50		1.30		1.60		ns	Figure 5		
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	Figures 3, 4		

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25°C. Temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 and A11.

Note 10: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuits
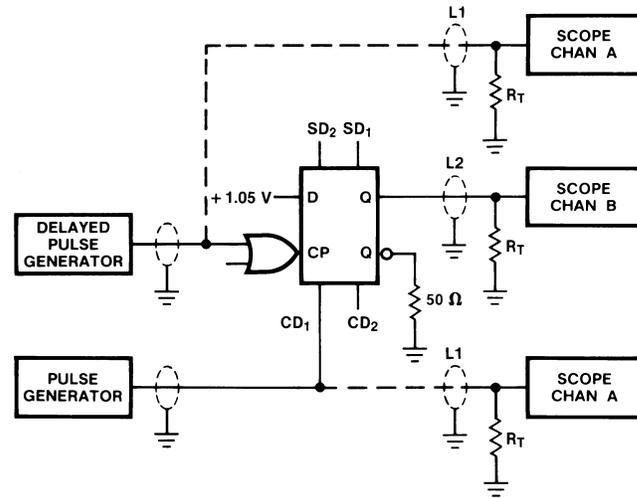
FIGURE 1. AC Test Circuit
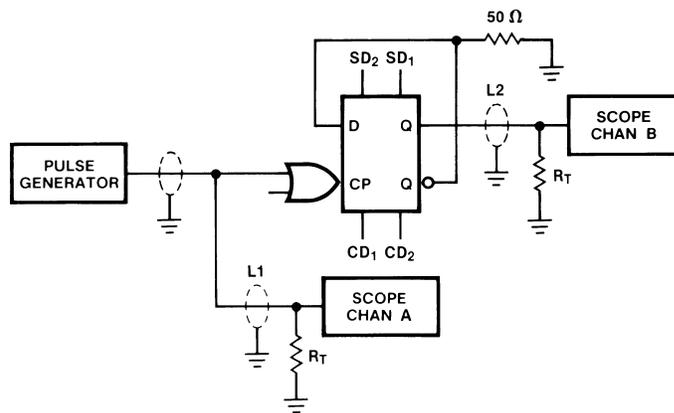
Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = Equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms
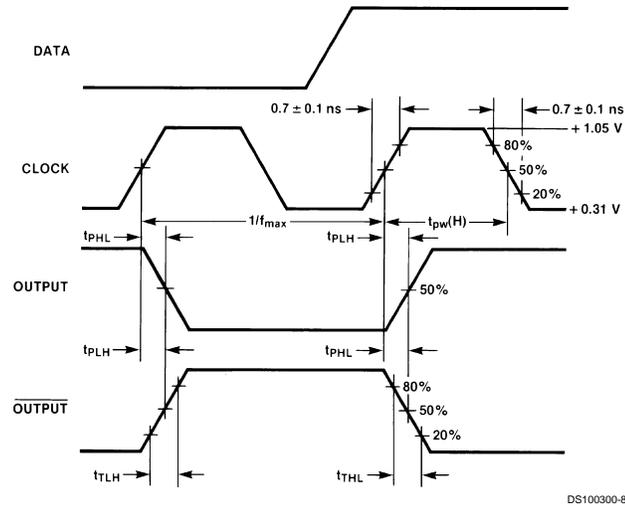
FIGURE 3. Propagation Delay (Clock) and Transition Times

DS100300-8
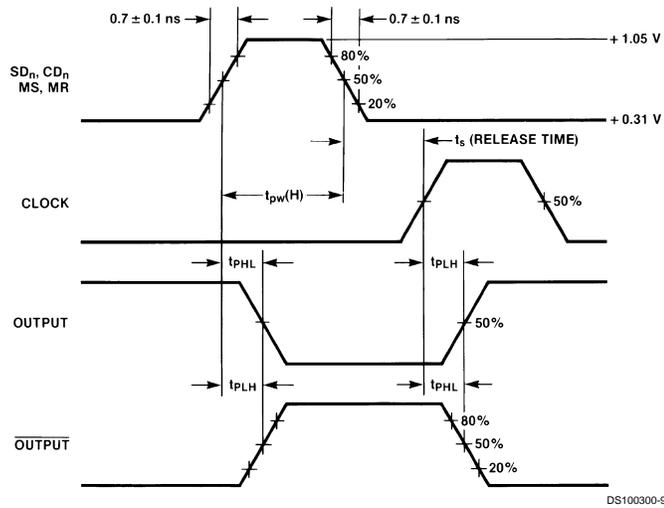
FIGURE 4. Propagation Delay (Resets)

DS100300-9
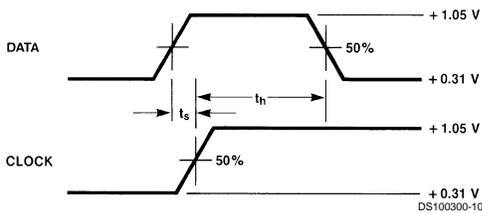
FIGURE 5. Data Setup and Hold Time

DS100300-10

Note 11: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 12: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

Physical Dimensions inches (millimeters) unless otherwise noted

1.215
(30.86)
MAX

0.025
(0.64)
RAD

0.030 — 0.055
(0.76 — 1.40)
RAD TYP

0.390
(9.91)
MAX

0.005
(0.13)
MIN TYP

GLASS
SEALANT

0.050 — 0.060
(1.27 — 1.52) TYP

0.032 — 0.042
(0.81 — 1.07) TYP

0.015 — 0.055
(0.38 — 1.40) TYP

0.400 — 0.430
(10.16 — 10.92)

0.180
(4.57)
MAX

0.225
(5.72)
MAX TYP

86° — 94°
TYP

90° — 100°
TYP

0.008 — 0.012
(0.20 — 0.30)
TYP

0.055
(1.40)
MAX TYP
BOTH ENDS

0.090 — 0.110
(2.29 — 2.79)
TYP

0.015 — 0.021
(0.38 — 0.53)
TYP

0.125
(3.18)
MIN
TYP

0.435 — 0.535
(11.05 — 13.59)

J24E (REV J)
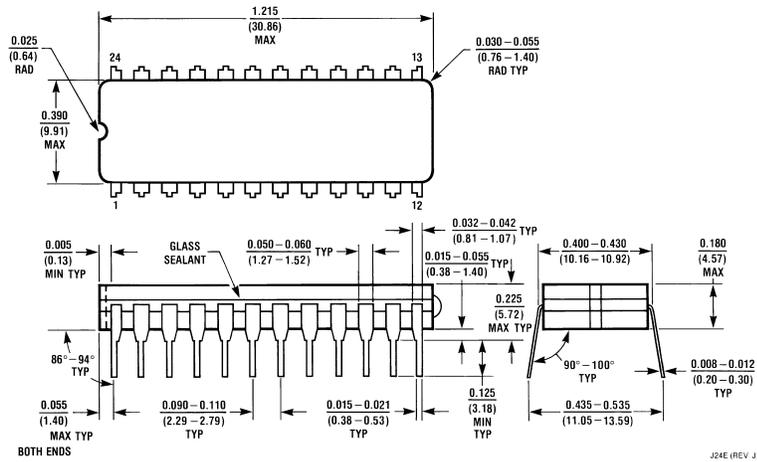
24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E

0.360
0.250 TYP

0.370 MIN
TYP
(MOLDED BODY)

0.360
0.250 TYP

0.007 TYP
0.004

PIN NO. 1
IDENT

0.018
0.016 TYP

0.075 MAX
8 PLCS

0.050
0.035

0.050 ± 0.005
TYP

0.085 MAX

0.400 MAX
TYP
GLASS

W24B (REV D)
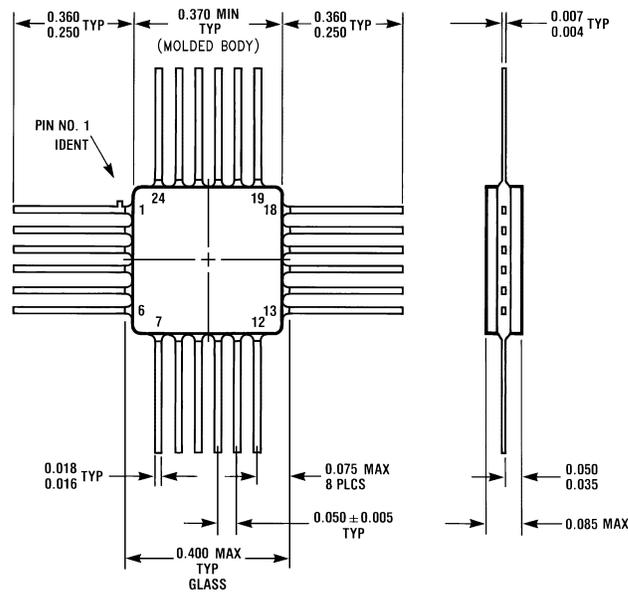
24-Lead Quad Cerpak (F)
NS Package Number W24B

100331 Low Power Triple D Flip-Flop

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