100353

100353 Low Power 8-Bit Register

Literature Number: SNOS131

National Semiconductor

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100353
Low Power 8-Bit Register

General Description

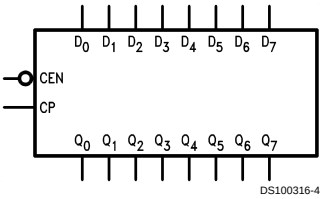
The 100353 contains eight D-type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), and a common clock enable pin ($\overline{CEN}$). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the $\overline{CEN}$ input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

The 100353 output drivers are designed to drive 50Ω termination to −2.0V. All inputs have 50 kΩ pull-down resistors.

Features

- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883

Logic Symbol

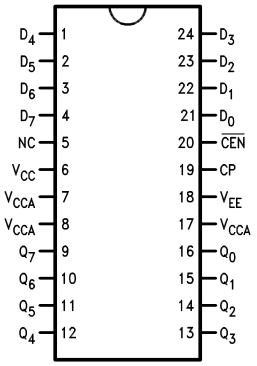


DS100316-4

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
Q_0–Q_7	Data Outputs
NC	No Connect

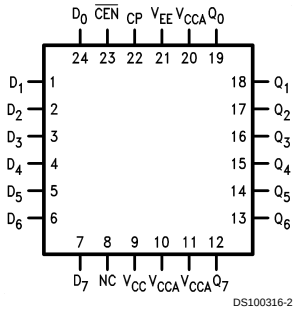
Connection Diagrams

24-Pin DIP



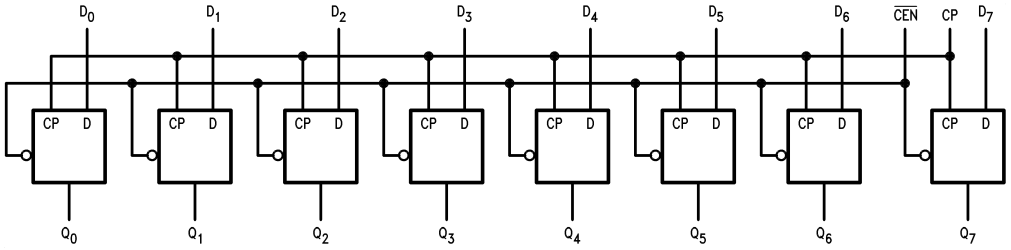
DS100316-1

24-Pin Quad Cerpak



DS100316-2

Logic Diagram



DS100316-5

Truth Table

Inputs			Outputs
D_n	$\overline{CEN}$	CP	Q_n
L	L	⌐	L
H	L	⌐	H
X	X	L	NC
X	X	H	NC
X	H	X	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change
⌐ = LOW to HIGH Transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impared

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to + 0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C			
		−1085	−870	mV	−55˚C	V_{IN} = V_{IH} (Max)	Loading with	(Notes 3, 4, 5)
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C	or V_{IL} (Min)	50Ω to −2.0V	
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C			
		−1085		mV	−55˚C	V_{IN} = V_{IH} (Min)	Loading with	(Notes 3, 4, 5)
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C	or V_{IL} (Max)	50Ω to −2.0V	
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for all Inputs		(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for all Inputs		(Notes 3, 4, 5, 6)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 3, 4, 5)
I_{IH}	Input HIGH Current		240	µA	0˚C to +125˚C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		(Notes 3, 4, 5)
			340	µA	−55˚C			
I_{EE}	Power Supply Current				−55˚C to	Inputs Open		
		−132	−42	mA	+125˚C	V_{EE} = −4.2V to −5.7V		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 1, 2*	(Note 10)

AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.70	3.30	0.80	3.10	0.80	3.50	ns		(Notes 7, 8,
t_{PHL}	CP to Output								*Figures 1, 2*	9, 11)
t_{TLH}	Transition Time	0.40	2.20	0.40	2.20	0.40	2.20	ns		(Note 10)
t_{THL}	20% to 80%, 80% to 20%									
t_s	Setup Time									
	D_n	0.30		0.30		0.30				
	$\overline{CEN}$ (Disable Time)	0.60		0.60		0.60		ns	*Figures 1, 3*	(Note 10)
	$\overline{CEN}$ (Release Time)	1.40		1.40		1.40				
t_h	Hold Time D_n	1.50		1.50		1.50		ns	*Figures 1, 4*	(Note 10)
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 2*	(Note 10)

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

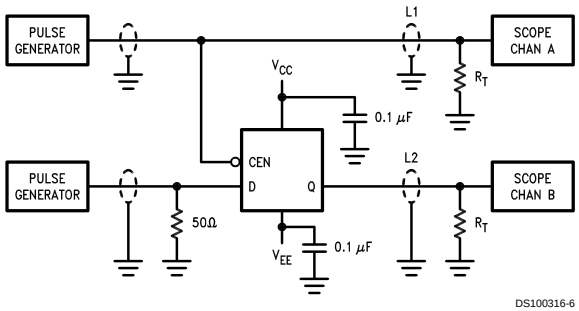
Note 8: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C, temperatures, Subgroups A10 and A11.

Note 10: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 11: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance linesR_T = 50Ω terminator internal to scopeDecoupling 0.1 μF from GND to V_{CC} and V_{EE} All unused outputs are loaded with 50Ω to GNDC_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC, Toggle Frequency Test Circuit

Switching Waveforms

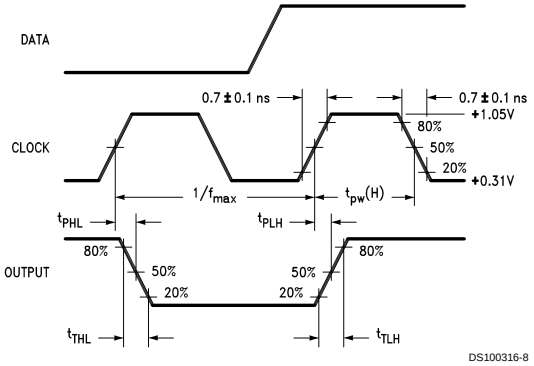


FIGURE 2. Propagation Delay (Clock) and Transition Times

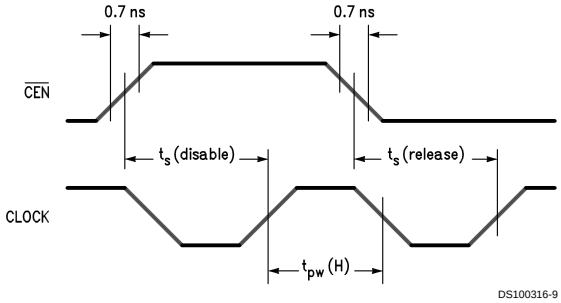
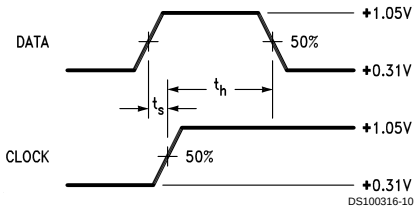


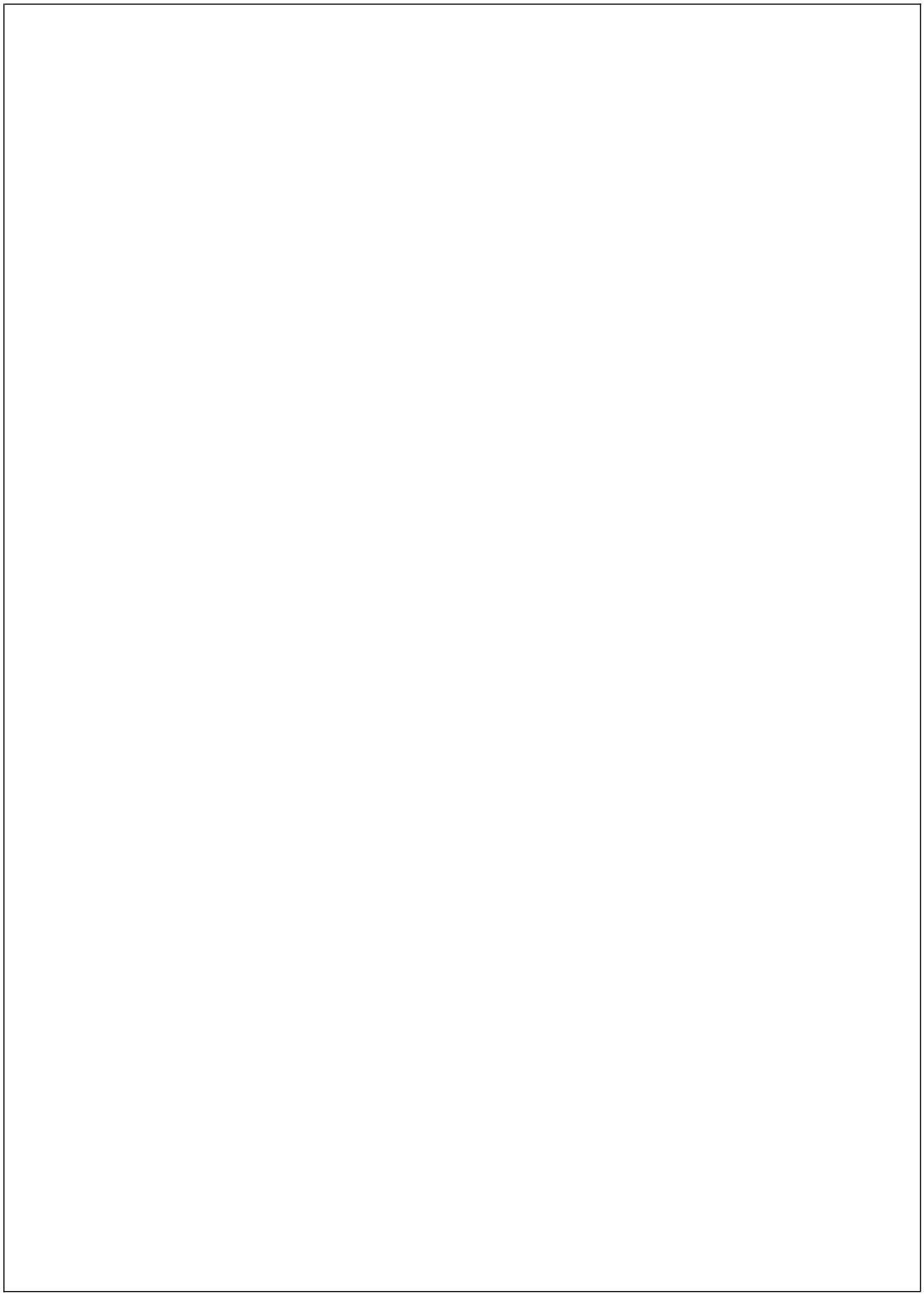
FIGURE 3. Setup and Pulse Width Times



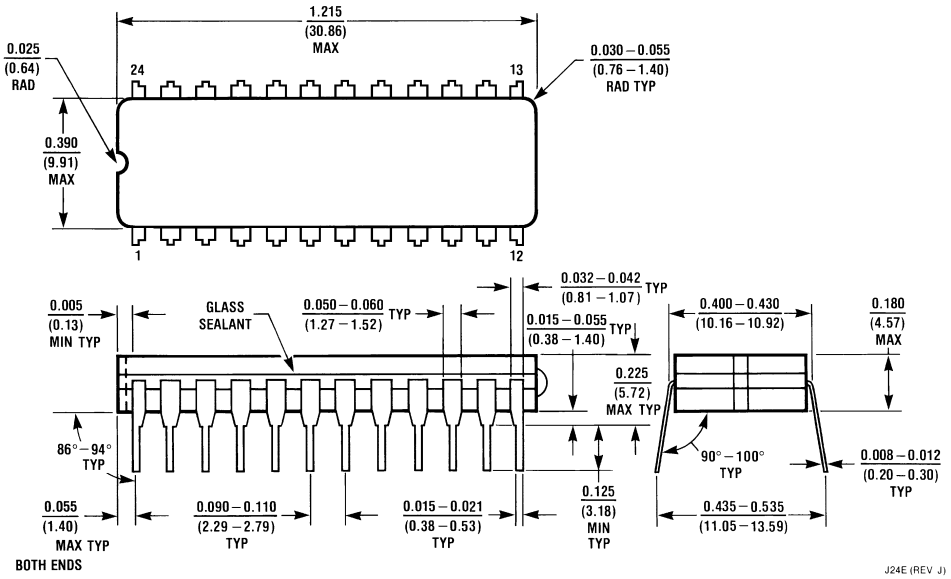
Note 12: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 13: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

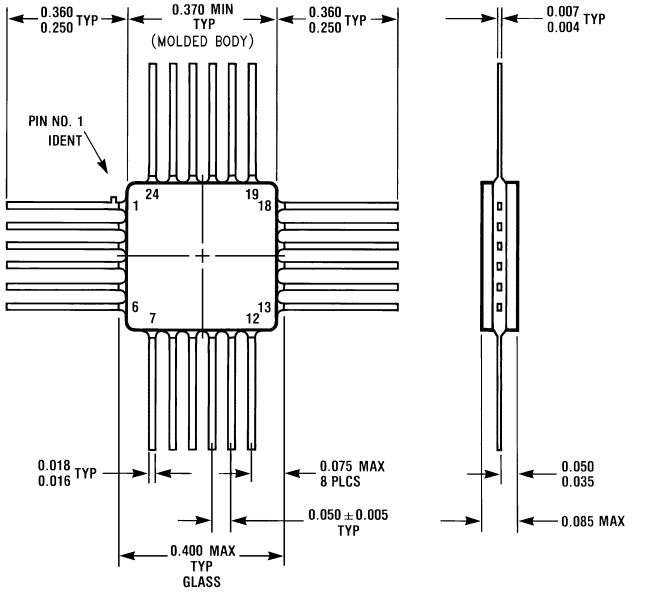
FIGURE 4. Data Setup and Hold Time



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24 Lead Quad Cerpak (F)
NS Package Number W24B

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