ERROR DETECTION and CORRECTION (EDC) UNIT

2960

FEATURES

- Boosts Memory Reliability Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold
- Very High Speed Perfect for MOS microprocessor minicomputer and mainframe systems.
 - Data in to error detect 32ns worst case

 Data in to corrected data out 65ns worst case High performance systems can use the Signetics EDC in the check-only mode to avoid memory system slowdown

- Replaces 25 to 50 MSI chips All necessary features are built-in to the Signetics 2960 including diagnostics data in data out and check bit latches
- Handles Data Words From 8 to 64 Bits The Signetics 2960 is cascadable: 1 EDC for 8 or 16 bits 2 for 32 bits 4 for 64 bits
- Easy Byte Operations Separate byte enables on the data out latch simplify the steps and cuts the time required for byte writes
- Built-in Diagnostics The processor may completely exercise the EDC under software control to check for proper operation.

PRODUCT DESCRIPTION

The Signetics 2960 Error Detection and Correction Unit (EDC) (Figure 1) contains the logic necessary to generate check bits on a 16-bit data field according to modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the EDC will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The 2960 can be expanded to operate 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Signetics 2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.



Figure 1. Block Diagram of 2960 Error Detection and Correction Unit