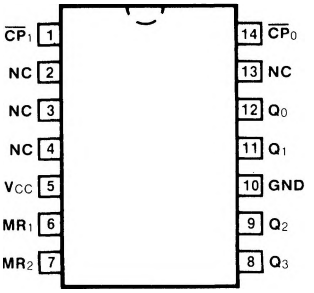
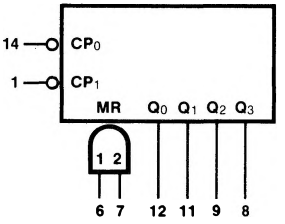
54/7492A
54LS/74LS92
DIVIDE-BY-TWELVE COUNTER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

DESCRIPTION — The '92 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-six. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7492APC, 74LS92PC		9A
Ceramic DIP (D)	A	7492ADC, 74LS92DC	5492ADM, 54LS92DM	6A
Flatpak (F)	A	7492AFC, 74LS92FC	5492AFM, 54LS92FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	0.125/1.5
$\overline{CP_1}$	÷6 Section Clock Input (Active Falling Edge)	3.0/3.0	0.250/2.0
MR_1, MR_2	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷6 Section Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

FUNCTIONAL DESCRIPTION — The '92 is a 4-bit ripple type divide-by-twelve counter. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divideby-six section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

MODE SELECTION TABLE

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

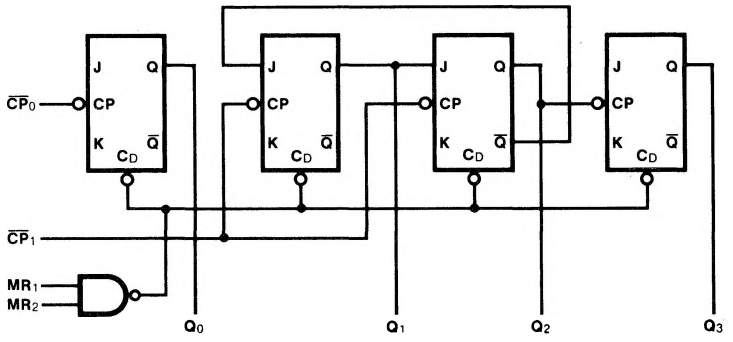
H = HIGH Voltage Level
L = LOW Voltage Level

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q_0 connected to $\overline{CP}_1$

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current, $\overline{CP_0}$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{IH}	Input HIGH Current, $\overline{CP_1}$		1.0		0.4	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current		39		15	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency, $\overline{CP_0}$ Input	32		32		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency, $\overline{CP_1}$ Input	16		16		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0		16 18		16 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_3		48 50		48 50	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3		32 35		32 35	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay, MR to Q_n		40		40	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	15		15		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	30		30		ns	
t_w (H)	MR Pulse Width HIGH	15		15		ns	Fig. 3-17
t_{rec}	Recovery Time, MR to CP	25		25		ns	