National Semiconductor

PRELIMINARY

74LCX16646
Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16646 contains sixteen non-inverting bidirectional registered bus transceivers with TRI-STATE® outputs, providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The four fundamental handling functions available are illustrated in *Figure 1* thru *Figure 4*.

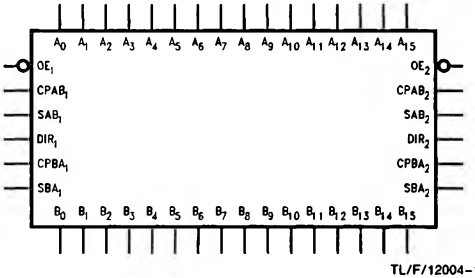
The LCX16646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model < 2000V
  Machine Model < 200V

Logic Symbol



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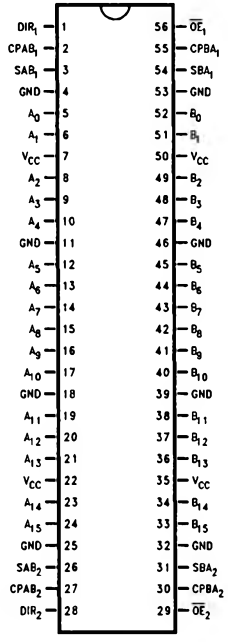
	SSOP	TSSOP
Order Number	74LCX16646MEA 74LCX16646MEAX	74LCX16646MTD 74LCX16646MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Real Time Transfer A-Bus to B-Bus

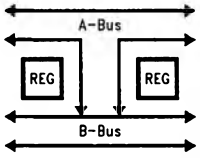

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

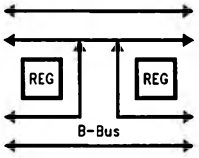

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FIGURE 2

Storage from Bus to Register

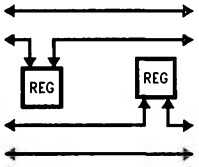

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FIGURE 3

Transfer from Register to Bus

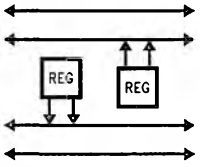

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FIGURE 4

Function Table (Note)

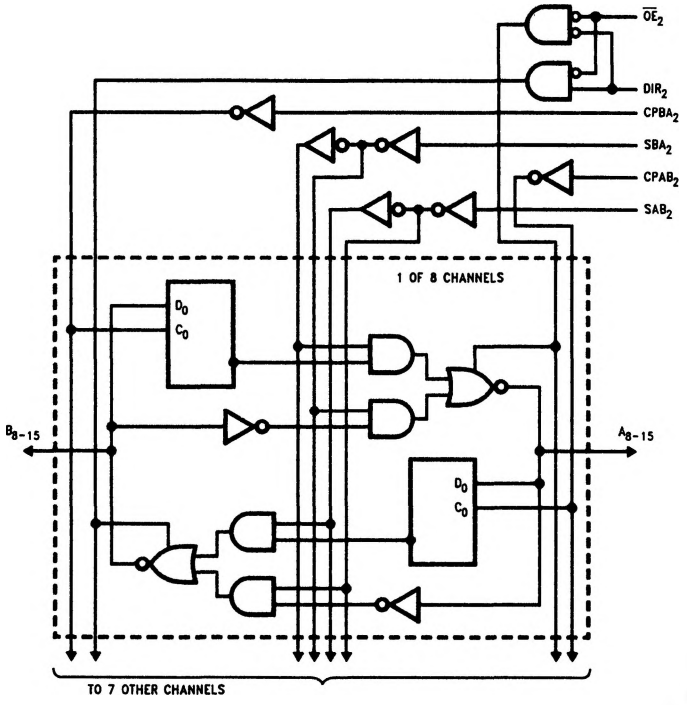
Inputs						Data I/O		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock An Data into A Register
H	X	X	↑	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↑	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L	Output	Input	Bn to An—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↑	X	H			Clock Bn into B Register and Output to An

Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level ↑ = LOW-to-HIGH Transition.

Logic Diagrams



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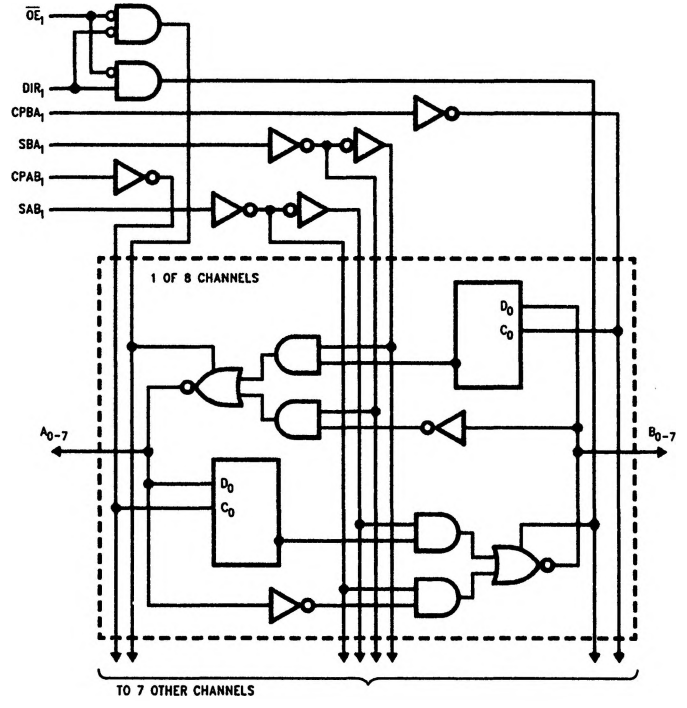

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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170				ns
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	5.0 5.0	1.5 1.5	6.0 6.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16646 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows: