## 74LCX652

## Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

## General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the $A$ or $B$ bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.
The LCX652 is designed for low voltage ( 3.3 V ) $\mathrm{V}_{\mathrm{CC}}$ applications with capability of interfacing to a 5 V signal environment.
The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5V tolerant inputs and outputs
- 7.0 ns tPD max, $10 \mu \mathrm{~A} \mathrm{I}_{\mathrm{CCQ}} \max$
- Power down high impedance inputs and outputs
- $2.0 \mathrm{~V}-3.6 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ supply operation
- $\pm 24 \mathrm{~mA}$ output drive
- Implements patented Quiet SeriesTM noise/EMI reduction circuitry
- Functionally compatible with 74 series 652
- Latch-up performance exceeds 500 mA
- ESD performance:

Human body model $>2000 \mathrm{~V}$ Machine model > 200V

## Logic Symbols

## Connection Diagram

IEEE/IEC


Pin Assignment for SOIC, SSOP and TSSOP


TL/F/11998-2

| Pin Names | Description |
| :--- | :--- |
| $A_{0}-A_{7}, B_{0}-B_{7}$ | A and B Inputs/TRI-STATE ${ }^{\oplus}$ Outputs |
| CPAB, CPBA | Clock Inputs |
| SAB, SBA | Select Inputs |
| OEAB, $\overline{O E B A}$ | Output Enable Inputs |


|  | SOIC JEDEC | SSOP Type II | TSSOP JEDEC |
| :--- | :---: | :---: | :---: |
| Order Number | 74LCX652WM <br> 74LCX652WMX | 74LCX652MSA <br> 74LCX652MSAX | 74LCX652MTC <br> 74LCX652MTCX |
| See NS Package <br> Number | M24B | MSA24 | MTC24 |

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.
The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.
Data on the $A$ or $B$ data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-
priate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal $D$ flip-flops by simultaneously enabling OEAB and $\overline{O E B A}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.


FIGURE 1

## Logic Diagram



TO 7 OTHER CHANNELS
TL/F/11998-4
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.
Function Table (Note)

| Inputs |  |  |  |  |  | Inputs/Outputs |  | Operating Mode |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OEAB | $\overline{\text { OEBA }}$ | CPAB | CPBA | SAB | SBA | $A_{0}$ thru $A_{7}$ | $B_{0}$ thru $B_{7}$ |  |
| L | H | HorL | HorL | X | X | Input | Input | Isolation |
| L | H | $\Gamma$ | $\sim$ | X | X |  |  | Store A and B Data |
| X | H | $\Gamma$ | HorL | X | X | Input | Not Specified | Store A, Hold B |
| H | H | $\Gamma$ | $\checkmark$ | X | X | Input | Output | Store $A$ in Both Registers |
| L | X | HorL | $\sim$ | X | X | Not Specified | Input | Hold A, Store B |
| L | L | $\Gamma$ | $\Omega$ | X | X | Output | Input | Store B in Both Registers |
| L | L | X | X | X | L | Output | Input | Real-Time B Data to A Bus |
| L | L | X | H or L | X | H |  |  | Store B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real-Time A Data to B Bus |
| H | H | HorL | X | H | X |  |  | Stored A Data to B Bus |
| H | L | HorL | HorL | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

$H=$ HIGH Voltage Level
$L=$ LOW Voltage Level
$\mathrm{X}=$ Immaterial
$\Gamma=$ LOW to HIGH Clock Transition
Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| Symbol | Parameter | Value | Conditions | Units |
| :---: | :---: | :---: | :---: | :---: |
| $V_{C C}$ | Supply Voltage | -0.5 to +7.0 |  | V |
| $\mathrm{V}_{1}$ | DC Input Voltage | -0.5 to +7.0 |  | V |
| $V_{0}$ | DC Output Voltage | -0.5 to +7.0 | Output in TRI-STATE | V |
|  |  | -0.5 to $V_{C C}+0.5$ | Output in High or Low State (Note 2) | $\checkmark$ |
| lıK | DC Input Diode Current | -50 | $\mathrm{V}_{1}<$ GND | mA |
| lok | DC Output Diode Current | $\begin{array}{r} -50 \\ +50 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{O}}<\mathrm{GND} \\ & \mathrm{~V}_{\mathrm{O}}>\mathrm{V}_{\mathrm{CC}} \end{aligned}$ | mA |
| 10 | DC Output Source/Sink Current | $\pm 50$ |  | mA |
| $I_{\text {CC }}$ | DC Supply Current per Supply Pin | $\pm 100$ |  | mA |
| IGND | DC Ground Current per Ground Pin | $\pm 100$ |  | mA |
| TSTG | Storage Temperature | -65 to +150 |  | ${ }^{\circ} \mathrm{C}$ |

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
Note 2: Io Absolute Maximum Rating must be observed.
Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: |
| VCC | Supply Voltage $\begin{array}{r}\text { Operating } \\ \text { Data Retention }\end{array}$ | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 3.6 \\ & 3.6 \end{aligned}$ | V |
| $V_{1}$ | Input Voltage | 0 | 5.5 | V |
| $\mathrm{V}_{0}$ | Output Voltage <br> HIGH or LOW State <br> TRI-STATE | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{gathered} V_{C C} \\ 5.5 \end{gathered}$ | V |
| $1 \mathrm{OH} / \mathrm{OL}$ | $\text { Output Current } \begin{array}{r} V_{C C}=3.0 \mathrm{~V}-3.6 \mathrm{~V} \\ V_{C C}=2.7 \mathrm{~V} \end{array}$ |  | $\begin{aligned} & \pm 24 \\ & \pm 12 \end{aligned}$ | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free-Air Operating Temperature | -40 | 85 | ${ }^{\circ} \mathrm{C}$ |
| $\Delta t / \Delta V$ | Input Edge Rate, $\mathrm{V}_{\mathrm{IN}}=0.8 \mathrm{~V}-2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ | 0 | 10 | ns/V |

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{c c}$ <br> (V) | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| $\mathrm{V}_{1 \mathrm{H}}$ | HIGH Level Input Voltage |  | 2.7-3.6 | 2.0 |  | V |
| $\mathrm{V}_{\text {IL }}$ | LOW Level Input Voltage |  | 2.7-3.6 |  | 0.8 | V |
| V OH | HIGH Level Output Voltage | $\mathrm{l}_{\mathrm{OH}}=-100 \mu \mathrm{~A}$ | 2.7-3.6 | $\mathrm{V}_{\mathrm{CC}}-0.2$ |  | V |
|  |  | $\mathrm{IOH}_{\mathrm{OH}}=-12 \mathrm{~mA}$ | 2.7 | 2.2 |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-18 \mathrm{~mA}$ | 3.0 | 2.4 |  | V |
|  |  | $\mathrm{IOH}=-24 \mathrm{~mA}$ | 3.0 | 2.2 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW Level Output Voltage | $\mathrm{lOL}^{\prime}=100 \mu \mathrm{~A}$ | 2.7-3.6 |  | 0.2 | V |
|  |  | $\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}$ | 2.7 |  | 0.4 | V |
|  |  | $\mathrm{l}_{\mathrm{OL}}=16 \mathrm{~mA}$ | 3.0 |  | 0.4 | V |
|  |  | $\mathrm{IOL}^{2}=24 \mathrm{~mA}$ | 3.0 |  | 0.55 | V |
| 1 | Input Leakage Current | $0 \leq \mathrm{V}_{1} \leq 5.5 \mathrm{~V}$ | 2.7-3.6 |  | $\pm 5.0$ | $\mu \mathrm{A}$ |
| loz | TRI-STATE I/O Leakage | $\begin{aligned} & 0 \leq V_{O} \leq 5.5 V \\ & V_{1}=V_{I H} \text { or } V_{I L} \end{aligned}$ | 2.7-3.6 |  | $\pm 5.0$ | $\mu \mathrm{A}$ |
| loff | Power-Off Leakage Current | $\mathrm{V}_{1}$ or $\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}$ | 0 |  | 100 | $\mu \mathrm{A}$ |
| Icc | Quiescent Supply Current | $V_{1}=V_{C C}$ or GND | 2.7-3.6 |  | 10 | $\mu \mathrm{A}$ |
|  |  | $3.6 \mathrm{~V} \leq \mathrm{V}_{1}, \mathrm{~V}_{\mathrm{O}} \leq 5.5 \mathrm{~V}$ | 2.7-3.6 |  | $\pm 10$ | $\mu \mathrm{A}$ |
| $\Delta l_{\text {CC }}$ | Increase in ICC per Input | $\mathrm{V}_{\text {IH }}=\mathrm{V}_{\mathrm{CC}}-0.6 \mathrm{~V}$ | 2.7-3.6 |  | 500 | $\mu \mathrm{A}$ |

## AC Electrical Characteristics

| Symbol | Parameter | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{\mathbf{C C}}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $f_{\text {max }}$ | Maximum Clock Frequency | 150 |  |  |  | MHz |
| $t_{\text {PHL }}$ $t_{\mathrm{PLH}}$ | Propagation Delay Bus to Bus | $\begin{aligned} & \hline 1.5 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 7.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \\ & \hline \end{aligned}$ | ns |
| $t_{\text {PHL }}$ <br> tple | Propagation Delay Clock to Bus | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 8.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 9.5 \end{aligned}$ | ns |
| ${ }^{\text {tpHL }}$ <br> tple | Propagation Delay Select to Bus | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 8.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 9.5 \end{aligned}$ | ns |
| $\begin{aligned} & \text { tpZL } \\ & t_{\mathrm{PLZH}} \\ & \hline \end{aligned}$ | Output Enable Time | $\begin{aligned} & \hline 1.5 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 8.5 \\ & 8.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 9.5 \\ & \hline \end{aligned}$ | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLZ}} \\ & \mathrm{t}_{\mathrm{PHZ}} \end{aligned}$ | Output Disable Time | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 8.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 9.5 \end{aligned}$ | ns |
| ts | Setup Time | 2.5 |  | 2.5 |  | ns |
| $t_{H}$ | Hold Time | 1.5 |  | 1.5 |  | ns |
| $t_{\text {w }}$ | Pulse Width | 3.3 |  | 3.3 |  | ns |
| $\begin{aligned} & \text { tOSHL } \\ & \text { toSLH } \\ & \hline \end{aligned}$ | Output to Output Skew (Note 1) |  | $\begin{aligned} & 1.0 \\ & 1.0 \\ & \hline \end{aligned}$ |  |  | ns |

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (LOSHU) or LOW to HIGH (LOSLH). Parameter guaranteed by design.

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | VCc <br> (V) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Typical |  |
| V OLP | Quiet Output Dynamic Peak $\mathrm{V}_{\text {OL }}$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{V}_{1 \mathrm{H}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V}$ | 3.3 | 0.8 | V |
| Volv | Quiet Output Dynamic Valley V $\mathrm{OL}^{\text {L }}$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{V}_{\mathrm{IH}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V}$ | 3.3 | 0.8 | V |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
| :--- | :--- | :---: | :---: | :---: |
| $\mathrm{C}_{I N}$ | Input Capacitance | $\mathrm{V}_{C C}=$ Open, $\mathrm{V}_{1}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | 7 | pF |
| $\mathrm{C}_{I / O}$ | Input/Output Capacitance | $\mathrm{V}_{C C}=3.3 \mathrm{~V}, \mathrm{~V}_{1}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | $\mathbf{8}$ | pF |
| $\mathrm{C}_{\mathrm{PD}}$ | Power Dissipation Capacitance | $\mathrm{V}_{C C}=3.3 \mathrm{~V}, \mathrm{~V}_{1}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}} \mathrm{F}=10 \mathrm{MHz}$ | 25 | pF |

## 74LCX652 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

| Temperature Range Family |
| :--- |
| $74=$ Commercial |

Device Type
Package Code
WM $=(0.300 "$ Wide) Molded Small Outline Package, JEDEC
MTC $=$ Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body
Width

