## DESCRIPTION

The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel in-parallel out register applications. They are also suitable for general purpose applications as parallel in-serial out, serial in-parallel out registers.

The flip-flops are arranged as dual 5 arrays, ( 8200 \& 8201) and single 10 arrays with reset, ( $8202 \& 8203$ ). The true output of each bit is made available to the user.

The 8200 and 8202 feature true " $D$ " inputs. The logic state presented at these "D" inputs will appear at the 0 outputs after a negative transition of the clock.
The 8201 and 8203 feature complementing " $D$ " inputs (" $\overline{\mathrm{D}}$ "). The logic state presented at these " $\overline{\mathrm{D}}$ " inputs will invert and appear at the $\mathbf{Q}$ outputs after a negative going transition of the clock. This complementing input feature (" $\bar{D}$ ") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

## LOGIC DIAGRAMS AND TRUTH TABLES



10-BIT BUFFER REGISTER


| $\mathrm{D}_{n}$ | $\overline{\text { RESET }}$ | $a_{n+1}$ |
| :---: | :---: | :---: |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

```
RESET = 0=>O = 0
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK
```

LOGIC DIAGRAMS AND TRUTH TABLES (Cont'd)


ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS |  |  |
| Propagation Delay |  |  |  |  |  |  |
| $t_{\text {on }}$ Clock to $Q$ |  | 30 | 45 | ns |  | 8 |
| $t_{\text {off }}$ Clock to Q |  | 25 | 40 | ns |  | 8 |
| $t_{\text {on }}$ Reset to 0 |  | 30 | 45 | ns |  | 8 |
| Set Up Time |  | 6 | 15 | ns |  | 10 |
| Hold Time |  | 0 | 5 | ns |  | 12 |
| Minimum Clock Width |  | 12 | 17 | ns |  |  |
| Transfer Rate | 15 | 35 |  | MHz |  | 8 |
| Output Short Circuit Current | -20 |  | -70 | mA |  |  |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to $\mathrm{V}_{\mathrm{CC}}$ -
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
"UP" Level = "1", "DOWN" Level = "0 ":
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Set Up Time defined as data presence before clock.
11. Outputs are in the low state for this test.
12. Hold time defined as data presence after clock.
13. $V_{C C}=5.25$ volts.

## SCHEMATIC DIAGRAMS



ton FROM $\overline{\text { RESET TO } Q}$


INPUT PULSE:
Amplitude $=2.6 \mathrm{~V}$
Clock: P.R.R. $=5 \mathrm{MHz}$
Reset: P.R.R. $=5 \mathrm{MHz}$
PW = $\mathbf{3 0}$ ns (at 50\% point) $t_{r}=t_{f}=5 \mathrm{~ns}$

TYPICAL APPLICATIONS
20 BIT (4 WORDS $\times 5$ BITS EACH) MEMORY CELL


Total Package Count $=\mathbf{2 - 8 2 0 0}$ 's
ONE OUT OF TEN - COUNTER/DISPLAY (SELF-CORRECTING)


TYPICAL APPLICATIONS (Cont'd)
M ULTIPLICATION AT 10 MHz OF A 20-BIT BINARY WORD

$P_{n}=\left(X_{n}\right) M$ WHERE $X_{n} \equiv$ MULTIPLICAND
M $\equiv$ MULTIPLIER
TOTAL PACKAGE COUNT $=9$ PACKAGES (4-8202'S AND 5.8260'S)


