signetics

256 BIT-BIPOLAR FIELD-PROGRAMMABLE READ ONLY MEMORY (FROM)

8223

REFER TO PAGE 13 FOR B AND E PIN CONFIGURATIONS.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8223 is a TTL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip select input is high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which permits wired-OR operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum. The 8223 may be programmed to any desired pattern by the user. (See fusing procedure.) This feature is ideal for prototype hardware and systems requiring propriety codes.

A Truth Table/Order Blank is included on page 199 for ordering custom patterns.

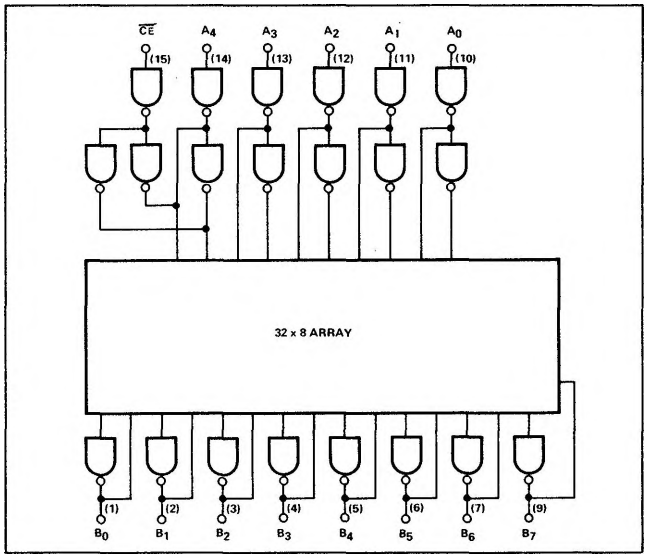
FEATURES

- **BUFFERED ADDRESS LINES**
- **ON THE CHIP DECODING**
- **CHIP ENABLE CONTROL LINE**
- **OPEN COLLECTOR OUTPUTS**
- **DIODE PROTECTED INPUTS**
- **NO SEPARATE FUSING PINS**

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
"1" Output Leakage Current			100	μA			2.0V		13
"0" Output Voltage			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
"1" Input Current									
An, Address			40	μA		4.5V			
$\overline{\text{Chip Enable}}$ Input			80	μA			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1		-1.6	mA	0.4V		0.4V		

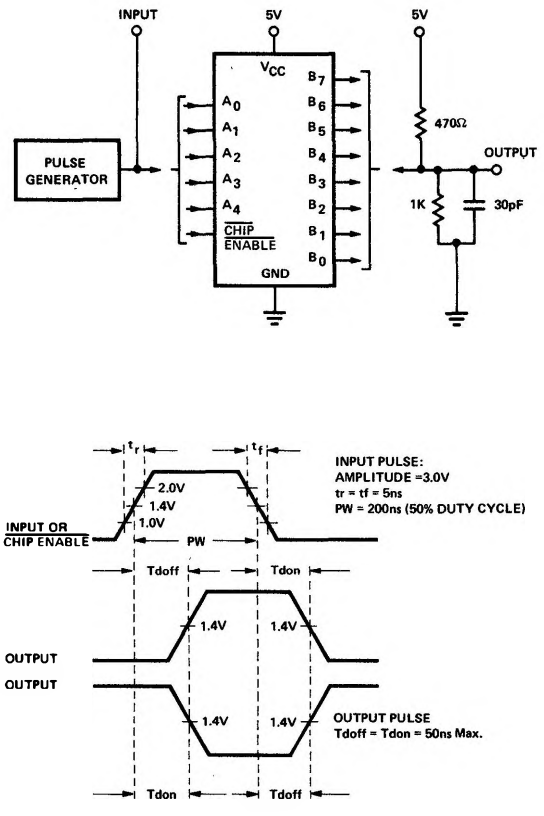
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
Propagation Delay									
An to Bn		35	50	ns				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to B_n		35	50	ns		4.5V	4.5V	DC F.O.=12	7,12
Power Consumption		310	400	mW		4.5V	4.5V		14
Input Latch Voltage	5.5			V			10mA		11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1" "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
14. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



Ground Pin 15 When Testing Address-Output Delays

FUSING PROCEDURE

The 8223 may be programmed by using Curtis Electro Devices PR23 Series or Spectrum Dynamics 300 and 400 Series Programmers. Each perform for the procedure outlined.

The 8223 Standard part is shipped with all outputs at Logical "0". To write a Logical "1" proceed as follows:

1. Remove V_{CC}.
2. Remove any load from the outputs.
3. Ground the $\overline{\text{Chip Enable}}$.
4. Address the desired location by applying ground for a "0" and 5.0±0.25V for a "1" at the address input lines.
5. Apply +12.5V to the output to be programmed through a 390Ω ±10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 50msec (1.0sec max.) Do not exceed a 25% duty cycle. Limit the V_{CC} overshoot to 1.0 volts, max, by "clamping" or "crowbar" circuit. V_{CC} current requirement is 400mA max at 12.5 volts.
7. Remove V_{CC}.
8. Open the output.
9. Proceed to the next output and repeat, or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 8223.