## DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.
The 8230 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the $f$ output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, the $\bar{f}$ output is unconditionally low and the foutput is unconditionally high. The 8230 is a functional and pin-for-pin replacement for the 9312.
The 8231 is a variation of the 8230 that provides open collector output $\overline{\mathrm{f}}$ for expansion of input terms. The 8232 is similar to the 8230 except in the effect of the INHIBIT input on the $\bar{f}$ output. With the INHIBIT low, the selected input appears at the $f$ output and, in complement, on the $\bar{\ddagger}$ output. With the INHIBIT input high, both the fand the $\bar{f}$ output are unconditionally low.

DIGITAL 8000 SERIES TTL/MSI
TRUTH TABLE

| ADDRESS |  |  | DATA INPUTS |  |  |  |  |  |  |  |  | OUTPUT |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $A_{2}$ | $A_{1}$ | A0 | 17 | 16 | 15 | 14 | 13 | $\mathrm{l}_{2}$ | 11 | 10 | INH | $f$ | $\begin{gathered} 8230 \\ 8231 \\ \bar{f} \end{gathered}$ | $\frac{8232}{f}$ |
| 0 | 0 | 0 | $x$ | $x$ | $x$ | x | x | x | x | 1 | 0 | , | 0 | 0 |
| 0 | 0 | 1 | $x$ | $\times$ | $x$ | x | x | x | 1 | x | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | $x$ | $x$ | $x$ | x | x | 1 | $x$ | x | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | $x$ | x | $x$ | x | 1 | x | x | x | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | $x$ | $\times$ | x | 1 | x | $\times$ | x | $\times$ | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | $x$ | x | 1 | x | x | $x$ | $x$ | x | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | x | 1 | x | x | $x$ | $x$ | $x$ | x | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | $x$ | x | $x$ | $x$ | $x$ | $x$ | x | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | x | x | x | x | $x$ | x | $x$ | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | $x$ | x | x | x | $x$ | x | 0 | x | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | $x$ | x | x | x | $x$ | 0 | x | x | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | $x$ | x | x | x | 0 | $\times$ | $x$ | x | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | x | $x$ | x | 0 | x | x | $x$ | x | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | x | $x$ | 0 | x | x | x | x | $x$ | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | $x$ | 0 | $x$ | x | x | $x$ | $x$ | x | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | x | $x$ | $x$ | $x$ | $x$ | $x$ | $x$ | 0 | 0 | 1 | 1 |
| x | $\times$ | $\times$ | x | x | x | x | x | $x$ | x | x | 1 | 0 | 1 | 0 |

$x=$ don't care

## LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | $A_{1}$ | $A_{2}$ | $A_{3}$ | INH | DATA INPUT In | OUTPUTS |  |
| "1'" Output Voltage, Output f | 2.6 | 3.5 |  | V | * | * | * | 0.8V | 2.0 V | -800mA | 6,11 |
| Output $\bar{f}(8230,8232)$ | 2.6 | 3.5 |  | V | * | * | * | 2.0 V | * | $-800 \mu \mathrm{~A}$ | 6, 11 |
| "1" Output Leakage Current, Output $\bar{f}$ (8231) |  |  | 150 | $\mu \mathrm{A}$ | 0.8V | 2.0 V | 2.0 V | 2.0 V | 0.6 V |  | 14 |
| "0" Output Voltage |  |  | 0.4 | V | 0.8V | 0.8V | 0.8V | 0.8V | 0.8V | 16 mA | 7.11 |
| "1" Input Current |  |  |  |  |  |  |  |  |  |  |  |
| Inputs An, $\mathrm{I}_{\mathrm{n}}$ |  |  | 40 | $\mu \mathrm{A}$ | 4.5 V | 4.5V | 4.5 V |  | 4.5 V |  |  |
| Input INH, 8230 \& 8231 |  |  | 80 | $\mu \mathrm{A}$ |  |  |  | 4.5 V |  |  |  |
| Input INH, 8232 |  |  | 80 | $\mu \mathrm{A}$ |  |  |  | 4.5 V |  |  |  |
| '00' Input Current |  |  |  |  |  |  |  |  |  |  |  |
| $A_{n} \cdot I_{n}, 1 N H$ (8230 \& 8231) | -0.1 |  | -1.6 | mA | 0.4V | 0.4V | 0.4 V |  | 0.4 V |  |  |
| INH, (8232) | -0.1 |  | -3.2 | mA |  |  |  | 0.4V |  |  |  |

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | A | A | A | INH | DATA INPUT In | OUTPUTS <br> f $\quad$ f |  |
| Propagation Delay |  |  |  |  |  |  |  |  |  |  |  |
| $A_{n}$ to $\bar{f}(8230,8232)$ |  | 19 | 30 | ns |  |  |  |  |  |  | 8 |
| $A_{n}$ to $\bar{f}$ (8231) |  | 17 | 30 | ns |  |  |  |  |  |  | 8 |
| $I_{n}$ to $\bar{f}(8230,8232)$ |  | 11 | 20 | ns |  |  |  |  |  |  | 8 |
| $\bar{f}$ to f |  | 10 | 15 | ns |  |  |  |  |  |  | 8 |
| $I_{n}$ to $\bar{f}$ (8231) |  | 13 | 24 | ns |  |  |  |  |  |  | 8 |
| INH to $\overline{\mathrm{f}}$ (8230, 8231) |  | 18 | 30 | ns |  |  |  |  |  |  | 8 |
| INH to for $\overline{\mathrm{f}}$ (8232) |  | 11 | 20 | ns |  |  |  |  |  |  | 8 |
| Power Consumption/Supply Current |  |  |  |  |  |  |  |  |  |  |  |
| 8230, 8231 |  |  | $\begin{aligned} & 250 / \\ & 47.7 \end{aligned}$ | $\mathrm{mW} / \mathrm{mA}$ | 4.5 V | 4.5V | 4.5V | 4.5V | OV |  | 13 |
| 8232 |  |  | $\begin{aligned} & 2621 \\ & 50.0 \end{aligned}$ | $\mathrm{mW} / \mathrm{mA}$ | 4.5 V | 4.5 V | 4.5V | 4.5 V | OV |  | 13 |
| Output Short Circuit Current |  |  |  |  |  |  |  |  |  |  |  |
| Output f | -20 |  | -70 | mA | OV | OV | OV | OV | 4.5 V | OV |  |
| Output $\overline{\mathrm{f}}(8230,8232)$ | -20 |  | -70 | $m A$ | OV | OV | OV | OV | OV | OV |  |
| Input Latch Voltage | 5.5 |  |  | $\checkmark$ | 10 mA | 10 mA | 10 mA | 10 mA | 10 mA |  | 12 |

## *See Truth Table for Logical Conditions

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level $=" 1 "$ " "DOWN" Level $=$ " 0 ".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to ${ }^{\mathbf{C C}}{ }^{\circ}$
8. Refer to AC Test figures.
9. One AC fan-out is defined as 50pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8 V for logical " 0 " and 2.0 V for logical " 1 ".
12. This test guarantees operation free of input latch-up over the specific operating power supply voltage range.
13. All $I_{n}$ data inputs are at $O V$. $V_{C C}=5.25 \mathrm{~V}$.
14. Connect an external 1 k resistor from $\mathrm{V}_{\mathrm{CC}}$ to the output terminal for this test.

## SCHEMATIC DIAGRAMS



AC TEST FIGURE AND WAVEFORMS


NON-INVERTING PATHS

$t_{r}=t_{f} \geq 3 n s$


## INVERTING PATHS



NOTES:

1. $5 K, 30 p F$ load includes test jigs and scope impedance.
2. Scope terminals to be $\leqslant 1 \frac{1}{2}$ " from package pins.
3. See truth table for logical conditions.

AC TEST CONDITIONS

| STEP NO. | TYPE/S | $\begin{aligned} & \text { DELAY } \\ & \text { FROM-TO } \end{aligned}$ | INPUTS |  |  |  | WAVE <br> FORM <br> TYPE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $l_{0}$ | 11 | $A_{0}$ | INH |  |
| 1 | ALL | $A_{0}$ to $\bar{f}$ | 0 V | Vcc | P.G. | 0 V | C, D |
| 2 | ALL | 10 to $\bar{f}$ | P. G. | 0 V | 0 V | 0 V | C, D |
| 3 | ALL | f to ${ }^{\text {* }}$ | P. G. | 0 V | 0 V | 0 V | C. D |
| 4 | 8230 | INH to f | $\mathrm{V}_{\text {cc }}$ | 0 V | 0 V | P. G. | A, B |
| 5 | 8231 | INH to $\bar{f}$ | 0 V | 0 V | 0 V | P. G. | C, D |
| 6 | 8232 | INH to f | $V_{\text {cc }}$ | 0 V | 0 V | P. G. | C, D |

NOTE: 1. P. G. = Pulse Generator

- Both $\mathbf{f}$ and $\overline{\mathbf{f}}$ are simultaneously loaded.

TYPICAL APPLICATIONS
EXPANSION OF 8231 TO MULTIPLEXER 64 LINES

${ }^{\cdot} f_{n}=f_{0}+f_{1}+f_{2} \ldots . f_{7}$
True Output
All Outputs may be tied together
to drive $8 \times 16 \mathrm{~mA}$ (eight 1.6 mA F.O.) or each Output may drive separately
ten 1.6 mA F.O.

Note:
Each 8231 has 8 data inputs which are not shown.

