DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.
The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

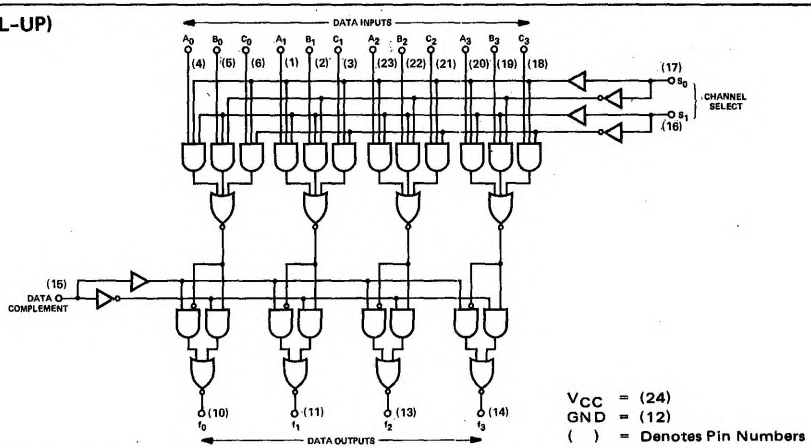
TRUTH TABLE

Data Input A_n B_n C_n	Channel Select S_0 S_1	Data Complement	Output Enable (8264)	Data Outputs
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	$\overline{A_n}$
x B_n x	0 1	1	1	$\overline{B_n}$
x x C_n	1 0	1	1	$\overline{C_n}$
x x x	0 0	1	1	1
x x x	x x	x	0	1

X = Either State

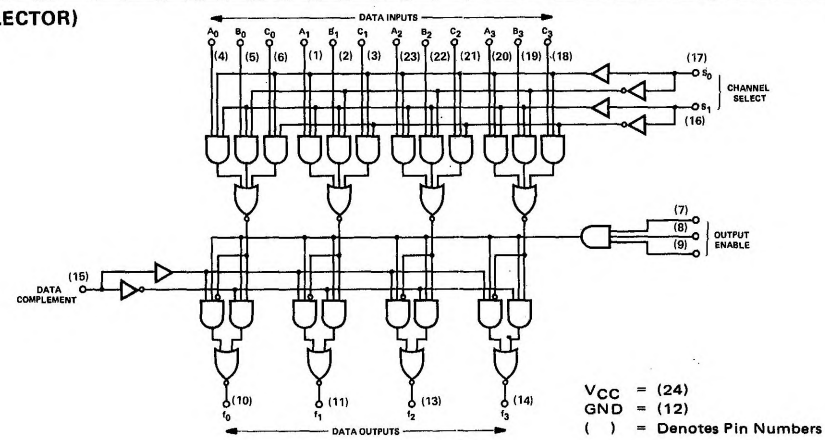
LOGIC DIAGRAMS

8263 (ACTIVE PULL-UP)



V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8264 (OPEN COLLECTOR)



V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	C_n	S_0	S_1	DATA COMP	OUTPUT ENABLE	OUTPUTS	
"1" Output Voltage (8263)	2.6	3.5		V	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V		-800μA	6
"1" Output Leakage Current (8264)			200	μA	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V	2.0V		8
"0" Output Voltage (8263)			0.4	V	0.8V	0.8V	0.8V	2.0V	2.0V	0.8V		9.6mA	7
"0" Output Voltage (8264)			0.4	V	0.8V							16.0mA	7
"0" Input Current													
A_n	-0.1		-1.6	mA	0.4V								
B_n	-0.1		-1.6	mA		0.4V		0.4V					
C_n	-0.1		-1.6	mA			0.4V		0.4V				
OE, DC	-0.1		-1.6	mA						0.4V	0.4V		
S_0, S_1	-0.1		-3.2	mA				0.4V	0.4V				
"1" Input Current													
A_n			40	μA	4.5V			0V	0V				
B_n			40	μA		4.5V			0V				
C_n			40	μA			4.5V	0V					
OE, DC			40	μA						4.5V	4.5V		
S_0, S_1			80	μA				4.5V	4.5V				

$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

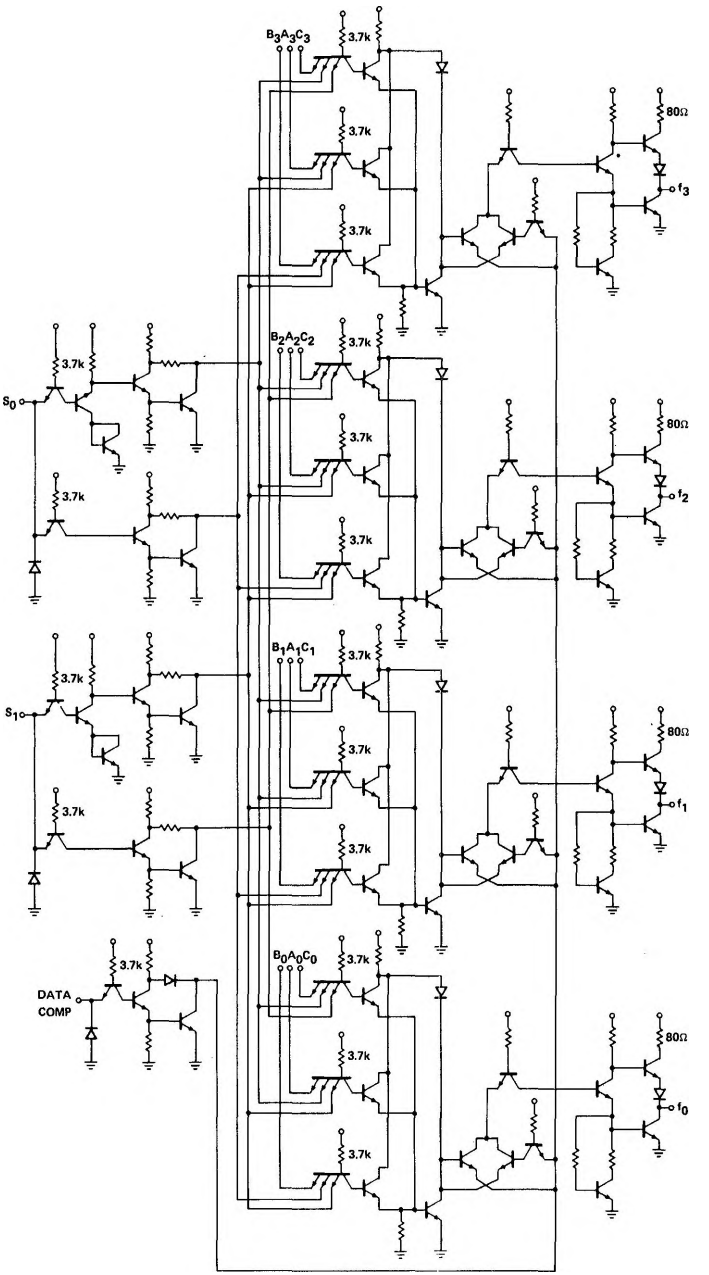
CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	C_n	S_0	S_1	DATA COMP	OUTPUT ENABLE	OUTPUTS	
Propagation Delay (8263)													
A_n to f_n		17	26	ns									10
S_0, S_1 to f_n		25	36	ns									10
DC to f_n		17	26	ns									10
Propagation Delay (8264)													
A_n to f_n		25	36	ns									10
S_0, S_1 to f_n		25	36	ns									10
DC to f_n		20	30	ns									10
OE to f_n		20	30	ns									10
Input Voltage Rating													
A_n	5.5			V	10mA			0V	0V				
B_n	5.5			V		10mA			0V				
C_n	5.5			V			10mA	0V					
S_0	5.5			V				10mA					
S_1	5.5			V					10mA				
DC	5.5			V						10mA			
OE	5.5			V							10mA		
Output Short Circuit Current (82S63)	-20		-70	mA								0V	9, 11
Power/Current Consumption													9
(8263)		378/ 72	420/ 80	mW/ mA				0V					
(8264)		400/ 76	475/ 90.4	mW/ mA				0V					

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
9. $V_{CC} = 5.25V$.
10. Refer to AC test figure.
11. Not more than one output should be shorted at a time.

7.

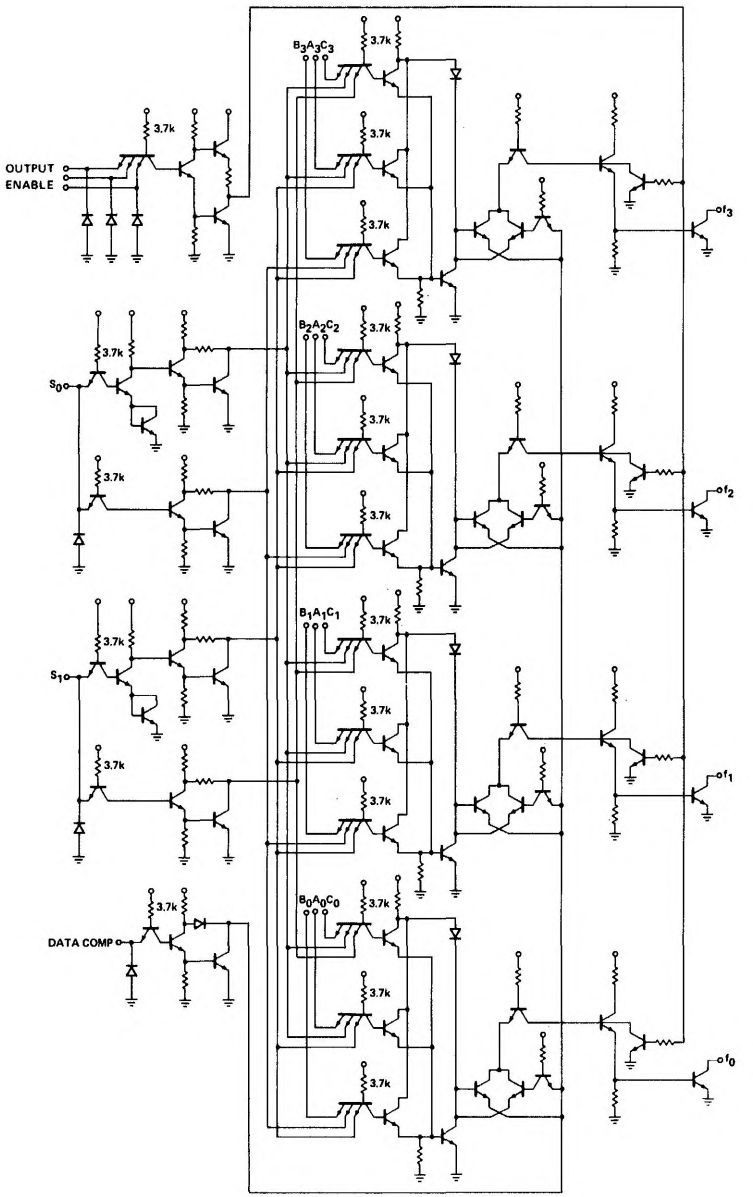
SCHEMATIC DIAGRAMS

8263



SCHEMATIC DIAGRAMS (Cont'd)

8264



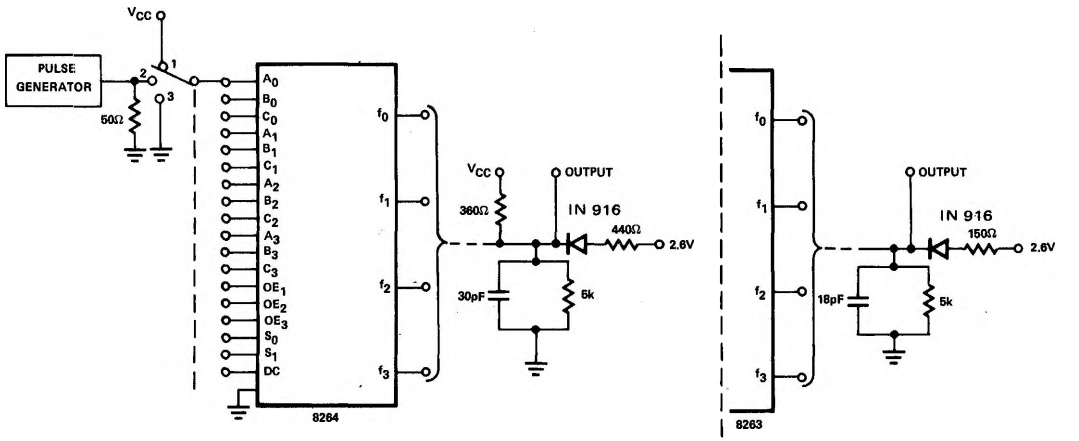
AC TESTING

Step No.	Delay From-To	Driven Inputs	Switching Positions: Other Inputs																	Waveform Types
			A_0	B_0	C_0	A_1	B_1	C_1	A_2	B_2	C_2	A_3	B_3	C_3	OE	OE	OE	S_0	S_1	DC	
1	A_n to f_n	2	2	1	1	2	1	1	2	1	1	2	1	1	1	1	1	1	1	1	C, D
2	S_0 to f_n	2	3	1	1	3	1	1	3	1	1	3	1	1	1	1	1	2	1	1	A, B
3	S_0 to f_n	2	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	1	C, D
4	S_1 to f_n	2	1	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	C, D
5	DC to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	C, D
6	OE_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	*	*	*	1	1	1	C, D

NOTE: Step number 6 is for 8264 only.

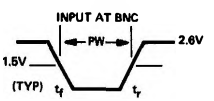
* Test one input at a time - others remain at "1".

AC TEST FIGURE AND WAVEFORMS

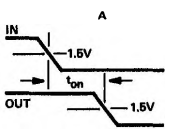


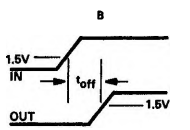
NOTE:
1. Scope terminals to be < 1½" from package pins.
2. Position 1 on switch provides a logical "1".
3. Position 2 on switch provides pulse. Position 3 on switch provides a logical "0".
4. All measurements are made at 1.5V level.
5. See truth table for logical conditions.

NON-INVERTING PATHS

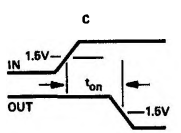


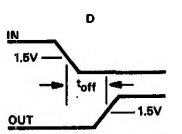
$t_r = t_f < 3ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz





INVERTING PATHS





TYPICAL APPLICATIONS

An approach to expanding the 8264 (bare collector output) is shown in Figure 1. The idea is to use common collectors with external pull-up resistors (one resistor for each of the four outputs) and make use of the output enable code.

As can be seen, the channel select lines are tied common, while a different enable code would be used to select a particular 8264. All non-selected 8264's have their outputs in the logic "1" condition, thus allowing the selected multiplexer to predominate.

Figure 2 illustrates a typical example using the 8263 (totem pole output) along with the 8281 (4-bit binary counter) and the 8270/71 (4-bit shift register), to implement a variable modulus counter. The 8270's act as a 3-register memory. The outputs of the 8270's are fed to the corresponding inputs of the 8263. Now there are three different presettable 4-bit words that can be chosen by the 8264. By alternating the channel select codes, the 8281 counter is preset with one of three words and produces an output whose repetition rate is dependent on the inputs from the multiplexer.

EXPANDING THE 8264

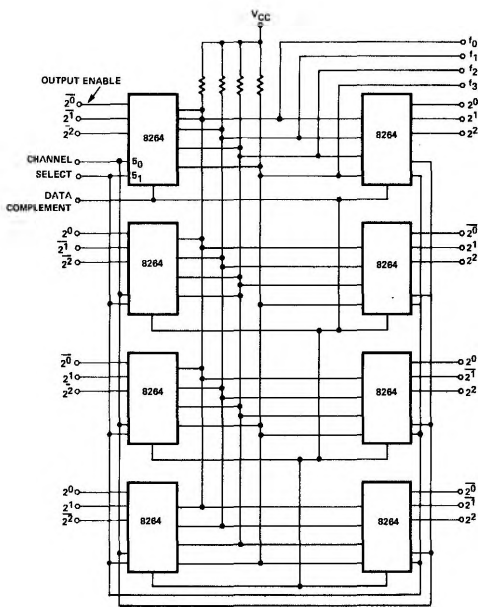


FIGURE 1

VARIABLE MODULUS COUNTER

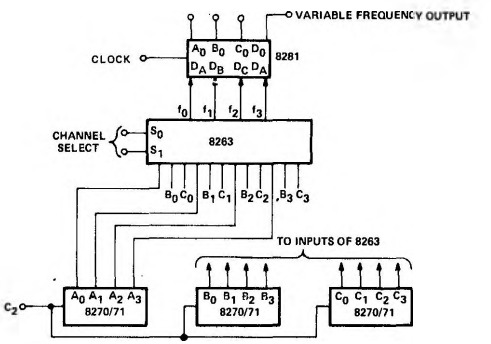


FIGURE 2