BINARY HEXADECIMAL AND BCD DECADE,
SYNCHRONOUS UP/DOWN COUNTERS

A,F,W PACKAGES

DIGITAL 8000 SERIES TTL/MSI

## DESCRIPTION

The Up/Down Counter is a monolithic MSI circuit containing gates and binaries interconnected to provide a bidirectional divide-by-ten (decade) or divide-by-sixteen (hexadecimal) result as a function of the clock input.
The output code of the decade up/down counter is the commonly used BCD (8421) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9.

The hexadecimal up/down counter provides the output sequence 0 through 15 which is presented in a weighted binary code (8421).

Set and Reset on the binary elements provide asynchronous entry with respect to the clock line, causing a count of " 0 " or " 15 " (8284) or of " 0 " or " 9 " (8285), and also inhibit propagation of count enable data.

Entry and propagation of data is performed in a synchronous manner with the clock line, which is active on its negative going excursion. The input from a previous stage or other source is channeled through "Carry $\mathrm{In}^{\prime \prime}$ and its propagation can be inhibited by the "Count Enable" line. "Carry In" and "Count Enable" input duality gives added flexibility in multiple package cascading applications.

Direction of the counter is steered from a single line (Up/ $\overline{\text { Down }})$, where a " 0 " level will cause a "down" count and a " 1 " level will accomplish an "up" count.

In addition to all $\mathbf{Q}$ outputs of the four binaries the $\overline{\mathbf{O}}$ output of the most significant binary (04) and the Carry Out term are available.

## LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | SET | RESET | UP/DOWN | COUNT ENABLE | CLOCK | CARRY IN | OUTPUTS |  |
| Power/Current Consumption |  | $\begin{gathered} 315 / \\ 60 \end{gathered}$ | $\begin{gathered} 420 / \\ 80 \end{gathered}$ | $\mathrm{mW} /$ $\mathrm{mA}$ |  |  |  |  |  |  |  | 10 |
| $t_{\text {on }}$ Clock to $\mathrm{O}_{4}$ \& $\overline{\mathrm{a}}_{4}$ |  | 32 | 45 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {on }}$ Clock to $\mathrm{a}_{1}, \mathrm{Q}_{2}, \mathrm{Q}_{3}$ |  | 28 | 40 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {off }} \text { Clock to } Q_{n}, \overline{\mathrm{O}}_{n}$ |  | 25 | 35 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {on }}$ Reset to $\mathrm{Q}_{\mathrm{n}}$ |  | 24 | 35 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {off }}$ Set to $Q_{n}$ |  | 15 | 25 | ns |  |  |  |  |  |  |  | 7 |
| $t$ on Reset to $\overline{\mathrm{a}}_{n}$ |  | 32 | 45 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {on }}$ Carry In to Carry Out |  | 15 | 25 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {off }}$ Carry In to Carry Out |  | 20 | 30 | ns |  |  |  |  |  |  |  | 7 |
| Clock Min. "1" Interval | $20^{\circ}$ | 15 |  | ns |  |  |  |  |  |  |  | 7 |
| Count Rate | 20 | 30 |  | MHz |  |  |  |  |  |  |  |  |
| Carry In, Count Enable, \& Up/Down Set-Up Time |  | 15 | 25 | ns |  |  |  |  |  |  |  |  |
| Carry In, Count Enable |  |  |  |  |  |  |  |  |  |  |  |  |
| \& Up/Down Hold Time |  | 0 | 2 | ns |  |  |  |  |  |  |  |  |
| Set/Reset Pulse Width |  | 20 | 25 | ns |  |  |  |  |  |  |  |  |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zerovolts
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
"UP" Level = "1", "DOWN" Level = "0".
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to $V_{C C}$
7. Refer to AC Test Figure.
8. Not more then one output should be shorted at a time.
9. Connect $Q_{4}$ to count enable, set the counter (1001), and count down. The counter will halt at BCD-7 (0111).
10. $V_{C C}=5.25$ volts. I

AC TEST FIGURES AND WAVEFORMS

## MODE OF OPERATION

|  | $\begin{aligned} & 8284 \\ & 8285 \end{aligned}$ | Binary Synchronous Up/Down Counter BCD Synchronous Up/Down Counter |  |  |  | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | SET | RESET | CARRYIN | COUNT <br> ENABLE | UP/DOWN |  |
| A. Asynchronous |  |  |  |  |  |  |
| 8284 Only | 0 | 1 | X | X | $\underline{x}$ | "15" ( $\left.\begin{array}{l}1 \\ 1\end{array} 111\right)$ |
| 8285 Only | 0 | 1 | X | X | X | "9" (1001) |
| B. Synchronous |  |  |  |  |  |  |
|  | 1 | 1 | $\times$ | 0 | X | Hold* |
|  | 1 | 1 | 1 | 1 | 0 | "Down" Count * |
|  | 1 | 1 | 1 | 1 | 1 | "Up" Count* |

*Function is synchronous with NEGATIVE going transition of the Clock pin.
$X=$ don't care.
CARRY OUT
Carry Out8284 $=$ Carry $\ln 1 \mathrm{Q}_{1} \mathrm{Q}_{2} \mathrm{Q}_{3} \mathrm{Q}_{4} \mathrm{UP}+{\overline{\alpha_{1}}} \overline{\mathrm{O}}_{2} \mathrm{C}_{3} \overline{\mathrm{Q}}_{4} \overline{\text { DOWN }}$
Carry Out8285 $=$ Carry $\operatorname{In} 1 \mathrm{Q}_{1} \mathrm{Q}_{4}$ UP $+\overline{\mathrm{C}}_{1} \overline{\mathrm{C}}_{2} \overline{\mathrm{Q}}_{3} \overline{\mathrm{Q}}_{4} \overline{\mathrm{DOWN}}$


AC TEST FIGURES AND WAVEFORMS (Cont'd)


## TYPICAL APPLICATIONS

## SYNCHRONOUS EXPANSION UP/DOWN COUNTERS



