

DESCRIPTION

The 82S190 and 82S191 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S190 and 82S191 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 3 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S190 and 82S191 devices are available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82S190/191, I, and for the military temperature range (-55°C to +125°C) specify S82S190/191, I.

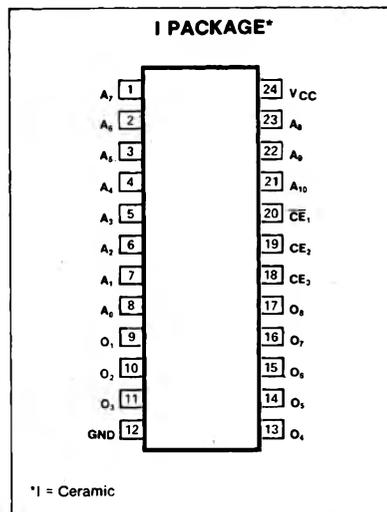
FEATURES

- **Address access time:**
N82S190/191: 80ns max
S82S190/: 100ns max
- **Power dissipation :** 40µW/bit typ
- **input loading:**
N82S190/191: -100µA max
S82S190/191: -150µA max
- 3 chip enable inputs
- On-chip address decoding
- **Output options:**
82S190: Open collector
82S191: Tri-state
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

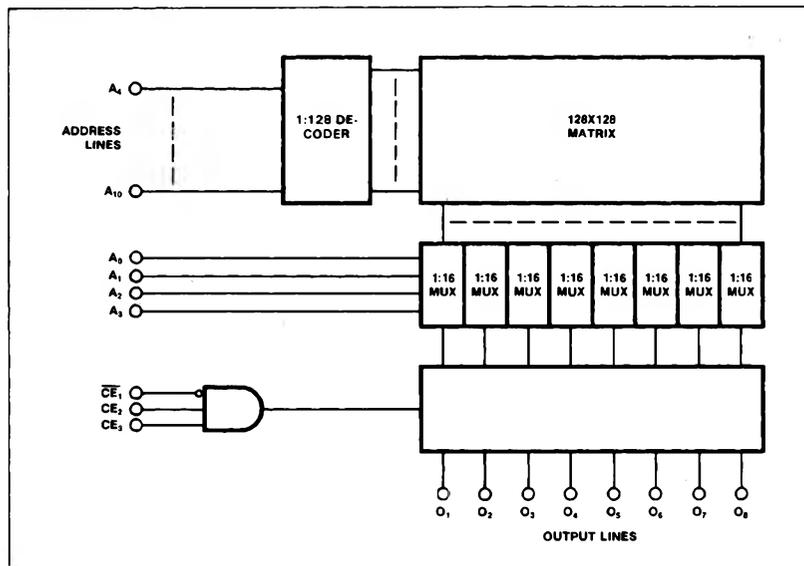
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
VCC	Supply voltage	+7	Vdc
VIN	Input voltage	+5.5	Vdc
VOH	Output voltage	+5.5	Vdc
VO	Off-state (82S141)	+5.5	Vdc
TA	Temperature range		°C
	Operating	0 to +75	
	N82S190/191	-55 to +125	
	S82S190/191		
TSTG	Storage	-65 to +150	

OBJECTIVE SPECIFICATION

82S190-I • 82S191-I

DC ELECTRICAL CHARACTERISTICS N82S190/191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S190/191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ¹	N82S190/191			S82S190/191			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA			.85			.80	V
V _{OL} V _{OH}	Output voltage Low High (82S191) I _{OUT} = 9.6mA I _{OUT} = -2mA, CE ₁ = Low, CE ₂ = High, CE ₃ = High, High stored			0.45			0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{OLK} I _{O(OFF)}	Output current Leakage (82S190) Hi-Z state (82S191)			40 -40			60 -60	μA
I _{OS}	Short circuit (82S191) V _{OUT} = 5.5V, CE ₁ = High, CE ₂ = Low, CE ₃ = Low V _{OUT} = 0.5V, CE ₁ = High, CE ₂ = Low, CE ₃ = Low V _{OUT} = 5.5V, CE ₁ = High, CE ₂ = Low, CE ₃ = Low V _{OUT} = 0V			40 -40			60 -60	μA
I _{CC}	V _{CC} supply current		130	175		130	185	mA
C _{IN} C _{OUT}	Capacitance Input Output V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S190/191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S190/191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S190/191			S82S190/191			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T _{AA} T _{CE}	Access time Output Output	Address Chip enable		50 20	80 40		50 20	100 50	ns
T _{CD}	Disable time Output	Chip disable		20	40		20	50	ns

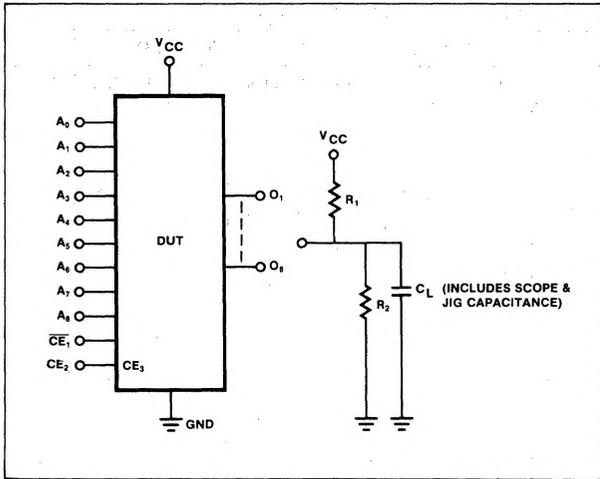
NOTES

- Positive current is defined as into the terminal referenced.
- Typical values are at V_{CC} = 5.0V, T_A = +25°C.

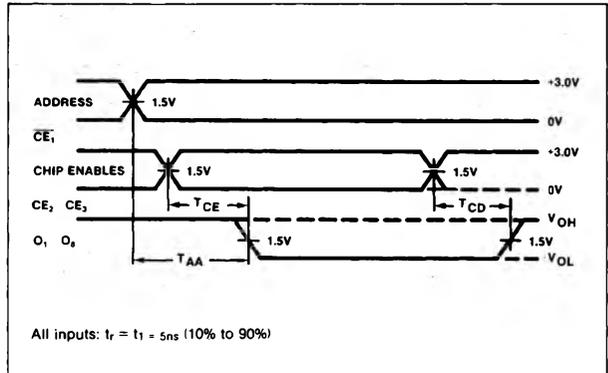
OBJECTIVE SPECIFICATION

82S190-I • 82S191-I

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT			
		Min	Typ	Max				
V_{CCP}	Power supply voltage To program ¹	8.5	8.75	9.0	V			
V_{CCH}	Verify limit Upper	5.3	5.5	5.7	V			
V_{CCL}	Lower	4.3	4.5	4.7	V			
V_S	Verify threshold ²	1.4	1.5	1.6	V			
I_{CCP}	Programming supply current	$V_{CCP} = +8.75 \pm .25V$			300	450	mA	
V_{IH}	Input voltage High	2.4		5.5		V		
V_{IL}	Low	0	0.4	0.8		V		
I_{IH}	Input current High	$V_{IH} = +5.5V$				50	μA	
I_{IL}	Low	$V_{IL} = +0.4V$				-500		
V_{OUT}	Output programming voltage ³	$I_{OUT} = 200 \pm 20mA$, Transient or steady state			16.0	17.0	18.0	V
I_{OUT}	Output programming current	$V_{OUT} = +17 \pm 1V$			180	200	220	mA
T_R	Output pulse rise time				10		50	μs
t_p	CE programming pulse width				0.3	0.4	0.5	ms
t_D	Pulse sequence delay				10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$					12	sec
T_{PSI}	Initial programming pause	$V_{CC} = 0V$			6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle ⁴						50	%
F_L	Fusing attempts per link						2	cycle

NOTES

1. Bypass V_{CC} to GND with a $0.01\mu F$ capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1V$ output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

OBJECTIVE SPECIFICATION

82S190-I • 82S191-I

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1 = \text{High}$, $CE_2 = \text{High}$ and $CE_3 = \text{High}$.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the \overline{CE}_1 input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the \overline{CE}_1 input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE

