8355
16,384 BIT ROM WITH I/O

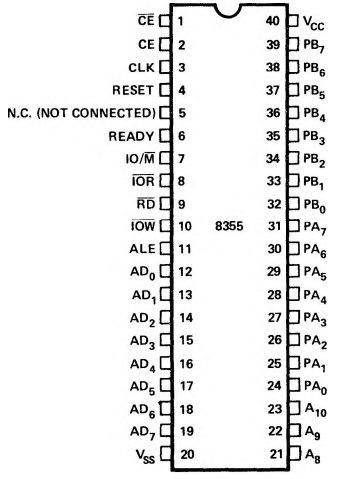
*Directly Compatible With 8085 CPU

- **2048 Words x 8 Bits**
- **Single +5V Power Supply**
- **Internal Address Latch**
- **2 General Purpose 8 Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40 Pin DIP**

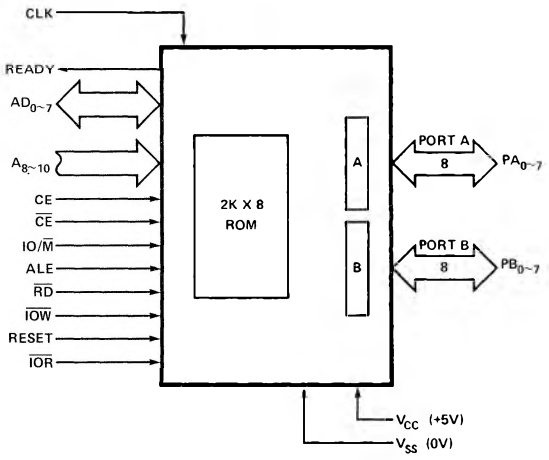
The 8355 is a ROM and I/O chip to be used in the MCS-85™ microcomputer system. The ROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



8355 FUNCTIONAL PIN DEFINITION

Symbol	Function
ALE	When ALE (Address Latch Enable) is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter address latched. The signals (AD, IO/$\overline{M}$, A_{8-10}, CE, $\overline{CE}$) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the ROM address. They do not affect I/O operations.
$\overline{CE}$ CE	Chip Enable Inputs: $\overline{CE}$ is active low and CE is active high. The 8355 can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state.
IO/$\overline{M}$	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.

Symbol	Function
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high and ALE high.
READY	Ready is a tri-state output controlled by $\overline{CE}$, CE, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 4).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by $\overline{IOR}$ low when the Chip is enabled and AD_0 low. Alternately, IO/$\overline{M}$ high and $\overline{RD}$ low may be used in place of $\overline{IOR}$ when the chip is enabled and AD_0 is low to allow reading from a port.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	An input high on RESET causes all pins in Ports A and B to assume input mode.
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination IO/$\overline{M}$ high and $\overline{RD}$ low.
V_{CC}	+5 volt supply.
V_{SS}	0 volt supply.

FUNCTIONAL DESCRIPTION

ROM Section

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out through AD_{0-7} output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers in 8355 determine the input/output status of each pin in the corresponding ports. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. *DDR's cannot be read.*

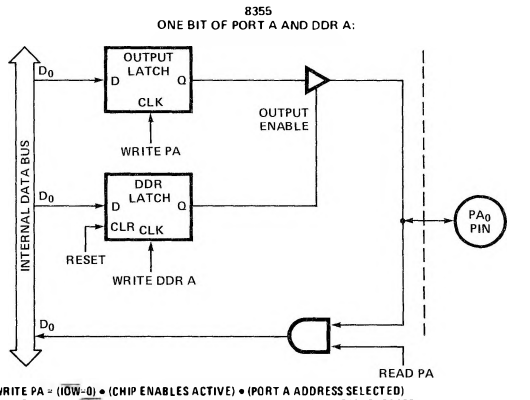
AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1}.

During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.



Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

System Interface with 8085

A system using the 8355 can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE and $\overline{CE}$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085 system can use up to 5 each 8355's without requiring a CE decoder. See Figure 1.

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the AD_{8-15} address lines. See Figure 2.

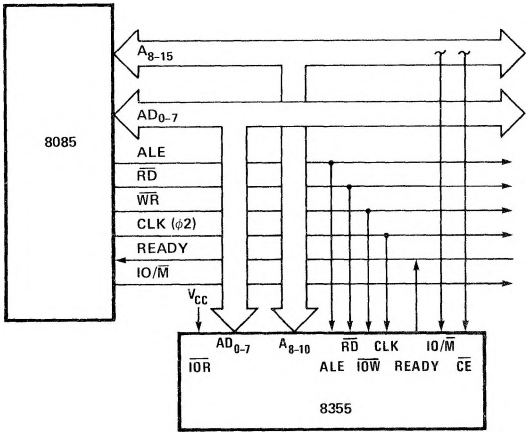
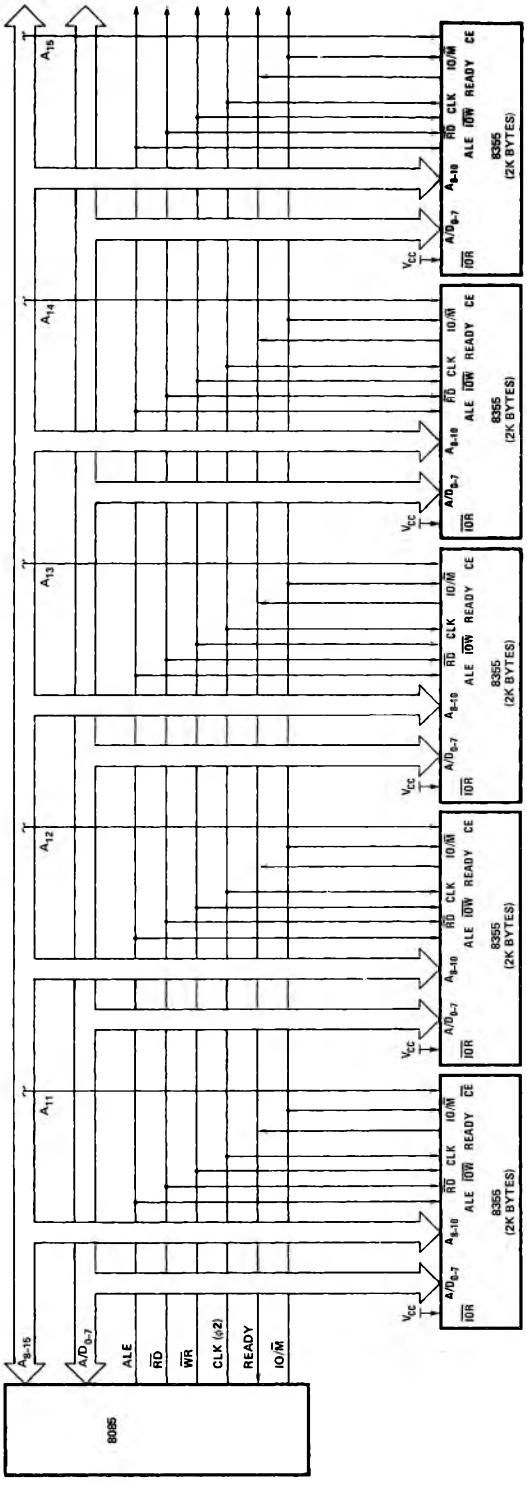


FIGURE 2. 8355 IN 8085 SYSTEM (MEMORY-MAPPED I/O).



Note: Use $\overline{CE}$ for the first 8355 in the system, and CE for the other 8355's. Permits up to 5 ea. 8355's in a system without CE decoder.

FIGURE 1. 8355 IN 8085 SYSTEM (STANDARD I/O).

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.3V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	C_{LOAD} = 150 pF (See Figure 3)
T_1	CLK Pulse Width	80		ns	
T_2	CLK Pulse Width	120		ns	
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	150 pF Load
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	120	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

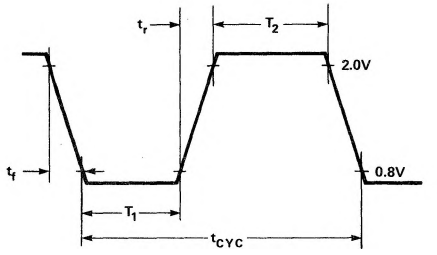


FIGURE 4. CLOCK SPECIFICATION FOR 8355.

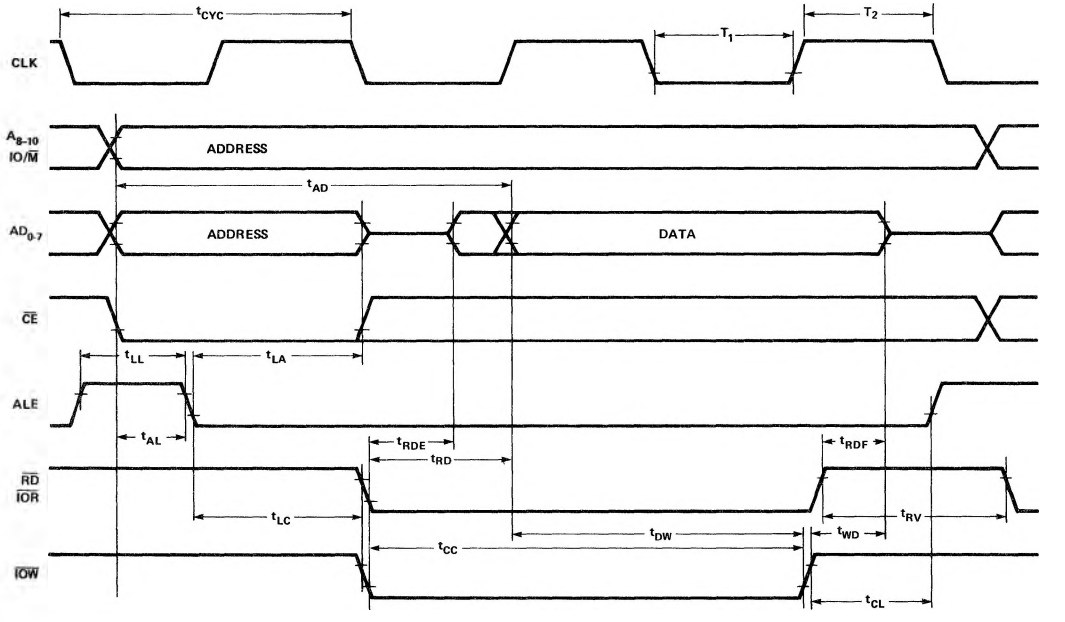


FIGURE 5. ROM READ AND I/O READ AND WRITE.

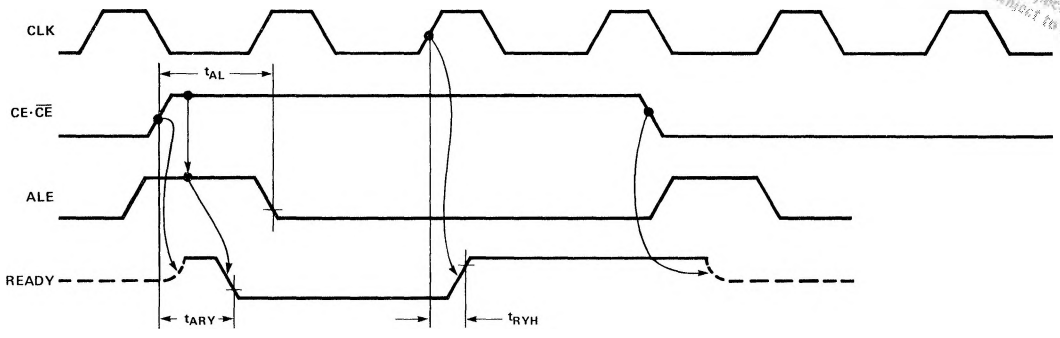


FIGURE 6. WAIT STATE TIMING (READY = 0).

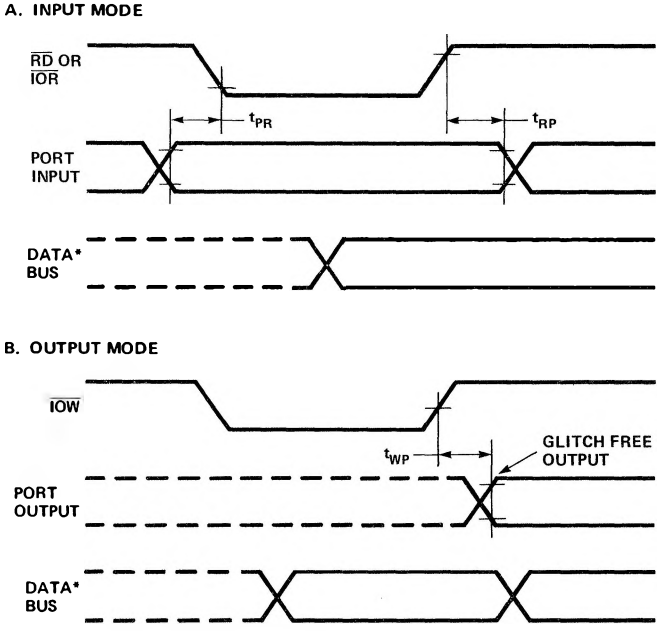


FIGURE 7. I/O PORT TIMING.