FIFO RAM CONTROLLER (FRC) 8X60

DESIGN FEATURES

- **12-Bit FIFO Address Generator**
- **Data Rate Exceeding 8MHz**
- **Asynchronous Read/Write Operations**
- **Three-State Address Outputs**
- **User-Defined Word Width**
- **Specifically Designed for Use with High-Speed Bipolar RAMs (Adaptable for Use with MOS RAMs)**
- **TTL Input and Output**
- **16mA Address-Drive Capability**

USE AND APPLICATION

- **Interface Between Independently-Clocked Systems**
- **Buffer Memories for Disk and/or Tape**
- **Data Communication Concentrators**
- **CPU/Terminal Buffering**
- **DMA Applications**
- **CRT Terminals**

PRODUCT DESCRIPTION

The Signetics 8X60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs—see **APPLICATIONS** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected—refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-served basis.

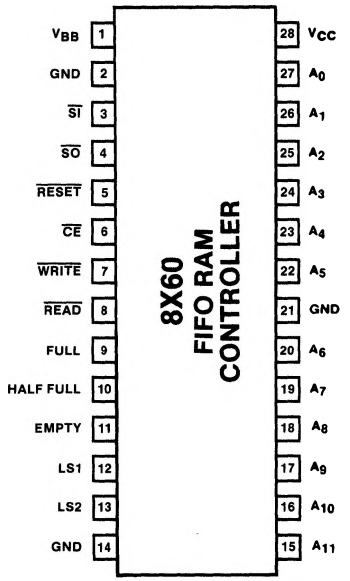
As shown in Figure 1, the FRC consists of:

- A 12-Bit Write Address Generation Counter (Counter #1) and a 12-Bit Read Address Generation Counter (Counter #2).
- A 12-Bit Up/Down Status Counter (Counter #3).
- Twelve Three-State Address Drivers.
- Control Logic.

The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the three-state address drivers. Counter #3 generates *full, empty,* and *half full* status.

PACKAGE AND PIN DESIGNATIONS

N, FQ PACKAGE



TOP VIEW

ORDER NUMBERS

N8X60N, RB8X60F

PIN NO.	IDENTIFIER	FUNCTION
1	V_{BB}	Supply voltage for internal circuits.
2, 14, 21	GND	Circuit ground.
3	$\overline{SI}$	Shift-In request for write cycle; active-low input
4	$\overline{SO}$	Shift-Out request for read cycle; active-low input.
5	$\overline{RESET}$	Active-low master reset input.
6	$\overline{CE}$	Active-low chip enable input
7	$\overline{WRITE}$	Write cycle address valid; active-low output
8	$\overline{READ}$	Read cycle address valid, active-low output
9	FULL	Memory full status output, also, override input capability. Active when *high*.
10	HALF FULL	Memory half-full status output, active-high
11	EMPTY	Memory empty status output; also, override input capability. Active when *high*
12	LS1	Least significant bit (LSB) of the memory length select input
13	LS2	Most significant bit (MSB) of the memory length select input
15-20 22-27	A_{11}-A_0	Three-state address outputs, A_0 = LSB
28	V_{CC}	Supply voltage.

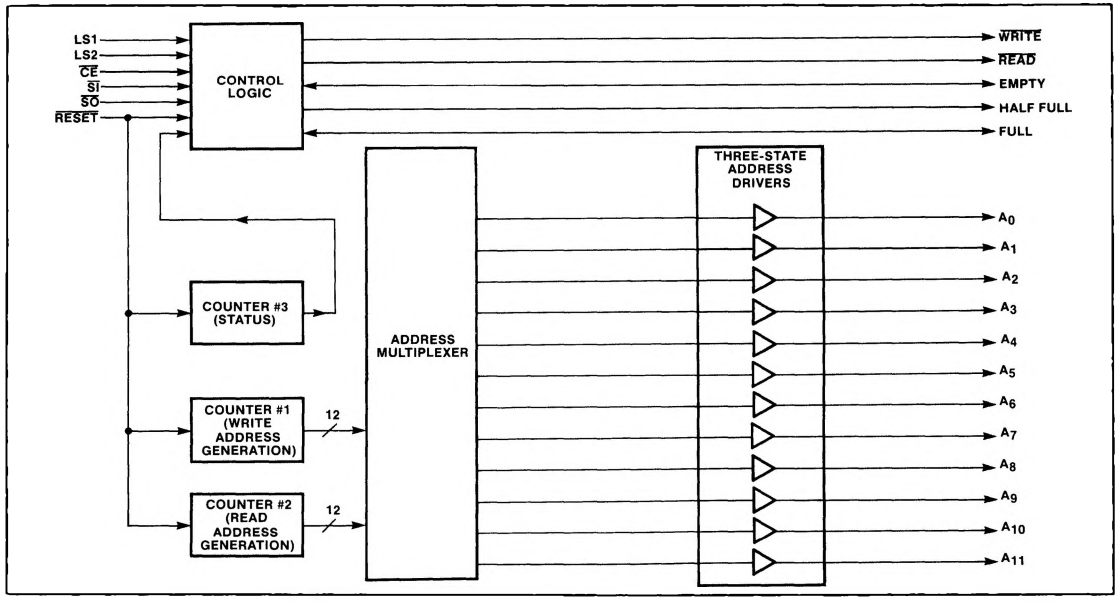


Figure 1. Functional Block Diagram of FIFO RAM Controller

FUNCTIONAL OPERATION

The FRC operates in either of two basic modes—*write* into the FIFO buffer memory or *read* from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the **Timing Diagrams.**

FIFO BUFFER MEMORY—WRITE CYCLE

To perform a write operation, $\overline{SO}$ must be *high* and SI must be *low*. When these conditions exist and other control parameters (Table 1) are satisfied, the write address in Counter #1 (Figure 1) is output to the address bus via the multiplexer and $\overline{WRITE}$ output goes *low*. (*Note.* Normally, the $\overline{WRITE}$ output goes *low* after the address output becomes stable—refer to *WRITE CYCLE TIMING DIAGRAM*. The $\overline{WRITE}$ output may then act as a *write* or *chip* enable for the RAMs that are used to implement the memory.)

When the *write* cycle is ended ($\overline{SI}$ is forced high), the $\overline{WRITE}$ output goes *high*, the address output buffers return to a high-impedance state, Counter #1 (Write Address Generation) and Counter #3 (Status) are both incremented, and Counter #2 (Read Address Generation) remains unchanged.

FIFO BUFFER MEMORY—READ CYCLE

To perform a read operation, $\overline{SI}$ must be *high* and $\overline{SO}$ must be *low*. When these conditions exist and other control parameters (Table 1) are satisfied, the read address contained in Counter #2 (Figure 1) is output to the address bus and the $\overline{READ}$ output goes *low*.

When the *read* cycle is ended ($\overline{SO}$ is forced *high*), the $\overline{READ}$ output goes *high*, the output buffers return to a high-impedance state, Counter #2 (Read Address Generation) is incremented, Counter #3 (Status) is decremented, and Counter #1 (Write Address Generation) remains unchanged.

CONTROL LOGIC

To prevent the possibility of operational conflicts. $\overline{SI}$ and $\overline{SO}$ are treated on a first-come/first-served basis; these two input signals are controlled by internal arbitration logic—refer to the applicable **TIMING DIAGRAMS** and **AC CHARACTERISTICS** for functional and timing relationships. If one cycle is requested while the other cycle is in progress, the requested cycle will commence as soon as the current-cycle is complete (provided other control parameters are satisfied).

As shown in the accompanying diagram, the buffer length of the FIFO memory can be hardware-selected via the Length Select (LS1, LS2) inputs. When less than the maximum length is selected, the unused high-order bits of the address outputs are held in the high-impedance state.

MEMORY LENGTH

LS1	LS2	HALF LENGTH	FULL LENGTH
L	L	2048	4096
H	L	32	64
L	H	512	1024
H	H	128	256

Generation of the status output signals (HALF FULL, FULL and EMPTY) is a function of the Length Select (LS1, LS2) inputs and the current state of Status Counter #3. In general, the status outputs reflect the conditions that follow:

- **HALF FULL**—this status output signals goes *high* on the positive-going edge of $\overline{SI}$ if the MSB of the selected length of Counter #3 becomes a "1". The HALF FULL signal will go from *high-to-low* on the positive-going edge of $\overline{SO}$ when, after the *read* cycle, the selected length of Counter #3 changes from "100 . . 00" to "011 . . 11". For example, if the selected memory length is 256 words (FULL = 256), then HALF FULL = 128 words; hence, on the

positive-going edge of $\overline{SO}$ when Counter #3 reaches a count of 127, the HALF FULL output will go from *high-to-low*

- **FULL**—this signal serves both as a status output and as an override input The FULL signal goes *high* on the negative-going edge of $\overline{SI}$ if all bits of Counter #3 for selected length are equal to "1" The FULL output goes from *high*-to-*low* on the negative-going edge of $\overline{SO}$
- **EMPTY**—this signal also serves as a status output and as an override input On the negative-going edge of $\overline{SO}$, the EMPTY output is driven *high* if Status Counter #3 contains a value of "1", on the positive-going edge of $\overline{SO}$, the counter is decremented to "0" The EMPTY output goes from *high*-to-*low* on the negative-going edge of $\overline{SI}$

Once the FULL signal is *high*, further Write Cycle Requests ($\overline{SI}$ = low) are ignored; similarly, once the EMPTY signal is *high*, further Read Cycle requests ($\overline{SO}$ = low) are ignored. However, to accommodate diversified applications, the FULL and EMPTY outputs are open-collector with on-chip 4 7K passive pull-up resistors If either the FULL or EMPTY pins are forced *low* via external control, the corresponding *write* or *read* cycle may resume (provided the external FULL or EMPTY input is held *low* until the corresponding $\overline{WRITE}$ or $\overline{READ}$ output goes *low*) and the address/status counters will continue normal operation*—refer to Table 1

The user must force the $\overline{RESET}$ input *low* to initialize the chip (*Note.* If the $\overline{RESET}$ signal is driven *low* during a *write* or *read* cycle, the address output may have a short period of uncertainty before assuming a high-impedance state) The following actions occur when $\overline{RESET}$ is active

- All internal counters are set to "0"
- All address output lines are forced to the high-impedance state
- HALF FULL and FULL outputs are forced *low*
- $\overline{WRITE}$, $\overline{READ}$, and EMPTY outputs are forced high

When $\overline{CE}$ is *high*, the address output lines are forced to the high-impedance state, further *write* or *read* cycle requests are ignored, and all counters remain unchanged If $\overline{CE}$ switches from *low*-to-*high* during a *write* or *read* cycle, the cycle in progress is always completed before the disabled state is entered For details of these operations, refer to the timing information shown later in this data sheet

*Refer to **Note** on inside back cover

Table 1. Summary of Operation

INPUTS				INITIAL	RESULTING OUTPUTS			COMMENTS
$\overline{RESET}$	$\overline{CE}$	$\overline{SI}$	$\overline{SO}$	CONDITIONS	$\overline{WRITE}$	$\overline{READ}$	ADDRESS BUS	
L	X	X	X		H	H	Hi-Z	Reset all counters to 0
H	X	H	H		H	H	Hi-Z	No action
H	L	L	H	FULL = L	L	H	Write address from Ctr #1	Shift into FIFO stack (Write Cycle)
H	L	L	H	FULL = H	H	H	Hi-Z	Stack full (Write inhibited)
H	L	H	L	EMPTY = L	H	L	Read address from Ctr #2	Shift out of FIFO stack (Read Cycle)
H	L	H	L	EMPTY = H	H	H	Hi-Z	Stack empty (Read inhibited)
H	L	L	↓	Write cycle in progress	L	H	Write address from Ctr #1	Continue write cycle (until $\overline{SI}$ goes high)
H	L	↓	L	Read cycle in progress	H	L	Read address from Ctr #2	Continue read cycle (until $\overline{SO}$ goes high)
H	L	L	L	EMPTY = H	L	H	Write address from Ctr #1	Shift in (Read inhibited)
H	L	L	L	FULL = H	H	L	Read address from Ctr #2	Shift out (Write inhibited)
H	L	↑	H	Write cycle in progress	↑	H	Goes to Hi-Z	Increment write address counter #1 and status counter #3
H	L	H	↑	Read cycle in progress	H	↑	Goes to Hi-Z	Increment read address counter #2, decrement status counter #3
H	L	↑	L	Write cycle in progress (Note 1)	↑	↓	Changes to read address from Ctr #2	Increment write address counter #1 and status counter #3
H	L	L	↑	Read cycle in progress (Note 2)	↓	↑	Changes to write address from Ctr #1	Increment read address counter #2, decrement status counter #3
H	H	↓	H		H	H	Hi-Z	Chip disabled
H	H	H	↓		H	H	Hi-Z	Chip disabled
H	↑	L	X	FULL = L, write cycle begun (Note 1)	L	H	Write address from Ctr #1	Continue write cycle (until $\overline{SI}$ goes high)
H	↑	X	L	EMPTY = L, read cycle begun (Note 2)	H	L	Read address from Ctr #2	Continue read cycle (until $\overline{SO}$ goes high)
H	↓	L	L	FULL = L, EMPTY = L	—	—	—	This set of conditions should be avoided

NOTES

1 Write cycle will occur if either $\overline{SI}$ goes *low* before $\overline{SO}$ goes *low* or EMPTY = H when $\overline{SO}$ goes *low*

2 Read cycle will occur if either $\overline{SO}$ goes *low* before $\overline{SI}$ goes *low* or FULL = H when $\overline{SI}$ goes *low*.

FIFO RAM CONTROLLER (FRC) 8X60

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{BB}	Supply Voltage for Internal Circuits	+4	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_{STG}	Storage Temperature Range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

CONDITIONS: Commercial— $V_{CC} = 5.0V (\pm 5\%)$, $V_{BB} = 1.5V (\pm 5\%)$[1], $0°C \le T_A \le 70°C$
Military— $V_{CC} = 5.0V (\pm 10\%)$, $V_{BB} = 1.5V (\pm 10\%)$[1], $T_A \le -55°C$, $T_C \le 125°C$

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	TYP[2]	MAX	LIMITS (MILITARY) MIN	TYP[2]	MAX	UNITS
V_{IH}	High level input voltage	Note 3	2.0			2.0			V
V_{IL}	Low level input voltage				0.8			0.8	V
V_{OH}	High level output voltage: All outputs except FULL and EMPTY	V_{CC} = Min; I_{OH} = −2.6mA	2.7	3.5		2.5	3.5		V
V_{OL}	Low level output voltage: Address Bus, $\overline{WRITE}$, $\overline{READ}$	V_{CC} = Min, I_{OL} = 16mA		0.38	0.5		0.38	0.5	V
	HALF FULL, FULL, and EMPTY	V_{CC} = Min; I_{OL} = 8mA		0.35	0.5		0.35	0.5	V
V_{CD}	Diode clamp voltage: All inputs except FULL and EMPTY	V_{CC} = Min; I_{CD} = −18mA	−1.5	−0.8		−1.5	−0.8		V
I_{IH}	High level input current: All inptus except FULL and EMPTY	V_{CC} = Max; V_{IH} = 2.7V		0.1	20		0.1	20	μA
	FULL and EMPTY	V_{CC} = Max; V_{IH} = 2.7V; Stack FULL or Stack EMPTY (Note 3)		−470	−750		−470	−900	μA
I_{IL}	Low level input current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IL} = 0.4V		−0.17	−0.4		−0.17	−0.4	mA
	FULL and EMPTY	V_{CC} = Max; V_{IL} = 0.4V; Stack FULL or Stack EMPTY		−1.12	−1.8		−1.12	−1.8	mA
I_{OH}	High level output current: FULL, EMPTY	V_{CC} = Min, V_{OH} = V_{CC} (min)		15	100		15	100	μA
I_{OZH}	High-Z output current (HIGH); Address Bus (Three-State)	V_{CC} = Max; V_{OUT} = 2.4V		0.9	20		0.9	20	μA
I_{OZL}	High-Z output current (LOW); Address Bus (Three-State)	V_{CC} = Max; V_{OUT} = 0.5V		−0.6	−20		−0.6	−20	μA
I_I	Input leakage current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IN} = 5.5V		0.03	0.1		0.03	0.1	mA
I_{OS}	Short-circuit output current: Address Bus and HALF FULL	V_{CC} = Max; V_{OH} = 0V	−15	−68	−100	−15	−68	−100	mA
	$\overline{WRITE}$, $\overline{READ}$	V_{CC} = Max; V_{OH} = 0V	−40	−73	−100	−40	−73	−100	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = Max; Address Bus = High-Z, 0°C →		81	140	−55°C →		140	mA
		70°C →		81	110	125°C →		100	
I_{BB}	Supply current from V_{BB}	V_{BB} = Max, 0°C →		63	95	−55°C	63	100	mA
		70°C →		63	85	125°C	63	90	

NOTES
1. V_{BB} can be obtained from a regulated 1.5V supply, alternately, proper supply current (I_{BB}) can be obtained by connecting a 56-ohm (±5%, 0.5W) resistor in series with V_{CC} as shown later in the **APPLICATIONS** diagram
2. Typical limits are. V_{CC} = 5.0V, T_A = 25°C
3. Because of the internal pull-up resistor on the FULL and EMPTY pins, a negative current is required to force the required voltage
4. V_{OL} at I_{OL} = 4mA for Military part

CONDITIONS: Commercial— V_{CC} = 5.0V (±5%), V_{BB} = 1.5V (±5%), 0°C ≤ T_A ≤ 70°C; Military— V_{CC} = 5.0V (±10%), V_{BB} = 1.5V (±10%), T_A ≤ −55°C, T_C ≤ 125°C; Loading— See TEST LOADING CIRCUITS

AC ELECTRICAL CHARACTERISTICS

PARAMETERS	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (Commercial) Min	Typ	Max	LIMITS (Military) Min	Typ	Max	UNITS
PULSE WIDTHS										
T_{LH} $\overline{SI}$ high	↑$\overline{SI}$	↓$\overline{SI}$	Stack approaching FULL (Note 1)	25	13		25	13		ns
T_{DH} $\overline{SO}$ high	↑$\overline{SO}$	↓$\overline{SO}$	Stack approaching EMPTY (Note 1)	30	16		30	16		ns
WRITE CYCLE TIMING										
T_{LA} Address stable delay	↓$\overline{SI}$	An	FULL = Low; $\overline{SO}$ = High		40	55		40	60	ns
T_{AW} Address lead time	An	↓$\overline{WRITE}$		3			0			ns
T_{LAW} $\overline{WRITE}$ output active delay	↓$\overline{SI}$	↓$\overline{WRITE}$	FULL = Low; $\overline{SO}$ = High	35	51	65	35	51	70	ns
T_{LW} $\overline{WRITE}$ output inactive dalay	↑$\overline{SI}$	↑$\overline{WRITE}$			3	10		3	10	ns
T_{WA} Address lag time	↑$\overline{WRITE}$	An		20	34		10	34		ns
T_{LT} Address output disable	↑$\overline{SI}$	An(Hi-Z)			37	60		37	60	ns
T_{LF} FULL status active delay	↓$\overline{SI}$	↑FULL	Stack approaching FULL; $\overline{SO}$ = High		39	65		39	70	ns
T_{LE} EMPTY status inactive delay	↓$\overline{SI}$	↓EMPTY	Stack = EMPTY		40	65		40	65	ns
T_{HFH} HALF-FULL status active delay	↑$\overline{SI}$	↑HALF FULL	Stack approaching HALF-FULL		30	45		30	50	ns
T_{DW} $\overline{WRITE}$ output active after read	↑$\overline{SO}$	↓$\overline{WRITE}$	Both $\overline{SI}$ & $\overline{READ}$ = Low		74	95		74	100	ns
READ CYCLE TIMING										
T_{DA} Address stable delay	↓$\overline{SO}$	An	EMPTY = Low; $\overline{SI}$ = High		40	55		40	60	ns
T_{AR} Address lead time	An	↓READ		−1			−5			ns
T_{DAR} $\overline{READ}$ output active delay	↓$\overline{SO}$	↓READ	EMPTY = Low; $\overline{SI}$ = High	30	48	65		35	70	ns
T_{DR} $\overline{READ}$ output inactive delay	↑$\overline{SO}$	↑$\overline{READ}$			5	10		5	10	ns
T_{RA} Address lag time	↑$\overline{READ}$	An		20	32		10	32		ns
T_{DT} Address output disable	↑$\overline{SO}$	An (Hi-Z)			37	60		37	60	ns
T_{DE} EMPTY status active delay	↓$\overline{SO}$	↑EMPTY	Stack approaching EMPTY; $\overline{SI}$ = High		38	50		38	50	ns
T_{DF} FULL status inactive delay	↓$\overline{SO}$	↓FULL	Stack = FULL		38	50		38	65	ns
T_{HFL} HALF-FULL status inactive delay	↑$\overline{SO}$	↓HALF FULL	Stack exactly HALF-FULL		54	75		54	85	ns
T_{LR} $\overline{READ}$ output active after wirte	↑$\overline{SI}$	↓$\overline{READ}$	Both $\overline{SO}$ & $\overline{WRITE}$ = Low		70	90		70	100	ns
CHIP ENABLE TIMING (WIRTE)										
T_{HEW} Chip enable hold time[2]	↓$\overline{SI}$	↑$\overline{CE}$	FULL = Low; $\overline{SO}$ = High	10	1		10	1		ns
T_{SEW} Chip disable setup time[3]	↑$\overline{CE}$	↓$\overline{SI}$	FULL = Low; $\overline{SO}$ = High	10	1		10	1		ns
T_{PEW} Chip enable delay time	↓$\overline{CE}$	↓$\overline{WRITE}$	FULL = Low; $\overline{SI}$ = Low; $\overline{SO}$ = High		69	95		69	110	ns
CHIP ENABLE TIMING (READ)										
T_{HER} Chip enable hold time[2]	↓$\overline{SO}$	↑$\overline{CE}$	EMPTY = Low; $\overline{SI}$ = High	10	1		10	1		ns
T_{SER} Chip disable setup time[3]	↑$\overline{CE}$	↓$\overline{SO}$	EMPTY = Low, $\overline{SI}$ = High	10	1		10	1		ns
T_{PER} Chip enable delay time	↓$\overline{CE}$	↓$\overline{READ}$	EMPTY = Low; $\overline{SO}$ = Low; $\overline{SI}$ = High		64	95		64	105	ns
RESET TIMING										
T_{RR} $\overline{RESET}$ recovery	↑$\overline{RESET}$	↓$\overline{WRITE}$	$\overline{SI}$ = Low		57	75		57	80	ns
T_{RL} $\overline{RESET}$ pulse width (low)	↓$\overline{RESET}$	↑$\overline{RESET}$		25	8		25	8		ns
FULL/EMPTY OVERRIDE TIMMING:										
T_{FW} Override Recovery for FULL	↓FULL	↓$\overline{WRITE}$	Stack = Full; $\overline{SI}$ = Low; $\overline{SO}$ = High		70	95		70	110	ns
T_{ER} Override Recovery for EMPTY	↓EMPTY	↓$\overline{READ}$	Stack = EMPTY; $\overline{SO}$ = Low; $\overline{SI}$ = High		65	90		65	105	ns

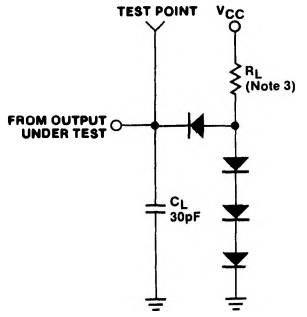
NOTES 1 Such that write/read request is inhibited after stack becomes full/empty

2 The earliest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output always occurs

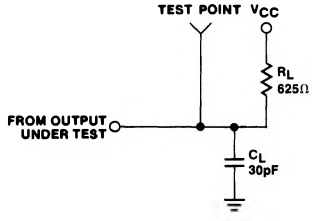
3 The latest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output never occurs

TEST LOADING CIRCUITS

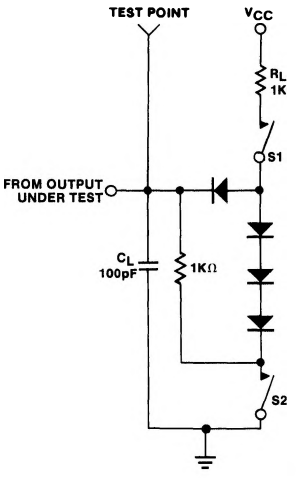
APPLICABLE PINS: $\overline{WRITE}$ (7), $\overline{READ}$ (8), HALF FULL (10)



APPLICABLE PINS: FULL (9) AND EMPTY (11)



APPLICABLE PINS: A_n (15-20, 22-27)

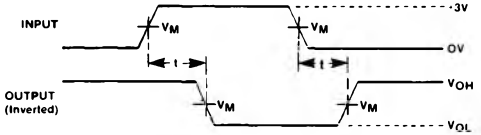


OUTPUT STATE		SWITCH POSITION	
FROM	TO	S1	S2
Low	High	Closed	Closed
High	Low	Closed	Closed
High	HI-Z	Closed	Closed
Low	HI-Z	Closed	Closed
HI-Z	High	Open	Closed
HI-Z	Low	Closed	Open

NOTES
1. In all cases C_L includes probe and jig capacitance
2. All diodes are 1N916, 1N3064, or equivalent
3. For $\overline{READ}$ and $\overline{WRITE}$ outputs, R_L = 280 ohms, for HALF FULL output, R_L = 2K ohms

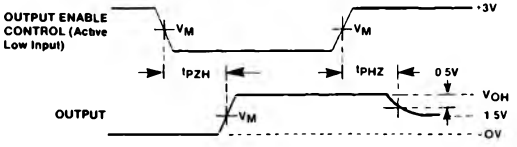
AC TEST WAVEFORMS

PROPAGATION DELAY
(Typical Example)

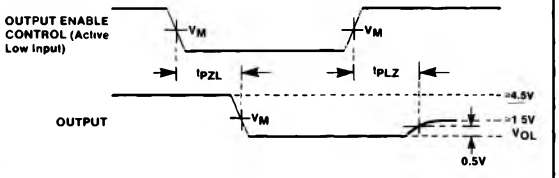


Note
Pulse widths and Setup/Hold times are measured using the same reference points as above waveform

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

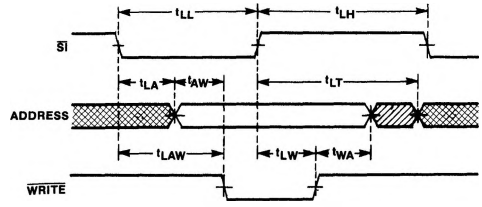


V_M = 1.5 V

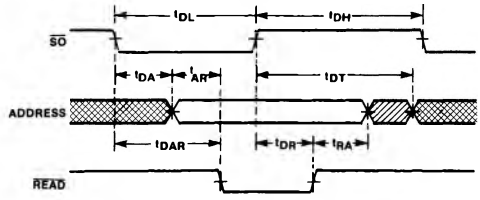
FIFO RAM CONTROLLER (FRC) 8X60

TIMING DIAGRAMS

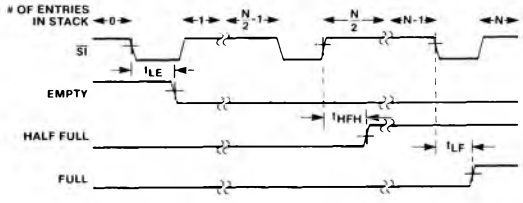
WRITE CYCLE TIMING



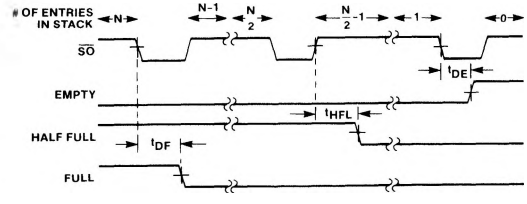
READ CYCLE TIMING



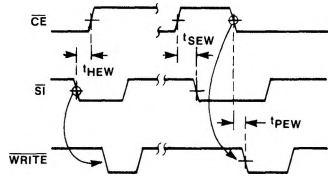
STATUS OUTPUT TIMING-WRITE



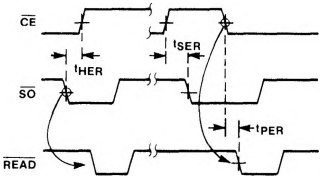
STATUS OUTPUT TIMING-READ



CHIP ENABLE TIMING WRITE*

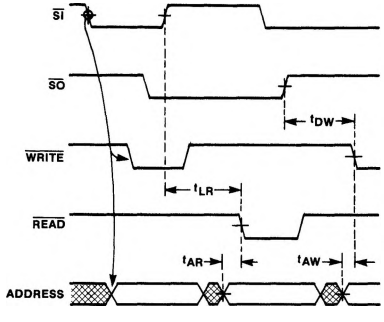


CHIP ENABLE TIMING READ*

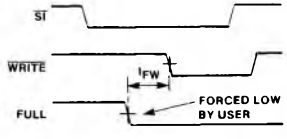


*The rising edge of $\overline{CE}$ should not occur within 10-nanoseconds before or after a falling edge of $\overline{SI}$ or $\overline{SO}$.

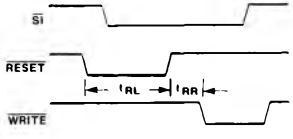
CHANGE OF CYCLE TIMING



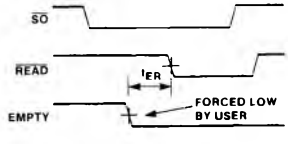
FULL OVERRIDE TIMING



RESET TIMING



EMPTY OVERRIDE TIMING



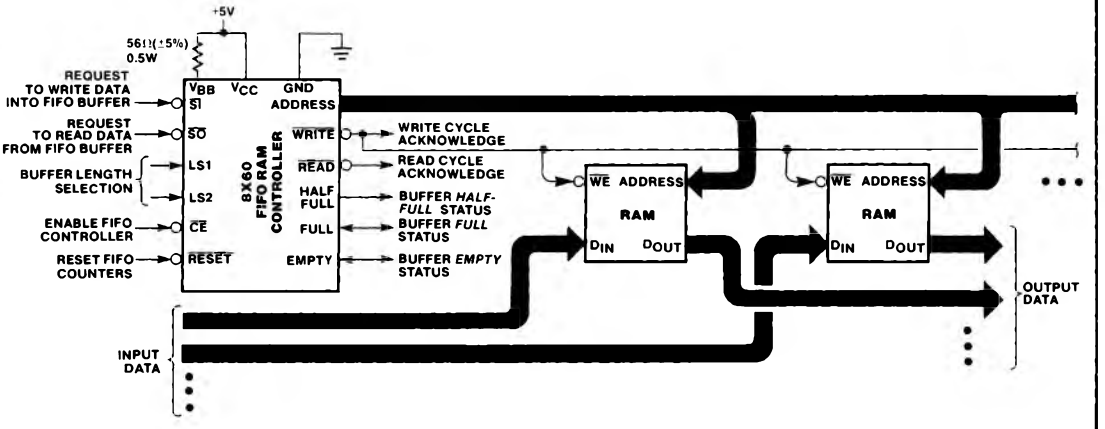
KEY

High-impedance state

Changing data

APPLICATIONS

IMPLEMENTATION OF A FIFO BUFFER USING THE 8X60 AND HIGH SPEED RAM



USING 8X60 WITH HIGH-DENSITY MOS RAMs