

January 1996

ACTS74MS

Radiation Hardened Dual D Flip Flop with Set and Reset

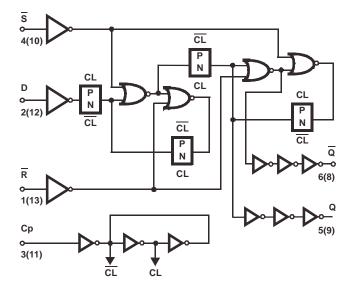
Pinouts Features Devices QML Qualified in Accordance with MIL-PRFF-38535 **14 PIN CERAMIC DUAL-IN-LINE** MIL-STD-1835 DESIGNATOR CDIP2-T14. · Detailed Electrical and Screening Requirements are Contained in LEAD FINISH C SMD# 5962-96713 and Intersil's QM Plan TOP VIEW 1.25 Micron Radiation Hardened SOS CMOS 14 VCC R1 1 13 R2 D1 2 Single Event Upset (SEU) Immunity: <1 x 10⁻¹⁰ Errors/Bit/Day CP1 3 12 D2 (Typ) 11 CP2 S1 4 10 S2 Q1 5 9 Q2 Q1 6 8 Q2 GND 7 • Latch-Up Free Under Any Conditions Military Temperature Range-55°C to +125°C • Significant Power Reduction Compared to ALSTTL Logic **14 PIN CERAMIC FLATPACK** MIL-STD-1835 DESIGNATOR CDFP3-F14, DC Operating Voltage Range 4.5V to 5.5V LEAD FINISH C Input Logic Levels TOP VIEW - VIL = 0.8V Max R1 🗖 _22 1 14 - VIH = VCC/2 Min 13 - R2 2 77 D1 E • Input Current ≤ 1µA at VOL, VOH 12 ____ D2 CP1 T ->7 3 <u>S1</u> г 77 4 11 ->>___ • Fast Propagation Delay..... 20ns (Max), 13ns (Typ) 32 S2 5 10 -77-77 Description Q1 Г 6 **_** Q2 22 77 9 __ Q2 GND r 7 8 77 27. The Intersil ACTS74MS is a Radiation Hardened Dual D Flip Flop with Set(s) and Reset (R). The logic level at data input is transferred to the output during the positive transition of the clock. The Set and Reset are independent from the clock and accomplished by a low level on the appropriate input. The ACTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic Family. The ACTS74MS is supplied in a 14 lead Ceramic Flatpack (K suffix) or a 14 Lead Ceramic Dual-In-Line Package (D suffix).

PART NUMBER TEMPERATURE RANGE		SCREENING LEVEL	PACKAGE	
5962F9671301VCC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead SBDIP	
5962F9671301VXC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead Ceramic Flatpack	
ACTS74D/Sample	25°C	Sample	14 Lead SBDIP	
ACTS74K/Sample	25°C	Sample	14 Lead Ceramic Flatpack	
ACTS74HMSR	25°C	Die	Die	

Ordering Information

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. 1-888-INTERSIL or 321-724-7143 | Intersil and Design is a trademark of Intersil Americas Inc. Copyright © Intersil Americas Inc. 2001, All Rights Reserved 1

Functional Diagram



TRUTH TABLE

	INP	OUTPUTS			
SET	RESET	СР	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	Х	Х	L	Н
L	L	Х	Х	H (Note 2)	H (Note 2)
Н	Н		Н	Н	L
Н	Н		L	L	Н
Н	Н	L	Х	Q0	Q0
H = High Level (Steady State) L = Low Level (Steady State)			X = Don't Care Transition from Low to High Level		

NOTES:

- 1. Q0 = the level of Q before the indicated input conditions were established.
- 2. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com

Die Characteristics

DIE DIMENSIONS:

88 mils x 88 mils 2240mm x 2240mm

METALLIZATION:

Type: AlSi Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO₂ Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY: <2.0 x 10⁵A/cm²

BOND PAD SIZE:

110μm x 110μm 4.3 mils x 4.3 mils

Metallization Mask Layout

