FEATURES

Dual 8-Bit ADCs on a Single Chip Low Power: $\mathbf{4 0 0}$ mW Typical On-Chip +2.5 V Reference and T/Hs<br>1 V p-p Analog Input Range<br>Single +5 V Supply Operation<br>+5 V or +3 V Logic Interface<br>120 MHz Analog Bandwidth<br>Power-Down Mode: < $\mathbf{1 2} \mathbf{~ m W}$<br>APPLICATIONS<br>Digital Communications (QAM Demodulators)<br>RGB \& YC/Composite Video Processing<br>Digital Data Storage Read Channels<br>Medical Imaging<br>Digital Instrumentation

## PRODUCT DESCRIPTION

The AD 9059 is a dual 8 -bit monolithic analog-to-digital converter optimized for low cost, low power, small size, and ease of use. With a 60 M SPS encode rate capability and full-power analog bandwidth of 120 M Hz typical, the component is ideal for applications requiring multiple ADCs with excellent dynamic performance.
To minimize system cost and power dissipation, the AD 9059 includes an internal +2.5 V reference and dual track-and-hold circuits. The ADC requires only a +5 V power supply and an encode clock. No external reference or driver components are required for many applications.
The AD 9059's single encode input is T TL/CM OS compatible and simultaneously controls both internal ADC channels. The parallel 8 -bit digital outputs can be operated from +5 V or +3 V supplies. A power-down function may be exercised to bring total consumption to $<12 \mathrm{~mW}$ when ADC data is not required for lengthy periods of time. In power-down mode the digital outputs are driven to a high impedance state.
Fabricated on an advanced BiCM OS process, the AD 9059 is available in a space saving 28 -lead surface mount plastic package ( 28 SSOP) and is specified over the industrial $\left(-40^{\circ} \mathrm{C}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ temperature range.
Customers desiring single channel digitization may consider the AD 9057, a single 8-bit, 60 M SPS monolithic based on the AD 9059 ADC core. The AD 9057 is available in a 20-lead surface mount plastic package (20 SSO P) and is specified over the industrial temperature range.

FUNCTIONAL BLOCK DIAGRAM


## PIN CONFIGURATION



## REV. 0

## AD9059- SPECIFICATIONS <br> ELECTRICAL CHARACTERIST|CS $\left(V_{D}=+5 \mathrm{~V}, \mathrm{~V}_{D D}=+3 \mathrm{~V}\right.$; external reference; ENCODE $=60 \mathrm{MSPS}$ unless otherwise noted)

|  |  |  | AD9059BRS |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Parameter | Temp | Test Level | Min | Typ | Max | Units


| Parameter | Temp | Test Level | AD9059BRS |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| DIGITAL INPUTS |  |  |  |  |  |  |
| Logic "1" Voltage | Full | VI | 2.0 |  |  | V |
| Logic "0" Voltage | Full | VI |  |  | 0.8 | V |
| Logic "1" Current | Full | VI |  |  | $\pm 1$ | $\mu \mathrm{A}$ |
| Logic " 0 " Current | Full | VI |  |  | $\pm 1$ | $\mu \mathrm{A}$ |
| Input Capacitance | $+25^{\circ} \mathrm{C}$ | V |  | 4.5 |  | pF |
| Encode Pulse Width High ( $\mathrm{E}_{\mathrm{H}}$ ) | $+25^{\circ} \mathrm{C}$ | IV | 6.7 |  | 166 | ns |
| Encode Pulse Width Low ( $\mathrm{teL}_{\text {L }}$ ) | $+25^{\circ} \mathrm{C}$ | IV | 6.7 |  | 166 | ns |
| DIGITAL OUTPUTS |  |  |  |  |  |  |
| Logic "1" Voltage ( $\mathrm{V}_{\text {DD }}=+3 \mathrm{~V}$ ) | Full | VI | 2.95 |  |  | V |
| Logic "1" Voltage ( $\mathrm{V}_{\mathrm{DD}}=+5 \mathrm{~V}$ ) | Full | IV | 4.95 |  |  | V |
| Logic " 0 " Voltage ( $\mathrm{V}_{\mathrm{DD}}=+3 \mathrm{~V}$ or +5 V ) Output C oding | Full | VI |  | Binar | $0.05$ | V |
| POWER SUPPLY |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{D}}$ Supply Current ( $\left.\mathrm{V}_{\mathrm{D}}=+5 \mathrm{~V}\right)$ | Full | VI |  | 72 | 92 | mA |
| $\mathrm{V}_{\text {DD }}$ Supply Current ( $\left.\mathrm{V}_{\mathrm{DD}}=+3 \mathrm{~V}\right)^{4}$ | Full | VI |  | 13 | 15 | mA |
| Power Dissipation ${ }^{5,6}$ | Full | VI |  | 400 | 505 | mW |
| Power-D own Dissipation | Full | VI |  | 6 | 12 | mW |
| Power Supply Rejection Ratio (PSRR) | $+25^{\circ} \mathrm{C}$ | I |  |  | 15 | mVN |

NOTES
${ }^{1} \mathrm{G}$ ain error and gain temperature coefficient are based on the ADC only (with a fixed +2.5 V external reference).
${ }^{2} t_{V}$ and $t_{P D}$ are measured from the 1.5 V level of the ENCODE to the $10 \% / 90 \%$ levels of the digital output swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of $\pm 40 \mu \mathrm{~A}$.
${ }^{3}$ SN R/harmonics based on an analog input voltage of -0.5 dBFS referenced to a 1.0 V full-scale input range.
${ }^{4}$ Digital supply current based on $V_{D D}=+3 \mathrm{~V}$ output drive with $<10 \mathrm{pF}$ loading under dynamic test conditions.
${ }^{5}$ Power dissipation is based on 60 M SPS encode and 10.3 M Hz analog input dynamic test conditions ( $\mathrm{V}_{\mathrm{D}}=+5 \mathrm{~V} \pm 5 \%, \mathrm{~V}_{\mathrm{DD}}=+3 \mathrm{~V} \pm 5 \%$ ).
${ }^{6} \mathrm{~T}$ ypical thermal impedance for the RS style (SSOP) 28 -pin package: $\theta_{\mathrm{J}} \mathrm{C}=39^{\circ} \mathrm{C} / \mathrm{W}, \theta_{\mathrm{CA}}=70^{\circ} \mathrm{C} / \mathrm{W}, \theta_{\mathrm{JA}}=109^{\circ} \mathrm{C} / \mathrm{W}$.
Specifications subject to change without notice.

## EXPLANATION OF TEST LEVELS Test Level

I - 100\% production tested.
II $-100 \%$ production tested at $+25^{\circ} \mathrm{C}$ and sample tested at specified temperatures.
III - Sample tested only.
IV - Parameter is guaranteed by design and characterization testing.
$V$ - Parameter is a typical value only.
VI - $100 \%$ production tested at $+25^{\circ} \mathrm{C}$; guaranteed by design and characterization testing for industrial temperature range.

## ABSOLUTE MAXIMUM RATINGS*


Analog Inputs .......................... . . -0.5 V to $\mathrm{V}_{\mathrm{D}}+0.5 \mathrm{~V}$
Digital Inputs . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to $\mathrm{V}_{\mathrm{D}}+0.5 \mathrm{~V}$
V ${ }_{\text {ReF }}$ Input . . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to $\mathrm{V}_{\mathrm{D}}+0.5 \mathrm{~V}$
Digital Output Current . . . . . . . . . . . . . . . . . . . . . . . . . 20 mA
Operating T emperature . . . . . . . . . . . . . . . . . $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage T emperature . . . . . . . . . . . . . . . . . . . $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

| Model | Temperature Range | Package Option |
| :--- | :--- | :--- |
| AD 9059BRS | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | RS-28 |
| AD 9059/PCB | $+25^{\circ} \mathrm{C}$ | E valuation B oard |

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD 9059 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



|  |  | MIN | TYP | MAX |
| :--- | :--- | :---: | :---: | :---: |
| $t_{\mathrm{A}}$ | APERTURE DELAY |  | 2.7 ns |  |
| $\mathrm{t}_{\text {EH }}$ | PULSE WIDTH HIGH | 6.7 ns |  | 166 ns |
| $\mathrm{t}_{\mathrm{EL}}$ | PULSE WIDTH LOW | 6.7 ns |  | 166 ns |
| $\mathrm{t}_{\mathrm{V}}$ | OUTPUT VALID TIME | 4.0 ns | 6.6 ns |  |
| $\mathrm{t}_{\text {PD }}$ | OUTPUT PROP DELAY |  | 9.5 ns | 14.2 ns |

Figure 1. Timing Diagram

## PIN CONFIGURATION

| AINA 1 | AD9059TOP VIEW(Not to Scale) | 28 AINB |
| :---: | :---: | :---: |
| vref 2 |  | 27 GND |
| PWRDN 3 |  | 26 encode |
| $\mathrm{v}_{\mathrm{D}} 4$ |  | 25 v |
| GND 5 |  | 24 GND |
| $v_{D D} 6$ |  | 23 VD |
| D7A (MSB) 7 |  | $22 \mathrm{D7B}$ (MSB) |
| D6A 8 |  | $21 \mathrm{D6B}$ |
| D5A 9 |  | 20 DFB |
| D4A 10 |  | 19 D4B |
| D3A 11 |  | 18 Dзв |
| D2A 12 |  | 17 D 2 B |
| D1A ${ }^{13}$ |  | $16 \mathrm{D1B}$ |
| DOA (LSB) 14 |  | 15 DOB (LSB) |

## PIN DESCRIPTIONS

| Pin No. | Name | Function |
| :---: | :---: | :---: |
| 1,28 | AINA, AINB | Analog Inputs for ADC A and B. |
| 2 | VREF | Internal Voltage Reference ( +2.5 V Typical); Bypass with $0.1 \mu \mathrm{~F}$ to Ground or Overdrive with External Voltage Reference. |
| 3 | PWRDN | Power-D own Function Select; Logic HIGH for Power-D own M ode (D igital Outputs Go to HighImpedance State). |
| 4, 25 | $V_{D}$ | Analog +5 V Power Supply. |
| 5, 24, 27 | GND | Ground. |
| 6, 23 | $V_{D D}$ | Digital Output Power Supply. N ominally +3 V to +5 V . |
| 7-14 | D 7A-D0A | Digital Outputs of ADCA. |
| 22-15 | D 7B-D 0B | Digital Outputs of ADCB. |
| 26 | ENCODE | Encode Clock for ADCs A and B (ADC s Sample Simultaneously On the Rising Edge of ENCODE). |

Table I. Digital Coding (VREF $=\mathbf{+ 2 . 5}$ V)

| Analog Input | Voltage Level | Digital Output |
| :--- | :--- | :--- |
| 3.0 V | Positive Full Scale | 11111111 |
| 2.502 V | M idscale $+1 / 2 \mathrm{LSB}$ | 10000000 |
| 2.498 V | M idscale - 1/2 L SB | 01111111 |
| 2.0 V | N egative Full Scale | 00000000 |



Figure 2. FFT Spectral Plot $60 \mathrm{MSPS}, 10.3 \mathrm{MHz}$


Figure 3. Spectral Plot $60 \mathrm{MSPS}, 76 \mathrm{MHz}$


Figure 4. SINAD/SNR vs. AIN Frequency


Figure 5. Harmonic Distortion vs. AIN Frequency


Figure 6. Two-Tone IMD


Figure 7. SINAD/SNR vs. Encode Rate


Figure 8. Power Dissipation vs. Encode Rate


Figure 9. SINAD/SNR vs. Temperature


Figure 10. ADC Gain vs. Temperature (With External +2.5 V Reference)


Figure 11. $t_{P D}$ vs. Temperature/Supply ( $+3 \mathrm{~V} /+5 \mathrm{~V}$ )


Figure 12. SINAD/SNR vs. Encode Pulse Width


Figure 13. ADC Frequency Response

## THEORY OF OPERATION

The AD 9059 combines A nalog D evices' proprietary M agAmp gray code conversion circuitry with flash converter technology to provide dual high performance 8 -bit ADC s in a single low cost monolithic device. The design architecture ensures low power, high speed, and 8-bit accuracy.
The AD 9059 provides two linked ADC channels that are clocked from a single EN CODE input (refer to block diagram). The two ADC channels simultaneously sample the analog inputs (AINA and AINB) and provide non-interleaved parallel digital outputs (D0A-D 7A and D OB-D 7B). The voltage reference (VREF) is internally connected to both ADC s so channel gains and offsets will track if external reference control is desired.
The analog input signal is buffered at the input of each ADC channel and applied to a high speed track-and-hold. The T/H circuit holds the analog input value during the conversion process (beginning with the rising edge of the ENCODE command). The T/H's output signal passes through the gray code and flash conversion stages to generate coarse and fine digital representations of the held analog input level. Decode logic combines the multistage data and aligns the 8-bit word for strobed outputs on the rising edge of the ENCODE command. The M agA mp/F lash architecture of the AD 9059 results in three pipeline delays for the output data.

## USING THE AD9059

## Analog Inputs

The AD 9059 provides independent single-ended high impedance ( $150 \mathrm{k} \Omega$ ) analog inputs for the dual ADCs. Each input requires a dc bias current of $6 \mu \mathrm{~A}$ (typical) centered near +2.5 V $( \pm 10 \%)$. The dc bias may be provided by the user or may be derived from the ADC's internal voltage reference. Figure 14 shows a low cost dc bias implementation allowing the user to capacitively couple ac signals directly into the ADC without additional active circuitry. For best dynamic performance the VREF pin should be decoupled to ground with a $0.1 \mu \mathrm{~F}$ capacitor (to minimize modulation of the reference voltage), and the bias resistor should approximately $1 \mathrm{k} \Omega$.

Figure 15 shows typical connections for high performance dc biasing using the ADC's internal voltage reference. All components may be powered from a single +5 V supply (example analog input signals are referenced to ground).

## Voltage Reference

A stable and accurate +2.5 V voltage reference is built into the AD 9059 (VREF). The reference output is used to set the ADC gain/offset and can provide dc bias for the analog input signals.
The internal reference is tied to the ADC circuitry through a $800 \Omega$ internal impedance and is capable of providing $300 \mu \mathrm{~A}$ external drive current (for dc biasing the analog input or other user circuitry).
Some applications may require greater accuracy, improved temperature performance, or gain adjustments which cannot be obtained using the internal reference. An external voltage may be
applied to the VREF pin to overdrive the internal voltage reference for gain adjustment of up to $\pm 10 \%$ (the VREF pin is internally tied directly to the ADC circuitry). ADC gain and offset will vary simultaneously with external reference adjustment with a $1: 1$ ratio (a $2 \%$ or 50 mV adjustment to the +2.5 V reference varies ADC gain by $2 \%$ and ADC offset by 50 mV ).
Theoretical input voltage range versus reference input voltage may be calculated from the following equations:

$$
\begin{aligned}
& V_{\text {RANGE }}(p-p)=V R E F / 2.5 \\
& V_{\text {MIDSCALE }}=V R E F \\
& V_{\text {TOP-OF-RANGE }}=V R E F+V_{\text {RANGE }} / 2 \\
& V_{\text {BOTTOM-OF-RANGE }}=V R E F-V_{\text {RANGE }} / 2
\end{aligned}
$$

The external reference should have a 1 mA minimum sink/ source current capability to ensure complete overdrive of the internal voltage reference.

## Digital Logic (+5 V/+3 V Systems)

The digital inputs and outputs of the AD 9059 can easily be configured to interface directly with +3 V or +5 V logic systems. The encode and power-down (PWRDN) inputs are CM OS stages with TTL thresholds of 1.5 V , making the inputs compatible with TTL, +5 V CM OS, and +3 V CM OS logic families. As with all high speed data converters, the encode signal should be clean and jitter free to prevent degradation of ADC dynamic performance.
The AD 9059's digital outputs will also interface directly with +5 V or +3 V CM OS logic systems. The voltage supply pins ( $\mathrm{V}_{\mathrm{DD}}$ ) for these CM OS stages are isolated from the analog $\mathrm{V}_{\mathrm{D}}$ voltage supply. By varying the voltage on these supply pins the digital output H IG H levels will change for +5 V or +3 V systems. The $\mathrm{V}_{\text {DD }}$ pins are internally connected on the AD 9059 die. $C$ are should be taken to isolate the $V_{D D}$ supply voltages from the +5 V analog supply to minimize noise coupling into the ADCs.
The AD 9059 provides high impedance digital output operation when the ADC is driven into power-down mode (PWRDN, logic HIGH). A 200 ns (minimum) power-down time should be provided before a high impedance characteristic is required. A 200 ns power-up period should be provided to ensure accurate ADC output data after reactivation (valid output data is available three clock cycles after the 200 ns delay).

## Timing

The AD 9059 is guaranteed to operate with conversion rates from 5 M SPS to 60 M SPS . At 60 M SPS the ADC is designed to operate with an encode duty cycle of $50 \%$, but performance is insensitive to moderate variations. Pulse width variations of up to $\pm 10 \%$ (allowing the encode signal to meet the minimum/ maximum HIGH/LOW specifications) will cause no degradation in ADC performance (refer to Figure 1 T iming Diagram).
D ue to the linked ENCODE architecture of the ADCs, the AD 9059 cannot be operated in a two-channel ping-pong mode.

## Power Dissipation

The power dissipation of the AD 9059 is specified to reflect a typical application setup under the following conditions: encode is 60 M SPS , analog input is -0.5 dBFS at $10.3 \mathrm{M} \mathrm{Hz}, \mathrm{V}_{\mathrm{D}}$ is $+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}$ is +3 V , and digital outputs are loaded with 7 pF typical ( 10 pF maximum). The actual dissipation will vary as these conditions are modified in user applications. Figure 8 shows typical power consumption for the AD 9059 versus ADC encode frequency and $V_{D D}$ supply voltage.


Figure 14. Capacitively Coupled AD9059
A power-down function allows users to reduce power dissipation when ADC data is not required. A TTL/CMOS HIGH signal (PWRDN ) shuts down portions of the dual ADC and brings total power dissipation to less than 10 mW . The internal bandgap voltage reference remains active during power-down mode to minimize ADC reactivation time. If the power-down function is not desired, Pin 3 should be tied to ground. Both ADC channels are controlled simultaneously by the PWRDN pin; they cannot be shut down or turned on independently.

## Applications

The wide analog bandwidth of the AD 9059 makes it attractive for a variety of high performance receiver and encoder applications. Figure 16 shows the dual ADC in a typical low cost I \& Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates empowers users to employ direct IF sampling techniques (refer to Figure 3, Spectral Plot). IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.


Figure 15. DC Coupled AD9059 (VIN Inverted)


Figure 16. I and Q Digital Receiver
The high sampling rate and analog bandwidth of the AD 9059 are ideal for computer RGB video digitizer applications. With a full-power analog bandwidth of $2 \times$ the maximum sampling rate, the ADC provides sufficient pixel-to-pixel transient settling time to ensure accurate 60 M SPS video digitization. Figure 17 shows a typical RGB video digitizer implementation for the AD 9059.


Figure 17. RGB Video Encoder



Digital Inputs


Digital Outputs


Analog Inputs

Figure 18. Equivalent Circuits

## Evaluation Board

The AD 9059/PCB evaluation board provides an easy-to-use analog/digital interface for the dual 8 -bit, 60 M SPS ADC. The board includes typical hardware configurations for a variety of high speed digitization evaluations. On-board components include the AD 9059 (in the 28-pin SSO P package), optional analog input buffer amplifiers, digital output latches, board timing drivers, and configurable jumpers for ac coupling, dc coupling, and power-down function testing. The board is configured at shipment for dc coupling using the AD 9059's internal reference.
For dc coupled analog input applications, amplifiers U3 and U 4 are configured to operate as unity gain inverters with adjustable offset for the analog input signals. F or full-scale ADC drive each analog input signal should be 1 V p-p into $50 \Omega$ referenced to ground. Each amplifier offsets its analog signal by +VREF ( +2.5 V typical) to center the voltage for proper ADC input drive. For dc coupled operation, connect E 7 to E9 (analog input A to R11), E14 to E13 (amplifier output to analog input A of AD 9059), E4 to E5 (analog input B to R10), and E 11 to E 10 (amplifier output to analog input B of AD 9059) using the board jumper connectors.
For ac coupled analog input applications, amplifiers U3 and U 4 are removed from the analog signal paths. The analog signals are coupled through capacitors C11 and C12, each terminated to the VREF voltage through separate $1 \mathrm{k} \Omega$ resistors (providing bias current for the AD 9059 analog inputs, AINA and AINB).

A nalog input signals to the board should be 1 V p-p into $50 \Omega$ for full-scale ADC drive. For ac coupled operation, connect E 7 to E8 (analog input A to C12 feedthrough capacitor), E 13 to E15 (C12 to R15 termination resistor for channel A), E4 to E6 (analog input B to C11 feedthrough capacitor), and E10 to E 12 (C 11 to R 14 termination resistor for channel B) using the board jumper connectors.
The on-board reference voltage may be used to drive the ADC or an external reference may be applied. The standard configuration employs the internal voltage reference without any external connection requirements. An external voltage reference may be applied at board connector input REF to overdrive the limited current output of the AD 9059's internal voltage reference. The external voltage reference should be +2.5 V typical.
The power-down function of the AD 9059 can be exercised through a board jumper connection. C onnect E2 to E1 (+5 V to PWRDN ) for power-down mode operation. For normal operation, connect E3 to E1 (ground to PWRDN).
The encode signal source should be T T L/CM OS compatible and capable of driving a $50 \Omega$ termination. The digital outputs of the AD 9059 are buffered through latches on the evaluation board ( $\mathbf{U} 5$ and $\mathbf{U} 6$ ) and are available for the user at connector Pins 30-37 and Pins 22-29. Latch timing is derived from the ADC ENCODE clock and a digital clocking signal is provided for the board user at connector Pins 2 and 21.


Figure 19. AD9059 Dual Evaluation Board Schematic


Figure 20. Evaluation Board Layout (Top)


Figure 21. Evaluation Board Layout (Bottom)

## OUTLINE DIMENSIONS

Dimensions shown in inches and ( mm ).


