ANALOG DEVICES

CMOS, 2.5 Ω Low Voltage, Triple/Quad SPDT Switches in Chip Scale

Preliminary Technical Data

ADG786/ADG788

FEATURES

+1.8 V to +5.5 V Single Supply +/-3 V Dual Supply 2.5 Ω On Resistance 0.5 Ω On Resistance Flatness 100pA Leakage Currents 19ns Switching Times Triple SPDT : ADG786 Quad SPDT : ADG788 Small Chip Scale Package Low Power Consumption TTL/CMOS Compatible Inputs

APPLICATIONS

Data Acquisition Systems Communication Systems Relay replacement Audio and Video Switching Battery Powered Systems

GENERAL DESCRIPTION

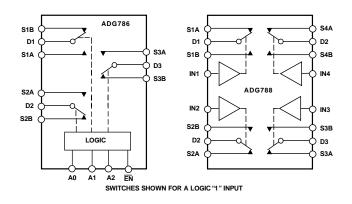
The ADG786 and ADG788 are low voltage, CMOS devices comprising three independently selectable SPDT (single pole, double throw) switches and four independently selectable SPDT switches respectively.

Low power consumption and operating supply range of +1.8 V to +5.5 V and dual +/-3 V make the ADG786 and ADG788 ideal for battery powered, portable instruments. All channels exhibit break before make switching action preventing momentary shorting when switching channels. An $\overline{\text{EN}}$ input on the ADG786 is used to enable or disable the device. When disabled, all channels are switched OFF.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, high signal bandwidths and low leakage currents. On resistance is in the region of a few Ohms, is closely matched between switches and very flat over the full signal range. These parts can operate equally well in either direction and have an input signal range which extends to the supplies.

The ADG786 and ADG788 are available in small Chip Scale packages.

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

- 1. Single/Dual Supply Operation. The ADG786 and ADG788 are fully specified and guaranteed with +3 V and +5 V single supply and +/-3 V dual supply rails.
- 2. Low On Resistance (2.5 Ω typical).
- 3. Low Power Consumption (<0.01 $\mu W).$
- 4. Guaranteed Break-Before-Make Switching Action.
- 5. Available in Chip Scale Package (CSP).

REV. PrC Jan. 2001

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	B V	ersion		
Parameter	+25°C	-40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	2.5		Ω typ	$V_{\rm S}$ = 0 V to $V_{\rm DD}$, $I_{\rm DS}$ = 10 mA;
	4.5	5.0	Ω max	Test Circuit 1
On-Resistance Match Between		0.1	Ω typ	$V_{\rm S}$ = 0 V to $V_{\rm DD}$, $I_{\rm DS}$ = 10 mA
Channels (ΔR_{ON})		0.4	Ω max	5 227 25
On-Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ	$V_{\rm S}$ = 0 V to $V_{\rm DD}$, $I_{\rm DS}$ = 10 mA
		1.2	Ω max	5 22 25
LEAKAGE CURRENTS				$V_{DD} = 5.5 V$
Source OFF Leakage I _S (OFF)	± 0.01		nA typ	$V_{\rm D} = 4.5 \text{ V/1 V}, V_{\rm S} = 1 \text{ V/4.5 V};$
bource off Leanage 15 (011)	± 10	± 20	nA max	Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	± 0.01	±20	nA typ	$V_D = V_S = 1$ V, or 4.5V;
enamer ert Leanage ID, 15 (ert)	± 10	± 20	nA max	Test Circuit 3
		_~0	in i mux	2 cot onour o
DIGITAL INPUTS		0.4	X 7 ·	
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current	0.005		. .	X 7 X 7 X 7
I _{INL} or I _{INH}	0.005	.0.1	µA typ	$V_{IN} = V_{INL}$ or V_{INH}
C Disital Innut Canaditanaa	4	± 0.1	µA max	
C _{IN} , Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	19		ns typ	$R_L = 300 \ \Omega, \ C_L = 35 \ pF;$
		34	ns max	$V_S = 3 V$, Test Circuit 4
t _{OFF}	7		ns typ	$R_L = 300 \ \Omega, \ C_L = 35 \ pF;$
· · · · · · · · · · · · · · · · · ·		12	ns max	$V_{\rm S} = 3$ V, Test Circuit 4
ADG786 t _{on} (EN)	20		ns typ	$R_L = 300 \ \Omega, \ C_L = 35 \ pF;$
	_	40	ns max	$V_s = 3 V$, Test Circuit 5
t _{OFF} (EN)	7	10	ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$;
	10	12	ns max	$V_s = 3 V$, Test Circuit 5
Break-Before-Make Time Delay, t_D	13		ns typ	$R_L = 300 \Omega, C_L = 35 pF;$
		1	ns min	$V_{\rm S} = 3$ V, Test Circuit 6
Charge Injection	± 3		pC typ	$V_{\rm S} = 2 \text{ V}, \text{R}_{\rm S} = 0 \Omega, \text{C}_{\rm L} = 1 \text{nF};$
	0.0			Test Circuit 7
Off Isolation	-62		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz;$
	-82		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Test Circuit 8
Channel to Channel Crosstalk	-62		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$;
	-82		dB typ	$R_L = 50 \ \Omega, \ C_L = 5 \ pF, \ f = 1 \ MHz;$
			J F	Test Circuit 9
-3 dB Bandwidth	200		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 8
C _s (OFF)	11		pF typ	
$C_{\rm D}, C_{\rm S}$ (ON)	34		pF typ	
POWER REQUIREMENTS			- ••	$V_{DD} = +5.5 V$
L_	0.001		uA turn	Digital Inputs = 0 V or $+5.5$ V
I _{DD}	0.001	1.0	µA typ µA max	1100000000000000000000000000000000000
		1.0	µA max	

NOTES ¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

$\label{eq:specific-product} \begin{array}{l} Preliminary \ Technical \ Data \\ SPECIFICATIONS^1 (V_{DD} = 3V \pm 10\%, \ V_{SS} = 0V, \ GND = 0 \ V, \ unless \ otherwise \ noted) \end{array}$

ADG786/ADG788

	B Ve	rsion -40°C		
Parameter	+25°C	-40 C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH Analog Signal Range On-Resistance (R_{ON}) On-Resistance Match Between Channels (ΔR_{ON}) On-Resistance Flatness ($R_{FLAT(ON)}$)	6 11	0 V to V _{DD} 12 0.1 0.5 3	V Ω typ Ω max Ω typ Ω max Ω typ	$\label{eq:VS} \begin{array}{l} V_S = 0 \ V \ to \ V_{DD}, \ I_{DS} = 10 \ mA; \\ Test \ Circuit \ 1 \\ V_S = 0 \ V \ to \ V_{DD}, \ I_{DS} = 10 \ mA \\ V_S = 0 \ V \ to \ V_{DD}, \ I_{DS} = 10 \ mA \end{array}$
LEAKAGE CURRENTS Source OFF Leakage I _S (OFF) Channel ON Leakage I _D , I _S (ON)	$\pm 0.01 \\ \pm 10 \\ \pm 0.01 \\ \pm 10$	±20 ±20	nA typ nA max nA typ nA max	$ \begin{array}{l} V_{\rm DD} = 3.3 \ V \\ V_{\rm S} = 3 \ V/1 \ V, \ V_{\rm D} = 1 \ V/3 \ V; \\ Test \ Circuit \ 2 \\ V_{\rm S} = \ V_{\rm D} = +1 \ V \ or \ +3 \ V; \\ Test \ Circuit \ 3 \end{array} $
DIGITAL INPUTS Input High Voltage, V_{INH} Input Low Voltage, V_{INL} Input Current I_{INL} or I_{INH} C_{IN} , Digital Input Capacitance	0.005 4	2.0 0.4 ±0.1	V min V max μA typ μA max pF typ	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS ² t _{on} t _{off}	28 9	55	ns typ ns max ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$; $V_S = 2 V$, Test Circuit 4 $R_L = 300 \Omega$, $C_L = 35 pF$;
ADG786 t _{on} (EN) t _{off} (EN)	29 9	16 60	ns max ns typ ns max ns typ	$ \begin{array}{l} V_{\rm S} = 2 \ V, \ \mbox{Test Circuit 4} \\ R_{\rm L} = 300 \ \Omega, \ C_{\rm L} = 35 \ p{\rm F}; \\ V_{\rm S} = 2 \ V, \ \mbox{Test Circuit 5} \\ R_{\rm L} = 300 \ \Omega, \ C_{\rm L} = 35 \ p{\rm F}; \end{array} $
Break-Before-Make Time Delay, ${\rm t}_{\rm D}$	22	16 1	ns max ns typ ns min	$V_{S} = 2 V, \text{ Test Circuit 5} \\ R_{L} = 300 \Omega, C_{L} = 35 pF; \\ V_{S} = 2 V, \text{Test Circuit 6} \end{cases}$
Charge Injection Off Isolation	±3 -62 -82		pC typ dB typ dB typ	$ \begin{array}{l} V_{S} = 1 \ V, \ R_{S} = \ 0 \ \Omega, \ C_{L} = 1 \ nF; \\ Test \ Circuit \ 7 \\ R_{L} = \ 50 \ \Omega, \ C_{L} = \ 5 \ pF, \ f = \ 10 \ MHz; \\ R_{L} = \ 50 \ \Omega, \ C_{L} = \ 5 \ pF, \ f = \ 1 \ MHz; \end{array} $
Channel to Channel Crosstalk	-62 -82		dB typ dB typ	Test Circuit 8 $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$; $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Test Circuit 9
-3 dB Bandwidth C _S (OFF) C _D , C _S (ON)	200 11 34		MHz typ pF typ pF typ	$R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 8
POWER REQUIREMENTS I _{dd}	0.001	1.0	μA typ μA max	V_{DD} = +3.3 V Digital Inputs = 0 V or +3.3 V

NOTES

 $^1 \rm Temperature\ ranges\ are\ as\ follows: B Version: -40°C to +85°C. <math display="inline">^2 \rm Guaranteed\ by\ design,\ not\ subject\ to\ production\ test.$

Specifications subject to change without notice.

ADG786/ADG788 **Preliminary Technical Data** $\frac{\text{Dual Supply}^{1}}{\text{U}_{\text{DD}} = +3 \text{ V} \pm 10\%, \text{ V}_{\text{SS}} = -3 \text{ V} \pm 10\%, \text{ GND} = 0 \text{ V}, \text{ unless otherwise noted}}{\text{B Version}}$

	BV	ersion		
-	0.50 G	-40°C	.	
Parameter	+25°C	to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R _{ON})	2.5	5 0	Ω typ	$V_{\rm S} = V_{\rm SS}$ to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA;
On Desistance Match Detrucen	4.5	$\begin{array}{c} 5.0 \\ 0.1 \end{array}$	Ω max	Test Circuit 1
On-Resistance Match Between Channels (ΔR_{ON})		0.1	Ω typ Ω max	$V_{S} = V_{SS}$ to V_{DD} , $I_{DS} = 10$ mA
On-Resistance Flatness $(R_{FLAT(ON)})$	0.5	0.4	Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10$ mA
On resistance Trainess (refLAT(ON))	0.0	1.2	Ω max	v ² = v ²² to v ^{DD} , v ^{D2} = 10 m ²
LEAKAGE CURRENTS				$V_{DD} = +3.3 \text{ V}, V_{SS} = -3.3 \text{ V}$
Source OFF Leakage I _S (OFF)	±0.01		nA typ	$V_{\rm S} = +2.25 \text{V}/-1.25 \text{V}, V_{\rm D} = -1.25 \text{V}/+2.25 \text{V};$
-	±10	± 20	nA max	Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	±0.01		nA typ	$V_{\rm S} = V_{\rm D} = +2.25$ V/-1.25 V, Test Circuit 3
	±10	± 20	nA max	
DIGITAL INPUTS		0.5		
Input High Voltage, V _{INH}		2.0	V min	
Input Low Voltage, V _{INL}		0.4	V max	
Input Current	0.005		uA tun	$V_{IN} = V_{INL}$ or V_{INH}
I _{INL} or I _{INH}	0.005	±0.1	μA typ μA max	$\mathbf{v}_{\rm IN} = \mathbf{v}_{\rm INL}$ or $\mathbf{v}_{\rm INH}$
C _{IN} , Digital Input Capacitance	4	±0.1	pF typ	
DYNAMIC CHARACTERISTICS ²	-		P ² ·JP	
t _{ON}	21		ns typ	$R_{L} = 300 \ \Omega, \ C_{L} = 35 \ pF;$
-011		35	ns max	$V_{\rm S} = 1.5$ V, Test Circuit 4
t _{OFF}	10		ns typ	$R_{L} = 300 \Omega$, $C_{L} = 35 pF$;
		16	ns max	$V_S = 1.5 V$, Test Circuit 4
ADG786 t _{on} (EN)	21		ns typ	$R_L = 300 \ \Omega, \ C_L = 35 \ pF;$
	10	40	ns max	$V_s = 1.5 V$, Test Circuit 5
t _{OFF} (EN)	10	16	ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$;
Break-Before-Make Time Delay, t _D	13	10	ns max ns typ	$V_S = 1.5 V$, Test Circuit 5 $R_L = 300 \Omega$, $C_L = 35 pF$;
Dieak-Deloie-Make Time Delay, t _D	15	1	ns typ	$V_{\rm S} = 1.5$ V, Test Circuit 6
Charge Injection	±5	1	pC typ	$V_{\rm S} = 0$ V, $R_{\rm S} = 0$ Ω , $C_{\rm L} = 1$ nF;
89			F- JF	Test Circuit 7
Off Isolation	-62		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$;
	-82		dB typ	$R_{L} = 50 \Omega$, $C_{L} = 5 pF$, $f = 1 MHz$;
			-	Test Circuit 8
Channel to Channel Crosstalk	-62		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz;$
	-82		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Test Circuit 9
-3 dB Bandwidth	200		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 9
C _S (OFF)	11		pF typ	- •
$C_{\rm D}, C_{\rm S}$ (ON)	34		pF typ	
POWER REQUIREMENTS				V_{DD} = +3.3 V
I _{DD}	0.001		μA typ	Digital Inputs = 0 V or $+3.3$ V
10D	0.001	1.0	μΑ typ μΑ max	Digital inputs -0 v of $+5.5$ v
I _{SS}	0.001	1.0	μΑ typ	$V_{SS} = -3.3 V$
		1.0	μA max	Digital Inputs = 0 V or $+3.3$ V
	l		I	0 r

NOTES ¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATING	GS ¹	Storage Temperature Range -65°	C to +150°C
$(T_A = +25^{\circ}C \text{ unless otherwise noted})$		Junction Temperature	+150°C
V_{DD} to V_{SS}	+7 V	20 Lead CSP, θ_{JA} Thermal Impedance	TBD°C/W
V_{DD} to GND	-0.3 V to +7 V	Lead Temperature, Soldering (10seconds)	300°C
V _{SS} to GND	+0.3 V to -3.5 V	IR Reflow, Peak Temperature	+220°C
55	-0.3 V to V _{DD} +0.3 Vor	ESD	2kV
	Whichever Occurs First	NOTES	
Digital Inputs ²	-0.3V to V_{DD} +0.3 V or	¹ Stresses above those listed under "Absolute Maximum Ratings" ma	
0 1	Whichever Occurs First	damage to the device. This is a stress rating only and functional ope	
Peak Current. S or D	100mA	at these or any other conditions above those listed in the operatio	
	s, 10% Duty Cycle max)	specification is not implied. Exposure to absolute maximum rate extended periods may affect device reliability. Only one absolute maximum rate of the specific device reliability.	
Continuous Current, S or D	30mA	be applied at any one time.	0,
Operating Temperature Range		² Overvoltages at IN, S or D will be clamped by internal diodes. Curren	nt should be limited
Industrial (B Version)	-40°C to +85°C	to the maximum ratings given.	

CAUTION -

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG786/ADG788 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

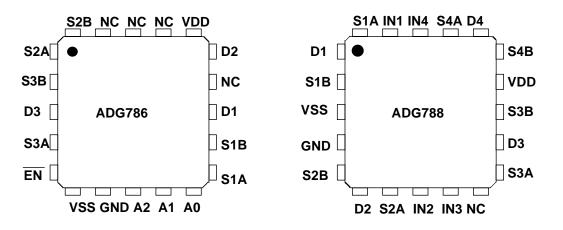


ADG786/ADG788

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG786BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-20
ADG788BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-20

PIN CONFIGURATIONS



Exposed Pad tied to Substrate, V_{SS}

ADG786/ADG788

Table 1. ADG786 Truth Table

A2	A1	A0	$\overline{E} \overline{N}$	ON Switch
X	Х	Х	1	NONE
0	0	0	0	D1-S1A, D2-S2A, D3-S3A
0	0	1	0	D1-S1B, D2-S2A, D3-S3A
0	1	0	0	D1-S1A, D2-S2B, D3-S3A
0	1	1	0	D1-S1B, D2-S2B, D3-S3A
1	0	0	0	D1-S1A, D2-S2A, D3-S3B
1	0	1	0	D1-S1B, D2-S2A, D3-S3B
1	1	0	0	D1-S1A, D2-S2B, D3-S3B
1	1	1	0	D1-S1B, D2-S2B, D3-S3B

Preliminary Technical Data

Table	1.	ADG788	Truth	Table	
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Logic	Switch A	Switch B
0	OFF	O N
1	O N	OFF

X = Don't Care

TERMINOLOGY

V_{DD} Most positive power supply potential. V_{SS} Most Negative power supply in a dual supply application. In single supply applications, this should be tied to ground close to the device. I_{DD} Positive supply current. I_{SS} Negative supply current. GND Ground (0 V) reference.SSource terminal. May be an input or output.DDrain terminal. May be an input or output.NLogic control input. $V_D(V_S)$ Analog voltage on terminals D, S R_{ON} Ohmic resistance between D and S. AR_{ON} On resistance match between any two channels, i.e. R_{ON} max - R_{ON} min $R_{FLATION}$ Flatness is defined as the difference between the maximum and minimum value of on-resistance as mea sured over the specified analog signal range.Is(OFF)Source leakage current with the switch "OFF."Ip. (SOFF)Drain leakage current with the switch "OFF."Ip. (SOFF)Drain leakage current with the switch "OFF."Ip. (Input)Input current of the digital input.VinktMaximum input voltage for logic "1".Invi.(Input)Input current of the digital input.Cs (OFF)"OFF" switch drain capacitance. Measured with reference to ground.Cp.(Cs(ON))"ON" switch capacitance. Measured with reference to ground.Cn.(EN)Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition.topF(EN)Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition.topF(CN)Delay time between the 50% and 9
In the second of the device.IppPositive supply current.IssNegative supply current.GNDGround (0 V) reference.SSource terminal. May be an input or output.DDDDrain terminal. May be an input or output.INLogic control input.Vp (Vs)Analog voltage on terminals D, SGONDOhnic resistance between D and S.AR _{ON} On resistance between D and S.AR _{ON} On resistance between D and S.AR _{ON} Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.Is(OFF)Dorain leakage current with the switch "OFF."Ip. Is (ON)Channel leakage current with the switch "ON".VintMaximum input voltage for logic "1".Invit.(Inv.)Invit.(Inv.)Input current of the digital input.Cs (OFF)"OFF" switch drain capacitance. Measured with reference to ground.Cp. Cs (ON)"ON" switch capacitance.Delay time measured between the 50% and 90% points of the digital input and the switch "ON" condition.Men switching from one address state to another.tor(EN)Delay time between t
IDDPositive supply current.IgsNegative supply current.GNDGround (0 V) reference.SSource terminal. May be an input or output.DDrain terminal. May be an input or output.INLogic control input.VD(Vs)Analog voltage on terminals D, SRonOhmic resistance between D and S.ARoNOn resistance match between any two channels, i.e. $R_{ON}max - R_{ON}min$ $R_{TLAT(ON)}$ Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.Is(OFF)Source leakage current with the switch "OFF."Ip. (ISF)Drain leakage current with the switch "OFF."Ip. (IS (ON)Channel leakage current with the switch "OFF."Ip. Is (ON)VinitMaximum input voltage for logic "0".VinitMinimum input voltage for logic "1".Intil (Intro)Intro (OFF)"OFF" switch drain capacitance. Measured with reference to ground.Cp. Cs(ON)"OFF" switch drain capacitance. Measured with reference to ground.Cp. Cs(ON)CharactCharacttransmonDelay time between the 50% and 90% points of the digital input and the switch "ON" conditionwhen switching from one address state to another.topF(EN)Delay time between the 50% and 90% points of the EN digital input and the switch "OFF" condition.topF(EN)Delay time between the 50% and 90% points of both switches when switching from one a
IssNegative supply current.GNDGround (0 V) reference.SSource terminal. May be an input or output.DDrain terminal. May be an input or output.INLogic control input. $V_D(V_S)$ Analog voltage on terminals D, S R_{ON} Ohmic resistance between D and S. ΔR_{ON} On resistance between D and S. AR_{ON} Flatness is defined as the difference between the maximum and minimum value of on-resistance as mea sured over the specified analog signal range.Is(OFF)Source leakage current with the switch "OFF."Ip. Is (ON)Channel leakage current with the switch "OFF."Ip. Is (ON)Channel leakage current with the switch "OFF."Ip. Is (ON)Channel leakage current with the switch "OFF."VINLMaximum input voltage for logic "1".VINLMinimum input voltage for logic "1".VINHMinimum input voltage for logic "1".VINH"OFF" switch drain capacitance. Measured with reference to ground.Cp. (OFF)"OFF" switch drain capacitance. Measured with reference to ground.Cp. (SGON)"ON" switch capacitance. Measured with reference to ground.Cp. (SCION)Delay time measured between the 50% and 90% points of the digital input and the switch "ON" condition.torfe(EN)Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition.torfe(EN)Delay time between the 80% points of both switches when switching from one address state to another.corection"OFF"transtring"OFF"dimensure o
$ \begin{array}{llllllllllllllllllllllllllllllllllll$
SSource terminal. May be an input or output.DDrain terminal. May be an input or output.INLogic control input.VD (V3)Analog voltage on terminals D, SRonOhmic resistance between D and S. ΔR_{ON} On resistance match between any two channels, i.e. R_{ON} max - R_{ON} min $R_{FLAT(ON)}$ Flatness is defined as the difference between the maximum and minimum value of on-resistance as mea sured over the specified analog signal range. I_S (OFF)Source leakage current with the switch "OFF." I_D (JS (ON)Channel leakage current with the switch "OFF." I_D , Is (ON)Channel leakage for logic "0". V_{INL} Maximum input voltage for logic "1". V_{INL} Maximum input voltage for logic "1". V_{INH} Minimum input voltage for logic "1". C_S (OFF)"OFF" switch capacitance. Measured with reference to ground. C_p , $C_S(ON)$ "ON" switch capacitance. Measured with reference to ground. C_p , $C_S(ON)$ Digital input capacitance. Measured with reference to ground. C_{P} , $C_S(ON)$ Digital input capacitance. Measured with reference to ground. C_{P} , $C_S(ON)$ Digital input capacitance. $T_{RANSITION}$ Delay time between the 50% and 90% points of the digital input and the switch "ON" condition. v_{PRE} Delay time between the 50% and 90% points of both switches when switching from one address state to another. $C_{PF}(EN)$ Delay time between the 50% and 90% points of both switches when switching from one address state to another. $C_{PF}(EN)$ Delay time between the 50%
DDrain terminal. May be an input or output.INLogic control input. $V_D(V_S)$ Analog voltage on terminals D, S R_{ON} Ohmic resistance between D and S. AR_{ON} On resistance match between any two channels, i.e. $R_{ON}max - R_{ON}min$ $R_{FLAT(ON)}$ Flatness is defined as the difference between the maximum and minimum value of on-resistance as mea sured over the specified analog signal range. I_S (OFF)Source leakage current with the switch "OFF." I_D (JS (OFF)Drain leakage current with the switch "OFF." I_D , I_S (ON)Channel leakage current with the switch "ON". V_{INL} Maximum input voltage for logic "0". V_{INL} Minimum input voltage for logic "1". $I_{INL}(INH)$ Input current of the digital input. C_S (OFF)"OFF" switch drain capacitance. Measured with reference to ground. C_D (CFF)Digital input capacitance. $C_D, C_S(ON)$ "ON" switch capacitance. Measured with reference to ground. $C_D, C_S(ON)$ Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another. t_{OFF} Delay time between the 50% and 90% points of the EN digital input and the switch "OFF" condition. t_{OFF} The measured between the 80% points of both switches when switching from one address state to another. t_{OFF} Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition. t_{OFF} The measured between the 80% points of both switches when switching from one address state to another. <td< td=""></td<>
INLogic control input. $V_D(v_S)$ Analog voltage on terminals D, S R_{ON} Ohmic resistance between D and S. AR_{ON} On resistance match between any two channels, i.e. $R_{ON}max - R_{ON}min$ $R_{FLAT(ON)}$ Flatness is defined as the difference between the maximum and minimum value of on-resistance as mea sured over the specified analog signal range. I_S (OFF)Source leakage current with the switch "OFF." I_D (OFF)Drain leakage current with the switch "OFF." I_D (OFF)Drain leakage current with the switch "ON." V_{INL} Maximum input voltage for logic "0". V_{INL} Maximum input voltage for logic "1". $I_{INL}(I_{INH})$ Input current of the digital input. C_S (OFF)"OFF" switch source capacitance. Measured with reference to ground. C_D (OFF)Digital input capacitance. Measured with reference to ground. $C_{D, CS}(ON)$ "ON" switch capacitance. Measured with reference to ground. C_{IN} Digital input capacitance. $T_{RANSTION}$ Delay time between the 50% and 90% points of the digital input and the switch "ON" condition. t_{OFF} Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition. t_{OFF} To the agained between the 80% points of both switches when switching from one address state to another. t_{OFF} Heasured between the 80% points of both switches when switching from one address state to another. t_{OFF} To the again of the glitch impulse transferred from the digital input to the analog output during switching. $njection$ Off Isol
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$ \begin{array}{lll} I_{S} \ (OFF) & Source leakage current with the switch "OFF." \\ I_{D} \ (OFF) & Drain leakage current with the switch "OFF." \\ I_{D}, I_{S} \ (ON) & Channel leakage current with the switch "ON." \\ V_{INL} & Maximum input voltage for logic "0". \\ V_{INH} & Minimum input voltage for logic "1". \\ I_{INL} (I_{INH}) & Input current of the digital input. \\ C_{S} \ (OFF) & "OFF" switch source capacitance. Measured with reference to ground. \\ C_{D} \ (OFF) & OFF" switch drain capacitance. Measured with reference to ground. \\ C_{D}, C_{S} (ON) & ON" switch capacitance. Measured with reference to ground. \\ C_{IN} & Digital input capacitance. Measured with reference to ground. \\ C_{IN} & Digital input capacitance. \\ T_{TRANSITION} & Delay time measured between the 50% and 90% points of the digital input and the switch "ON" condition. \\ more switching from one address state to another. \\ t_{ON}(EN) & Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition. \\ t_{OFF} (EN) & Delay time between the 50% and 90% points of the EN digital input and the switch "OFF" condition. \\ more switching from one address state to another. \\ t_{OPEN} & "OFF" time measured between the 80% points of both switches when switching from one address state to another. \\ Charge Injection & A measure of the glitch impulse transferred from the digital input to the analog output during switching. \\ A measure of unwanted signal coupling through an "OFF" switch. \\ \end{array}$
$ \begin{array}{lll} I_{D} \ (\text{OFF}) & \text{Drain leakage current with the switch "OFF."} \\ I_{D}, I_{S} \ (\text{ON}) & \text{Channel leakage current with the switch "ON."} \\ W_{\text{INL}} & \text{Maximum input voltage for logic "0".} \\ W_{\text{INH}} & \text{Minimum input voltage for logic "1".} \\ I_{\text{INL}, (I_{\text{INH}})} & \text{Input current of the digital input.} \\ C_{S} \ (\text{OFF}) & "\text{OFF" switch source capacitance. Measured with reference to ground.} \\ C_{D}, (\text{OFF}) & "\text{OFF" switch drain capacitance. Measured with reference to ground.} \\ C_{D}, C_{S} \ (\text{ON}) & "\text{ON" switch capacitance. Measured with reference to ground.} \\ C_{D}, C_{S} \ (\text{ON}) & "\text{ON" switch capacitance. Measured with reference to ground.} \\ C_{D}, C_{S} \ (\text{ON}) & \text{Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition.} \\ Measured with reference to ground. \\ C_{ON} \ (\text{EN}) & \text{Delay time between the 50% and 90\% points of the EN digital input and the switch "ON" condition.} \\ t_{OFF} \ (\text{EN}) & \text{Delay time between the 50\% and 90\% points of the EN digital input and the switch "OFF" condition.} \\ More \ (\text{OFF})^{T} \ (\text{time measured between the 80\% points of both switches when switching from one address state to another.} \\ C_{\text{DR}} \ (\text{OFF})^{T} \ (\text{time measured between the 80\% points of both switches when switching from one address state to another.} \\ C_{\text{DFFN}} \ (\text{OFF}^{T} \ \text{time measured between the 80\% points of both switches when switching from one address state to another.} \\ C_{\text{harge}} \ (\text{A measure of the glitch impulse transferred from the digital input to the analog output during switching.} \\ A \ measure of unwanted signal coupling through an "OFF" switch.} \ (\text{OFF" switch.} \ (\text{OFF" switch.} \ (\text{OFF" switch.} \ (\text{OFF" switch)} \ (OFF" swit$
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V_{INL} Maximum input voltage for logic "0". V_{INH} Minimum input voltage for logic "1". $I_{INL}(I_{INH})$ Input current of the digital input. C_S (OFF)"OFF" switch source capacitance. Measured with reference to ground. C_D (OFF)"OFF" switch drain capacitance. Measured with reference to ground. $C_D, C_S(ON)$ "ON" switch capacitance. Measured with reference to ground. C_{IN} Digital input capacitance. $T_{RANSITION}$ Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition $t_{ON}(EN)$ Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition. $t_{OFF}(EN)$ Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition. $t_{OFF}(EN)$ Delay time between the 50% and 90% points of both switches when switching from one address state to another. $t_{OFF}(EN)$ Delay time between the 50% and 90% points of both switches when switching from one address state to another. $t_{OFF}(EN)$ Delay time between the 80% points of both switches when switching from one address state to another. t_{OFF} Time measured between the 80% points of both switches when switching from one address state to another. t_{OFF} A measure of the glitch impulse transferred from the digital input to the analog output during switching.InjectionA measure of unwanted signal coupling through an "OFF" switch.
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C_S (OFF)"OFF" switch source capacitance. Measured with reference to ground. C_D (OFF)"OFF" switch drain capacitance. Measured with reference to ground. $C_D, C_S(ON)$ "ON" switch capacitance. Measured with reference to ground. C_{IN} Digital input capacitance. $t_{TRANSITION}$ Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another. $t_{ON}(EN)$ Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition. $t_{OFF}(EN)$ Delay time between the 50% and 90% points of the EN digital input and the switch "OFF" condition. t_{OPEN} "OFF" time measured between the 80% points of both switches when switching from one address state to another.Charge InjectionA measure of the glitch impulse transferred from the digital input to the analog output during switching.Off IsolationA measure of unwanted signal coupling through an "OFF" switch.
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another. Charge Injection Off Isolation A measure of unwanted signal coupling through an "OFF" switch.
Injection Off Isolation A measure of unwanted signal coupling through an "OFF" switch.
Off Isolation A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic
capacitance.
Bandwidth The frequency at which the output is attenuated by 3dBs.
On Response The Frequency response of the "ON" switch.
Insertion The loss due to the ON resistance of the switch.
Loss

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TYPICAL PERFORMANCE CHARACTERISTICS

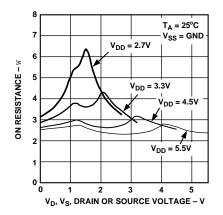


Figure 1. On Resistance as a Function of $V_D(V_S)$ for for Single Supply

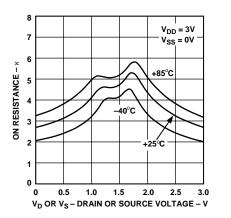


Figure 4. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply

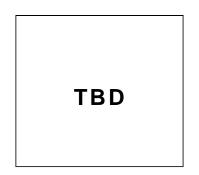


Figure 7. Leakage Currents as a function of $V_D(V_S)$

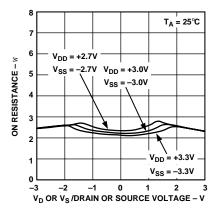


Figure 2. On Resistance as a Function of $V_D(V_S)$ for Dual Supply

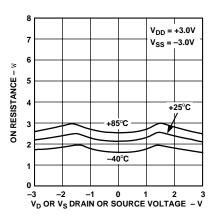


Figure 5. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Dual Supply

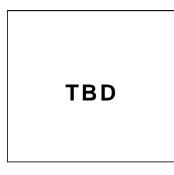


Figure 8. Leakage Currents as a function of $V_D(V_S)$

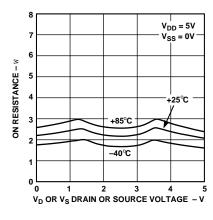


Figure 3. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply

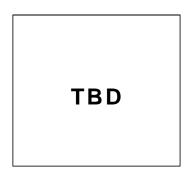


Figure 6. Leakage Currents as a function of $V_D(V_S)$

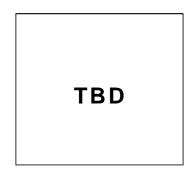


Figure 9. Leakage Currents as a function of Temperature

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Preliminary Technical Data

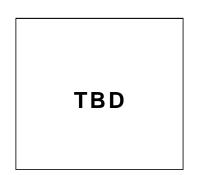


Figure 10. Leakage Currents as a Function of Temperature

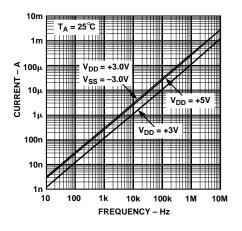


Figure 13. Supply Currents vs. Input Switching Frequency

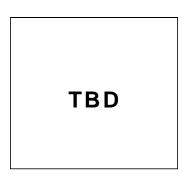


Figure 11. T_{ON}/T_{OFF} Times vs. Temperature

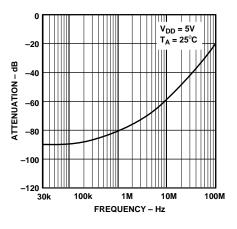


Figure 14. Off Isolation vs. Frequency

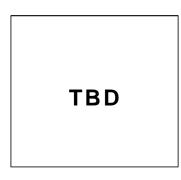


Figure 12. On Response vs. Frequency

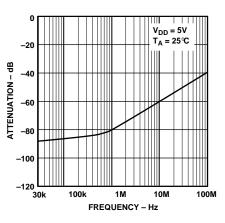


Figure 15. Crosstalk vs. Frequency

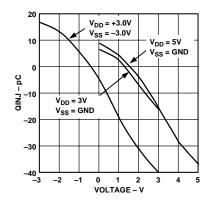
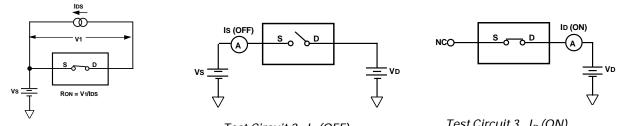


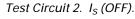
Figure 16. Charge Injection vs. Source Voltage

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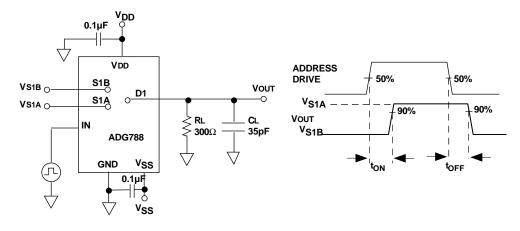
Test Circuits



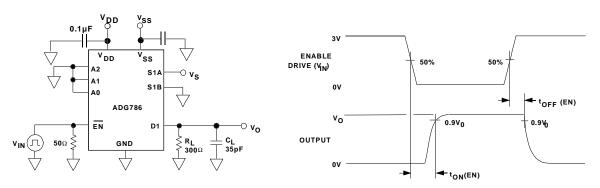
Test Circuit 1. On Resistance.



Test Circuit 3. I_D (ON)



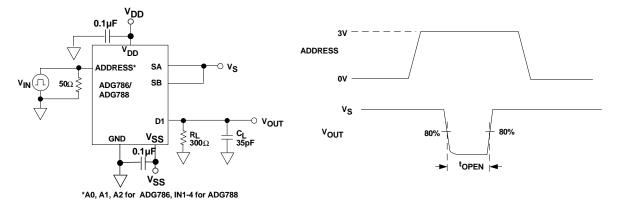
Test Circuit 4. Switching Times.



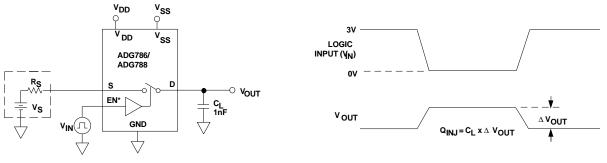
Test Circuit 5. Enable Delay, t_{ON} (EN), t_{OFF} (EN).

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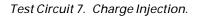
Preliminary Technical Data

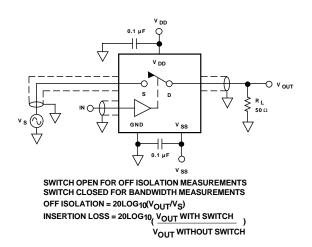


Test Circuit 6. Break Before Make Delay, t_{OPEN}.

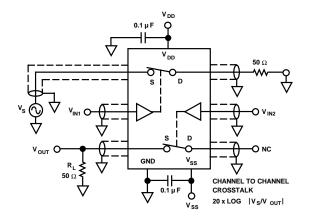


* IN1-4 for ADG786





Test Circuit 8. OFF Isolation and Bandwidth.



Test Circuit 9. Channel-to-Channel Crosstalk.

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead CSP (CP-20)

