ANALOG DEVICES

JPEG2000 Co-processor

Preliminary Technical Data — ADV-JP2000

16-May-2001

Features

- SURF™ (Spatial Ultra-efficient Recursive Filtering) patented technology enables high-performance, low-power, and low-cost JPEG2000 compression/ decompression.
- Lossless compression at >10 Mpixels/second
- Reversible and irreversible 5/3 wavelet transform.
- Lossless and Lossy compression modes. Supports 8 or 10-bit pixel components in reversible mode and 8 to 14-bit pixel components in irreversible mode.
- Programmable tile size up to 160 x 128 in three-component interleaved mode, up to 256 x 256 in single-component mode.
- Flexible pixel/component interface.
- Coding pass distortion metrics provided for precise control of compressed image size.
- A single 16-bit asynchronous SRAM style interface allows glue-less connection to most microcontrollers and ASICs.
- 3.3v I/O and 1.5-1.8v core supply.
- 7mm x 7mm 48-ball fpBGA.

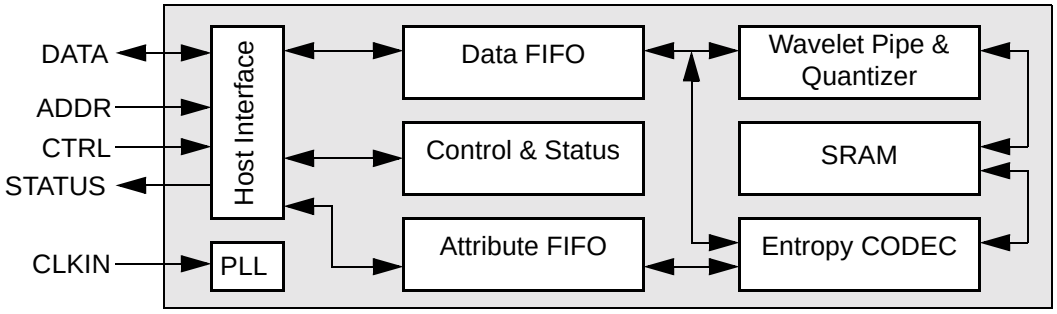
Applications

- Digital Still Cameras
- Networked video and image distribution systems
- Wireless video and image distribution
- Image archival/retrieval
- Digital CCTV and surveillance systems
- Video editing systems

General Description

The ADV-JP2000 is a high-performance image compression co-processor that implements the computationally intensive operations of the JPEG2000 (J2K) image compression standard. The ADV-JP2000 can process images at a rate of >10 Mpixels/sec in lossless mode, and at significantly higher rates when used in lossy mode. The chip supports lossless compression of 8 or 10-bit component data and can support lossy compression of component data up to 14-bits. This chip, along with a minimal amount of software on the user's host processor, will provide a complete high performance JPEG2000 image compression and decompression solution. The chip contains a full custom wavelet processor and entropy codec as well as associated interface and control functions. The wavelet processor implements the 5/3 wavelet transform in either reversible or irreversible modes. The entropy codec supports the key features in the current JPEG2000 specification. The ADV-JP2000 provides a very flexible interface that supports a wide variety of pixel and component formats.

The ADV-JP2000 provides a single simple asynchronous interface for all communications between itself and a host CPU or system ASIC. The ADV-JP2000 supports both single and dual-address DMA transfers to and from on-chip FIFOs. A complete definition of the DMA process is described in "DMA Access Modes," on page 5. Control and status registers within the ADV-JP2000 are addressed directly using the address bus,



Rev. PrA

SURF is a trademark of Analog Devices, Inc.

This information applies to a product under development. Its characteristics and specifications are subject to change without no tice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing. No responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O.Box 9106, Norwood, MA 02062-9106, U.S.A. **www.analog.com/video**

Tel:1-800-ANALOGD (262-5643) Fax:781-461-3700

©Analog Devices,Inc., 2001

the chip select, and the appropriate read or write strobe.

Operational Overview

The ADV-JP2000 has two basic modes of operation, encode and decode. In encode (compression), the ADV-JP2000 accepts a single uncompressed image tile and creates a stream of J2K compliant code-blocks. In decode (decompression), this process is reversed. Both encode and decode are broken down into two separate processes, Wavelet processing, which includes quantization, and Entropy processing.

The ADV-JP2000 operates on a rectangular section of an image called a tile. The maximum tile size supported depends on the number of components in the tile and the maximum desired width. For component interleaved tiles (i.e., tiles containing both luminance and chrominance data) the ADV-JP2000's maximum tile size is 160 x 128. For single-component tiles, the maximum tile size is 256 x 256. The minimum tile size supported is 8 x 8.

During encode, the ADV-JP2000 also generates a stream of attributes for each code-block. The code-block attributes are used by the host's software to create packet headers for the final J2K bit stream. The chip can also be programmed to provide distortion metrics for each coding pass. The distortion metrics can be used by the host software to precisely control the resultant file size when operating in lossy mode.

During decode, the ADV-JP2000 requires a minimal set of attributes to be loaded prior to processing each code-block. Details of the attribute data are describe in "Code-block Attribute Formats," on page 3

The encode process consists of five basic steps: (1) load configuration and operating parameters, (2) load a single uncompressed tile into the ADV-JP2000, (3) issue a start command, (4) wait for output data to become ready, and (5) unload J2K compressed code-blocks and attributes. The attributes can be read after each code-block is completed, or the user can allow them to accumulate in the attribute FIFO to be read at a later time. Note: If the ADV-JP2000 is configured for code-block termination and distortion metric output is not enabled, then all of the attribute data for the complete tile will fit in the on-chip FIFO. This allows the host software to wait until it has unloaded all code-block data before having to unload the attribute data.

The decode process also consists of five basic steps: (1) load configuration and operating parameters, (2) load a set of J2K compressed code-blocks and attributes for a single tile into the ADV-JP2000, (3) issue a start command, (4) wait for output data to become ready, and (5) unload the uncompressed tile. Each code-block's attributes must have been written to the ADV-JP2000 prior to loading its associated code-block. A code-block's attributes can be written immediately prior to loading the code-block, or several code-blocks worth of attributes can be written in advance provided there is room for them in the attribute FIFO.

Data FIFO Formats

This FIFO is used to transfer either uncompressed tile data or J2K compressed code-blocks. The data type and access direction are implied from the mode and load state of the ADV-JP2000. The Data FIFO is comprised of 128 words (16-bits).

Pixel Formats

The ADV-JP2000 supports three component modes: (1) three-component interleaved, (2) two-component interleaved, and (3) single-component. Three-component mode supports 4:2:2 tiles in which Y, Cb and Cr are interleaved. The two-component interleaved mode is used when processing a chrominance (Cb/Cr) only tile when using 4:2:2 pixel data formats. Single-component supports a tile with only one component, such as luminance. It can also be used to process 4:4:4 data, one component at a time. Uncompressed tile data is always transferred in raster order starting from the upper-left corner of the tile.

The ADV-JP2000 supports both reversible and irreversible wavelet transforms. The reversible transform supports either 8 or 10-bit pixel component input. The irreversible transform supports fixed precision 8 and 10-bit pixel components as well as a variable precision format that supports up to 14-bits. The user may optionally specify zero, one or two guard bits when using 8 or 10-bit data. 8 and 10-bit pixel components are right (lsb) justified on the 16-bit data bus. The ADV-JP2000 also supports several packing modes to allow two 8-bit components to be transferred in a single 16-bit word. For three-component 4:2:2 mode, this represents pairs of Y/Cb and Y/Cr. For two-component interleaved mode, pairs of Cb and Cr are packed

into one word. For single-component mode, two components of the same type can be packed into one word. For non-packed formats, the user must provide the data in a properly interleaved fashion. For example, for three-component 4:2:2 non-packed mode, the data must be presented in the following order Y_0,Cb_0,Y_1,Cr_0,Y_2,Cb_2,Y_3,Cb_2,...

The ADV-JP2000 also features a raw pixel component mode that supports up to 14-bits per component. In raw mode the pixel components must be left (msb) justified on the 16-bit data bus and all scaling, guard bit adjustment, and sign extension must be done by the user. Input data of less then 14-bits must be padded out to 14-bits by inserting zeros into the lsbs. The alignment of all pixel formats is shown in Figure 1, “Pixel Component Formats,” on pag e3.

Compressed Byte Stream Format

The ADV-JP2000 encodes or decodes JPEG2000 byte stream code-blocks. The code-blocks are always 64 by 64 unless the wavelet sub-band is smaller then that dimension. In that case, the code-block’s size will be equal to the sub-band size. The bytes are packed into 16-bit words in big-endian order. If a compressed code-block ends on an odd byte boundary, then the first compressed byte of the next codeblock will be packed into the low byte. The exception to this is at the end of the last codeblock in the tile. In this case, the low byte in the last word will be padded with zeroes.

Code-block Attribute Formats

During encode, the Attribute FIFO is used to transfer the code-block attributes to the host CPU so that the software can create the necessary J2K packet headers. When the ADV-JP2000 is in encode mode, it will output two header words for each code-block and a segment length count for each coding pass. Optionally, if distortion metrics are enabled, then each segment length count will also be paired with the corresponding distortion metric for the particular coding pass.

During decode, this FIFO is used to transfer code-block attributes to the ADV-JP2000 so that the compressed code-blocks can be properly extracted and decompressed. When the JP2000 is in decode, the host CPU must not insert distortion metrics into the Attribute FIFO. The Attribute FIFO is comprised of 128 words (16-bits).

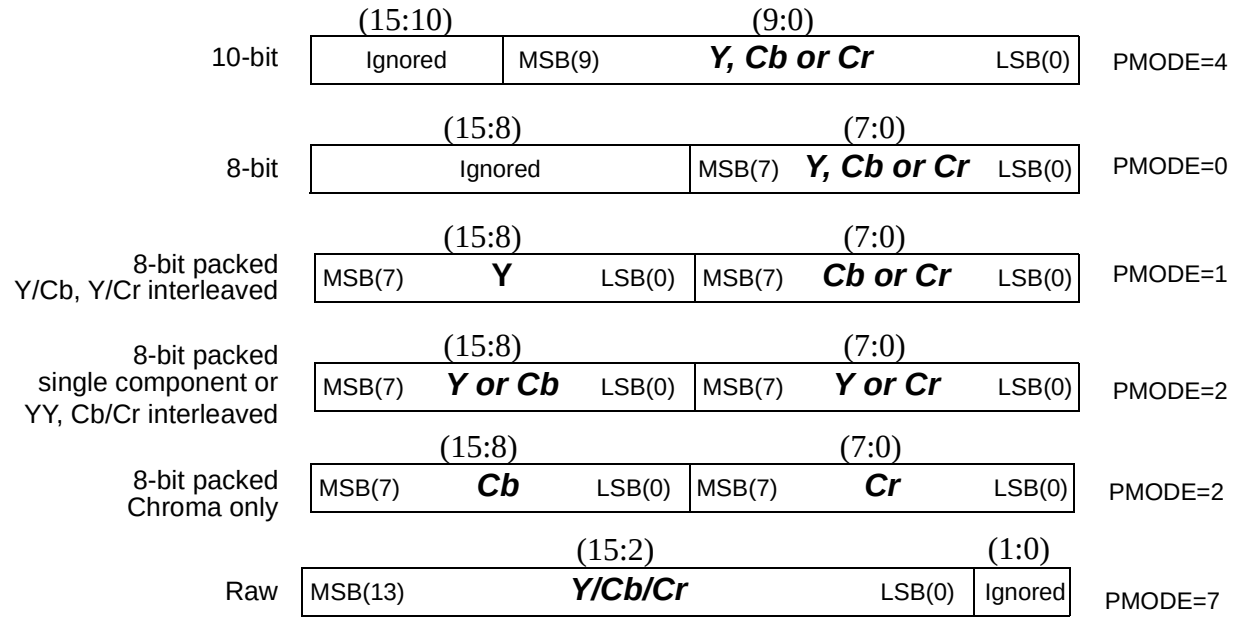


FIGURE 1. Pixel Component Formats

Code-block Header 1

First word of code-block attribute packet for each code-block.

Bit(s)	Name	Description	Note:
1:0	CBY	Code-block Y index	
3:2	CBX	Code-block X index	
5:4	SBID	Sub-band ID; 0=LL, 1=LH, 2=HL, 3=HH	
7:6	LEV	Transform Level; 0=lowest	
9:8	COMP	Component; 0=Y, 1=Cb, 2=Cr	
13:10	NZBP	Number of leading zero bit-planes	
14	LCB	Last code-block flag, must be set to 1 for last code-block, 0 otherwise.	
15	CHF	Code header flag, set to 1 to indicate this is a header word	

Code-block Header 2

Second word of code-block attribute packet for each code-block.

Bit(s)	Name	Description	Note:
5:0	NCP	Number of coding passes in code-block	
11:6	NCS	Number of code-word segments	
12	RCE	Byte length running counts; 0=delta counts, 1=running count	Encode only
13	BLE	Byte lengths included; 0=not include, 1=included	Encode only
14	DME	Distortion metrics included; 0=not included, 1=included	Encode only
15	CHF	Code header flag, set to 1 to indicate this is a header word	

Code-block Distortion Metric

The distortion metric for each code-word segment. This data is optional in encode mode and must be omitted in decode mode.

Bit(s)	Name	Description	Note:
7:0	MANT	Mantissa	
14:8	EXP	Exponent	
15	CHF	Code block header flag, Must always be zero for this word	

Code-word Segment Length

The length of the code-word segment in bytes.

Bit(s)	Name	Description	Note:
14:0	CSL	Number of bytes in code-word segment	
15	CHF	Code block header flag, Must always be zero for this word	

DMA Access Modes

In addition to normal addressed read and write operations, the ADV-JP2000 supports self initiated DMA and host initiated DMA accesses.

Both single and dual-address DMA modes are supported for self initiated DMA. The dual-address mode is very similar to the addressed read and write operations except the ADV-JP2000 initiates a data transfer by asserting DREQ. In single-address DMA mode, the ADV-JP2000 also initiates the data transfer by asserting DREQ, but it determines the direction and type of transfer based on the load-state and access mode of the chip.

The ADV-JP2000 operates in one of two modes, encode or decode. Furthermore, each of these modes has two load-states, load or unload. When the ADV-JP2000 is in single-address DMA mode, it is capturing data in fly-by mode. In this mode the ADV-JP2000 is capturing data off of the data bus while sharing a common set of read/write enables with another peripheral. This makes it necessary for the ADV-JP2000 to have different interpretations of the RD and WE signals. For instance, when the ADV-JP2000 is in Encode, Single-address DMA mode, and expecting data to be loaded, it is actually watching the data bus for reads (RD) issued by the host CPU and ignores any writes. When it sees a read on the data bus, it actually interprets this as a write. Conversely, when the ADV-JP2000 is expecting data to be unloaded, it will interpret writes (WE) issued by the host CPU as reads and ignore any writes.

The functionality of the RD, WE and DACK pins for single-address DMA mode is described in Table 1, “Single-address DMA mode pin functionality.,” on page 5 below.

Table 1: Single-address DMA mode pin functionality.

CS	Mode	Access Mode	Load-State	RD	WE	DACK
0	Don’t care	Don’t care	Don’t care	Register read	Register write	Normal
1	ENC	Single	Load	Pixel write	Ignored	*
1	ENC	Single	Unload	Ignored	Code-block read	*
1	DEC	Single	Load	Code-block write	Ignored	*
1	DEC	Single	Unload	Ignored	Pixel read	*

** DACK acts as chip select (CS)*

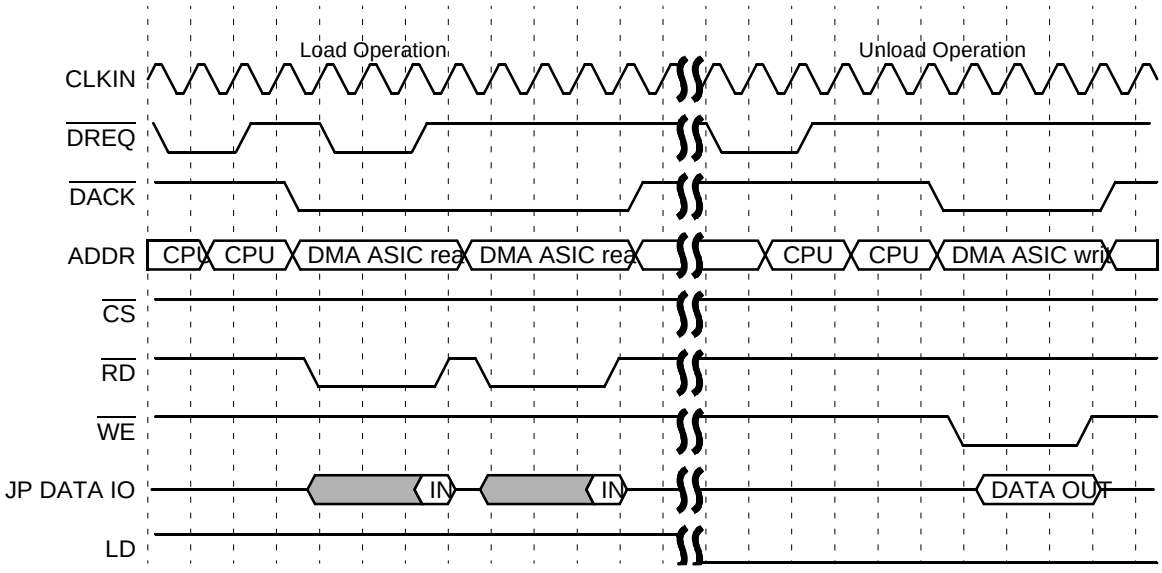


FIGURE 1. Example of Single-address DMA Operation

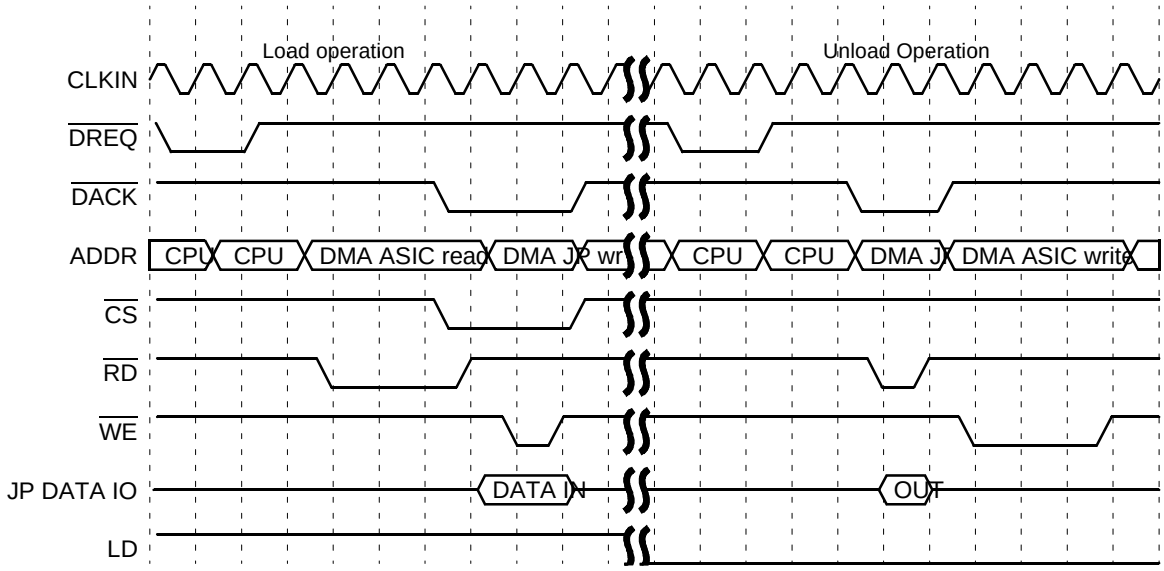


FIGURE 2. Example of Dual-address DMA Operation

The ADV-JP2000 also supports host initiated DMA by providing dedicated chip selects that allow direct access to both the Data and Attribute FIFOs without the requirement to provide an address. When this mode is enabled, DACK, and optionally DREQ, are used as chip selects for the two on-chip FIFOs. Two versions of host initiated DMA are available: 1) Single-Chip-Select, and 2) Dual-Chip-Select. For Single-Chip-Select mode, the DACK is used to access either FIFO as indicated by the Target bit in the DMA mode (DMODE) register. For Dual-Chip-Select mode, DACK is used to access the Data FIFO, and DREQ is used to access the Attribute FIFO.

Pin Descriptions

Name	Pins	I/O	Description
CLKIN	1	I	Input clock.
RESET	1	I	Reset. Causes the ADV-JP2000 to immediately reset and enter a low-power state.
DATA<15:0>	16	I/O	Bi-directional data bus.
ADDR<5:0>	6	I	Address bus.
DREQ	1	I or 0	Data transfer request pulse. This signal indicates that the ADV-JP2000 is ready to send or receive data. The actual direction of the data flow is implied by the mode and state of the ADV-JP2000. The duration of the active pulse is programmable through a mode register. The default pulse-width is two CLKIN periods. When Dual-Chip-Select mode is active, this pin is an input and is used to qualify accesses to the Attribute FIFO (Refer to “DMA Access Modes,” on page 5 for more details.)

Pin Descriptions

Name	Pins	I/O	Description
$\overline{\text{DACK}}$	1	I	Data transfer acknowledge. This is a signal from the host CPU that indicates that the data transfer request ($\overline{\text{DREQ}}$) has been acknowledge and that data will be transferred on the completion of the $\overline{\text{DACK}}$ period. When Single-Chip-Select mode is enabled, this pin is used to qualify accesses either the Data or Attribute FIFOs, depending on the Target bit in the DMA mode (DMODE) register. If Dual-Chip-Select mode is enabled, this pin is used to qualify accesses to the Data FIFO. (Refer to “DMA Access Modes,” on page 5 for more details.)
$\overline{\text{CS}}$	1	I	Chip select. This signal is used to qualify addressed read and write access to the ADV-JP2000.
$\overline{\text{WE}}$	1	I	Write Enable. This signal has two different functions depending on the DMA access mode, the current load-state of the ADV-JP2000 and the state of $\overline{\text{CS}}$. When $\overline{\text{WE}}$ is asserted in conjunction with an active $\overline{\text{CS}}$, then this signal functions as a normal write enable regardless of the load-state or DMA access mode. This will cause data present on DATA<15:0> to be written to the register addressed by ADDR<5:0>.
$\overline{\text{RD}}$	1	I	Read Enable. This signal has two different functions depending on the DMA access mode, the current load-state of the ADV-JP2000 and the state of $\overline{\text{CS}}$. When $\overline{\text{RD}}$ is asserted in conjunction with an active $\overline{\text{CS}}$, then this signal functions as a normal read enable regardless of the load-state or DMA access mode. This will cause the ADV-JP2000 to output data, from the register addressed by ADDR<5:0>, onto DATA<15:0>.
$\overline{\text{ACK}}$	1	O	Acknowledge. This signal indicates that the last register access was successful. Note: due to synchronization issues, control and status register accesses may incur an additional delay, so the host software should wait for acknowledgement from the ADV-JP2000. FIFO accesses, on the other hand, are guaranteed to occur immediately and do not need to be checked for acknowledge, provided that the timing constraints are observed.
$\overline{\text{IRQ}}$	1	O	Interrupt pin. This pin indicates that the ADV-JP2000 requires the attention of the host processor. This pin can be programmed to indicate the status of the internal interrupt conditions within the ADV-JP2000 such as FIFO over/under runs, end of processing or miscellaneous error conditions. The interrupt sources are enabled via bits in register IRQIE.
LD	1	O	ADV-JP2000 load-state status pin. This pin indicates that the ADV-JP2000 is loading data (LD = 1, being written to) or unloading data (LD = 0, being read from).
VDD	2	P	Positive supply for core
GND	2	G	Ground for core

Pin Descriptions

Name	Pins	I/O	Description
IOVDD	6	P	Positive supply for I/O.
IOGND	6	G	Ground for I/O

Register Descriptions

0x00 MODE Mode control register R/W

This register is used to set the ADV-JP2000's basic mode of operation.

Bits	Name	Description	Reset Value
0	SFTRST	Soft reset	1
1	ENC	Encode (compression) mode	1
2	START	Start encode or decode process, bit is cleared on completion	0
3	LOAD	Load-state; 1=load, 0=unload (read only)	1
15:4	*reserved*	Reserved for future use, always write 0; ignored unless NOAUTO is active	undefined

0x01 PMODE Pixel mode control register R/W

This register is used to set pixel/component formats.

Bit(s)	Name	Description	Reset Value
1:0	CMPMD	Component Mode	0
		0=Three-component YCbCr 4:2:2 interleaved mode. Y,Cb,Y,Cr...	
		1=Single-component only. This mode is useful for processing a luminance only tile.	
		2=Two-component interleaved mode. This is mode is useful for processing an interleaved chrominance tile Cb,Cr,Cb,Cr...	
		3=Undefined	
3:2	*reserved*	Reserved, always write 0	undefined
6:4	PCKMD	Packing mode	0
		0 = 8-bit unpacked (using DATA[7:0] only)	
		1 = 8-bit packed Y/Cr, Y/Cb	
		2 = 8-bit packed Y/Y and/or Cb/Cr	
		4 = 10-bit (using DATA[9:0])	
		7 = 14-bit raw (using DATA[15:2])	
		All other combinations may result in unexpected results.	
15:7	*reserved*	Reserved, always write 0	undefined

Examples of packing mode sequences:

PMODE	8-Bit Packing Formats	Component Packing Sequence (MSB/LSB, MSB/LSB...)
0x0010	Packed, 3-component, interleaved	Y*0*/Cb*0*, Y*1*/Cr*0*, Y*2*/Cb*2*, Y*3*/Cr*2*,...
0x0020	Packed, 3-component, alternating	Y*0*/Y*1*, Cb*0*/Cr*0*, Y*2*/Y*3*, Cb*2*/Cr*2*,...
0x0021	Packed, 1-component	Y*0*/Y*1*, Y*2*/Y*3*, Y*4*/Y*5*,...
0x0022	Packed, 2-component, interleaved	Cb*0*/Cr*0*, Cb*2*/Cr*2*, Cb*4*/Cr*4*,...

0x02 WMODE Wavelet mode control register R/W

This register is used to set the modes and formats for the wavelet processor.

Bit(s)	Name	Description	Reset Value
0	REV	Enable reversible transform mode 0=irreversible, 1= reversible In irreversible mode the 8 or 10-bit data is automatically msb justified for the wavelet process. The user may optionally specify up to two additional guard bits when this mode is enabled.	1
1	*reserved*	Reserved, always write 0	undefined
3:2	YDLEVEL	Luminance decomposition levels	3
4	*reserved*	Reserved, always write 0	undefined
6:5	CDLEVEL	Chrominance decomposition levels	3
9:7	*reserved*	Reserved, always write 0	undefined
10	YUNI	Luminance component format; 0=Bipolar, 1=Unipolar	0
11	CUNI	Chrominance component format; 0=Bipolar, 1=Unipolar	
13:12	*reserved*	Reserved, always write 0	undefined
15:14	GBITS	Number of guard bits. [0,1 or 2]	0

0x03 CMODE Code-block mode control register R/W

This register sets the modes and formats of code-block and code-block attribute generation.

Bit(s)	Name	Description	Reset Value
0	BYPASS	Enable arithmetic bypass mode	0
1	VCAUS	Enable Vertically stripe causal context	0
2	CPTERM	Termination mode; 0=after each code block, 1=after each pass	0
3	DMEN	Enable distortion metric output	0
4	RCEN	Enable running count for code-segment lengths	0
5	RSTCXT	Reset contexts after each coding pass	0
15:6	*Reserved*	Reserved for future use; always write 0	undefined

0x04 DMODE DMA mode control register R/W

This register sets the DMA mode and target/source location of DMA accesses.

Bit(s)	Name	Description	Reset Value
0	ENABLE	Enable DMA	0
1	SDMA	Single address DMA mode enable	0
2	TARG	DMA target; 0=Data FIFO, 1=Attribute FIFO	0
3	*reserved*	Reserved for future use; always write 0	undefined
7:4	DRQPLEN	$\overline{\text{DREQ}}$ pulse width. $\overline{\text{DREQ}}$ will have an active pulse width of DRQPLEN cycles. If DRQPLEN = 0, then the pulse width will be 32 cycles. NOTE: This count is referenced to the internal clock.	8
8	CSMODE	Chip-Select FIFO access	0
9	DCS-MODE	Dual-Chip-Select FIFO access	0
15:8	*reserved*	Reserved for future use; always write 0	undefined

0x05 HSIZE Tile Horizontal Size R/W

Tile horizontal dimension.

Bit(s)	Name	Description	Reset Value
8:0	HSIZE	Tile Horizontal size	0
15:9	*reserved*	Reserved for future use; always write 0	undefined

For three-component interleaved pixel format (4:2:2), HSIZE should be set to the horizontal dimension of the luminance tile. For two-component interleaved chrominance, HSIZE is the combined size of the two components. (Ex. if Cb and Cr are both 128 x 256 tiles, then the total HSIZE will be 256 (128 x 2).

0x06 VSIZE Tile Vertical Size R/W

Tile vertical dimension.

Bit(s)	Name	Description	Reset Value
8:0	VSIZE	Tile vertical size	0
15:9	*reserved*	Reserved for future use; always write 0	undefined

0x07 IRQIE Interrupt enables R/W

This register is used to enable the conditions that will cause an interrupt to occur.

Bits	Name	Description	Reset Value
0	DRDY	Indicates that the data can now be read from the ADV-JP2000. Encode: the first code-block word has been written to the data FIFO. Decode: the first uncompressed word has been written to the data FIFO.	0
1	TENDI	Indicates that the ADV-JP2000 has received all data necessary to process the current tile. Only applicable during load (i.e., LOAD=1) Encode: the wavelet processor has received the last uncompressed word from the data FIFO. Decode: the entropy CODEC has received the last code-block from the data FIFO.	0
2	TENDO	Indicates that the last word of a tile has been written to the FIFO by the ADV-JP2000. Only applicable during unload (i.e., LOAD=0) Encode: the entropy CODEC has written the last code-block to the data FIFO. Decode: the wavelet processor has written the last uncompressed word to the data FIFO.	0
3	TOUT	Indicates that the last word of the tile has been read by the host CPU. Encode: If data is being read from the Data FIFO, then TOUT will fire when the host reads the last code-word of the tile. If data is being read from the Attribute FIFO, then TOUT will fire when the host reads the last attribute of the tile. Decode: If data is being read from the Data FIFO, then TOUT will fire when the host reads the last word of the uncompressed tile.	0
4	CBEND	Indicates that a code block boundary has been reached Encode: a code-block boundary has been reached and the host software should retrieve the code-block attribute data. Decode: a code-block boundary has been reached and the host software should send, or have already sent, attribute data for the next code-block.	0
5	TRANS	Processing of the data being loaded has been completed	0
6	DFTH	Data FIFO threshold has been tripped.	0
7	AFTH	Attribute FIFO threshold has been tripped.	0
8	DFERR	Data FIFO has overflowed or underflowed.	0
9	AFERR	Attribute FIFO has overflowed or underflowed.	0
10	CAERR	Code-block attribute error	0
11	ACERR	Arithmetic coder overflow	0
12	TSZERR	Tile size error; number of pixel components loaded does not match tile size.	0

Bits	Name	Description	Reset Value
14:13	*reserved*	Reserved for future use; always write 0	undefined
15	FERR	The ADV-JP2000 has encountered an unexpected fatal error	0

0x08 IRQFLG Interrupt flags RO/WO

This register indicates which interrupt conditions are currently active. The bits in this register correspond directly to the bits in the interrupt enable register (IRQIE). Individual interrupts are cleared by writing a 1 in the proper bit position of this register (i.e., “Write 1 to clear”.)

0x09 MIRQFLG Masked interrupt flags RO

This register indicates which of the enabled interrupt conditions are currently active (i.e., this is the equivalent of and-ing IRQIE with IRQFLG.)

0x0A DFCNT Data FIFO count RO

This register indicates the number of valid items currently in the Data FIFO.

Bits	Name	Description	Reset Value
6:0	DCOUNT	Indicates the number of valid items currently in the Data FIFO.	0
15:7	*reserved*	Reserved for future use; always write 0	undefined

0x0B DFTHR Data FIFO threshold R/W

This register contains the Data FIFO threshold. This register sets the full/empty threshold of the Data FIFO. The full/empty status of the Data FIFO is indicated in the IRQFLG register. When data is being read from the ADV-JP2000, the status will be set high whenever the number of **valid** entries in the FIFO is greater then, or equal to, the threshold. When data is being written to the ADV-JP2000, the status will be set high whenever the number of **empty** entries in the FIFO is greater then, or equal to, the threshold.

Bits	Name	Description	Reset Value
6:0	DFTHR	Data FIFO threshold	0
15:7	*reserved*	Reserved for future use; always write 0	undefined

0x0C AFCNT Attribute FIFO count RO

This register indicates the number of valid items currently in the Attribute FIFO. This register’s function is identical to DFCNT.

Bits	Name	Description	Reset Value
6:0	ACOUNT	Indicates the number of valid items currently in the Attribute FIFO.	0
15:7	*reserved*	Reserved for future use; always write 0	undefined

0x0D AFTHR Attribute FIFO threshold R/W

This register contains the Attribute FIFO threshold. This registers's function is identical to DFTHR.

Bits	Name	Description	Reset Value
6:0	ATHRESH	Attribute FIFO threshold	0
15:7	*reserved*	Reserved for future use; always write 0	undefined

0x0E TEST Test Register

Writing to this location may cause unexpected results. Data read from these location is undefined and may yield different results from chip to chip.

Bits	Name	Description	Reset Value
15:0	*reserved*	ADI TEST ONLY	undefined

0x0F VERSION Chip revision register RO

This register contains version identifier.

Bits	Name	Description	Reset Value
7:0	VERSION	Version ID	N/A
15:8	*reserved*	Reserved for future use	undefined

0x10-0x19 LQFACT Luminance Quantizer Factors R/W

Bits	Name	Description (ENCODE)	Reset Value
11:0	MANT	Mantissa (μ_b)	undefined
15:12	EXP	Exponent (ε_b)	undefined

Bits	Name	Description (DECODE)	Reset Value
10:0	MANT	Mantissa (μ_b)	undefined
15:11	EXP	Exponent (ε_b)	undefined

These registers contain the luminance, or single component, quantization or dequantization factors for Encode and Decode respectively. Refer to Annex E, Quantization, in the JPEG2000 specification for a detailed definition of these parameters. For Decode, these values are identical to the step-size parameters, ε_b and μ_b, as defined in the JPEG2000 bit stream. In Encode, these registers must be programmed with the inverse step-size. A detailed description of the quantization and dequantization process can be found in Appendix A of this document.

There is one register for each Mallat block of the wavelet transform. The number of registers needed and the order of their appearance in this list is based on the number of levels of wavelet transform. If the ADV-JP2000 is processing interleaved pixel component data, then the same set of quantizer factors will be used for both components. The registers are ordered as follows, where N_L represents the Nth decomposition level:

N_LLL, N_LHL, N_LLH, N_LHH, N_L-*1*HL, N_L-*1*LH, N_L-*1*HH,... *1*HL, *1*LH, *1*HH

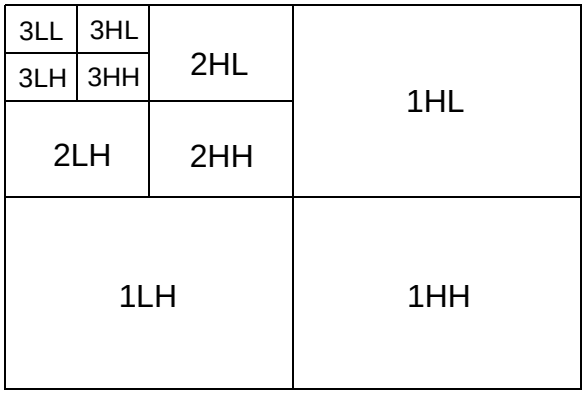


FIGURE 3. Mallat Block Identification (3-level transform)

0x1A-0x23 CBQFACT Cb Chrominance Quantizer Factors R/W

Bits	Name	Description (ENCODE)	Reset Value
11:0	MANT	Mantissa (μ_b)	undefined
15:12	EXP	Exponent (ε_b)	undefined

Bits	Name	Description (DECODE)	Reset Value
10:0	MANT	Mantissa (μ_b)	undefined
15:11	EXP	Exponent (ε_b)	undefined

These registers contain the Cb chrominance quantization or dequantization factors for Encode and Decode respectively. These have the same function and ordering as LQFACT, described above.

0x24-0x2D CRQFACT Cr Chrominance Quantizer Factors R/W

Bits	Name	Description (ENCODE)	Reset Value
11:0	MANT	Mantissa (μ_b)	undefined
15:12	EXP	Exponent (ε_b)	undefined

Bits	Name	Description (DECODE)	Reset Value
10:0	MANT	Mantissa (μ_b)	undefined
15:11	EXP	Exponent (ε_b)	undefined

These registers contain the Cr chrominance quantization or dequantization factors for Encode and Decode respectively. These have the same function and ordering as LQFACT, described above.

0x2E-39 Reserved for future use

Writing to these locations may cause unexpected results. Data read from these location is undefined and may yield different results from chip to chip.

0x3A CTSIZEM Compressed tile size (MSW). RO

Contains the most significant word (MSW) of the compressed tile size in bytes. Encode only.

Bits	Name	Description	Reset Value
15:0	CTSIZEM	The number of bytes in the last compressed tile. This number is only valid upon completion of the entropy coding process as indicated by the TEND or TOUT interrupt.	0

0x3B CTSIZEL Compressed tile size (LSW) RO

Contains the least significant word (LSW) of compressed tile size in bytes. Encode only.

Bits	Name	Description	Reset Value
15:0	CTSIZEL	The number of bytes in the last compressed tile. This number is only valid upon completion of the entropy coding process as indicated by the TEND or TOUT interrupt.	0

0x3D DFIFO Data FIFO R/W

This address is not used to access a register directly. This register provides a mechanism to allow access to the Data FIFO via a normal addressed access instead of a DMA access. *(See "Data FIFO Formats," on page 2 for a description of the data formats found in this register.)*

0x3E AFIFO Code-block Attribute FIFO R/W

This address is not used to access a register directly. This register provides a mechanism to allow access to the Attribute FIFO via a normal addressed access instead of a DMA access. *(See "Code-block Attribute Formats," on pag e3 for a description of the data formats found in this register.)*

0x3F PLLCTRL PLL control register R/W

This register is used to configure the ADV-JP2000's on-chip phase locked loop.

Bits	Name	Description	Reset Value
2:0	PLLMD	Multiplier 1 = 2X, 3=4X, 7=8X, all other values are illegal	1
3	BYPASS	Bypass PLL, Internal clock = 1/2 CLKIN	0
4	CDOUBLE	Clock doubler (additional 2X multiplier)	1
5	CHALVE	Clock divider (additional 2X divider)	0
6	PDN	Power down	0
7	SM	Scantest mode	0
15:8	*reserved*	Reserved for future use; always write 0	undefined

The default configuration for the PLL is set to generate an internal clock that is 4 times the frequency of the CLKIN pin.

Specifications

Specifications subject to change without notice.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vdd_{core}	DC supply voltage, core	1.35	1.98	V
$Vdd_{I/O}$	DC supply voltage, I/O	2.97	3.63	V
V_{Input}	Input range	-0.3	3.6	V
Temp	Operating ambient temperature range in free air	0	70	^{o}C

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage	VDD = max	2.0	-	-	V
V_{IL}	Lo-Level Input Voltage	VDD = min	-	-	0.8	V
V_{OH}	Hi-Level Output Voltage	VDD = min, I_{OH} = -0.5mA	2.4	-	-	V
V_{OL}	Lo-Level Output Voltage	VDD = min, I_{OL} = 2mA	-	-	0.4	V
I_{IH}	Hi-Level Input Current	VDD = max, V_{IN} = VDD	-	TBD	-	uA
I_{IL}	Lo-Level Input Current	VDD = max, V_{IN} = 0v	-	TBD	-	uA
I_{OZH}	Three-State Leakage Current	VDD = max, V_{IN} = VDD	-	TBD	-	uA
I_{OZL}	Three-State Leakage Current	VDD = max, V_{IN} = 0v	-	TBD	-	uA
I_{DD}	Supply Current (Power Down)	VDD = max	-	-	100	uA
I_{DD}	Supply Current (Active)	VDD = max	-	-	100	mA
C_I	Input Pin Capacitance		-	-	8	pF
C_O	Output Pin Capacitance		-	-	8	pF

Timing Characteristics

TABLE 2. CLKIN and $\overline{\text{RESET}}$

Parameter	Comments	Min	Typ	Max	Unit
tCLK	CLKIN period	33.3	-	50.0	nS
tCLKL	CLKIN Width Low	10	-	-	nS
tCLKH	CLKIN Width High	10	-	-	nS
tRST	$\overline{\text{RESET}}$ Width Low	5tCLK	-	-	nS

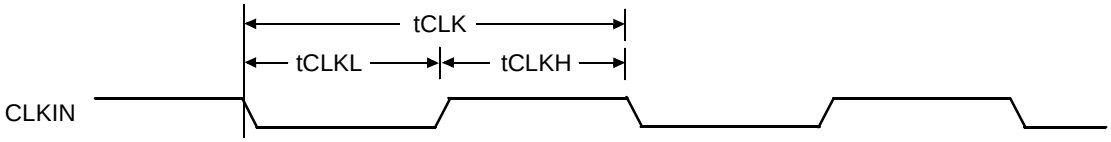


FIGURE 4. CLKIN

TABLE 3. Read Operation (internal registers only, does not apply to FIFO accesses)

Parameter	Comments	Min	Typ	Max	Unit
tDRD	Read access time	23.5	-	32.7	nS
tHZRD	Data hold	-	-	5	nS
tSC	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ setup	0	-	-	nS
tSA	Address setup	2	-	-	nS
tHC	$\overline{\text{CS}}$ hold	0	-	-	nS
tHA	Address hold	0	-	-	nS
tRH	Read inactive pulse width	18.5	-	-	nS
tRL	Read active pulse width	33	-	-	nS
tRC	Read Cycle time	51.5	-	-	nS

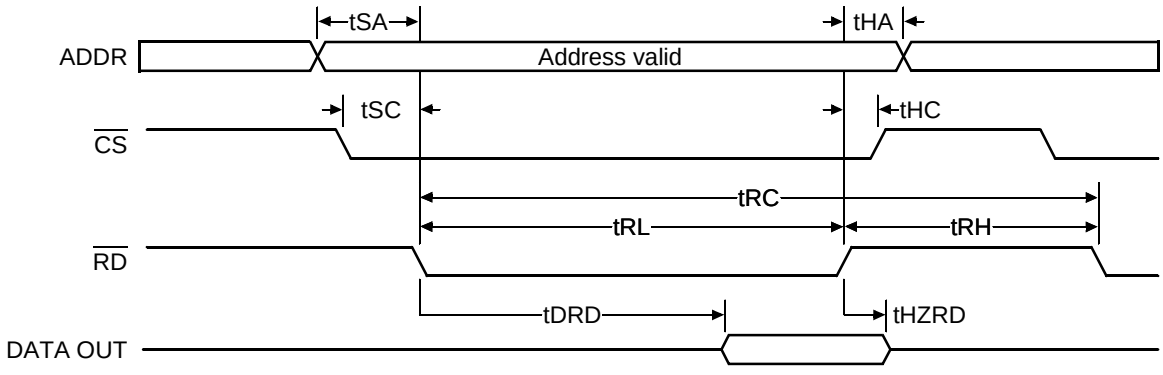


FIGURE 5. Read Operation

TABLE 4. Write Operation (internal registers only, does not apply to FIFO accesses)

Parameter	Comments	Min	Typ	Max	Unit
tSD	Data setup	2	-	-	nS
tHD	Data hold	1	-	-	nS
tSC	$\overline{CS}$ to $\overline{WE}$ setup	0	-	-	nS
tSA	Address setup	2	-	-	nS
tHC	$\overline{CS}$ hold	0	-	-	nS
tHA	Address hold	0	-	-	nS
tWH	Write inactive pulse width	18.5	-	-	nS
tWL	Write active pulse width	18.5	-	-	nS
tWC	Write Cycle time	37	-	-	nS

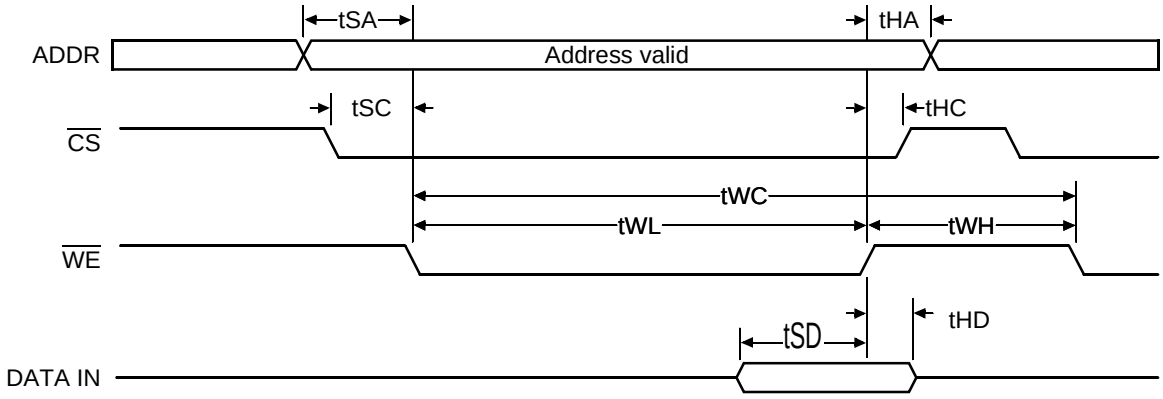


FIGURE 6. Write Operation

TABLE 5. Single-address DMA Write Operation (applies to FIFO accesses only.)

Parameter	Comments	Min	Typ	Max	Unit
tSD	Data setup	2	-	-	nS
tHD	Data hold	1	-	-	nS
tSC	$\overline{CS}$ to $\overline{RD}$ setup	0	-	-	nS
tSA	Address setup	2	-	-	nS
tHC	$\overline{CS}$ hold	0	-	-	nS
tHA	Address hold	0	-	-	nS
tWH	Write inactive pulse width	18.5	-	-	nS
tWL	Write active pulse width	18.5	-	-	nS
tWC	Write Cycle time	37	-	-	nS

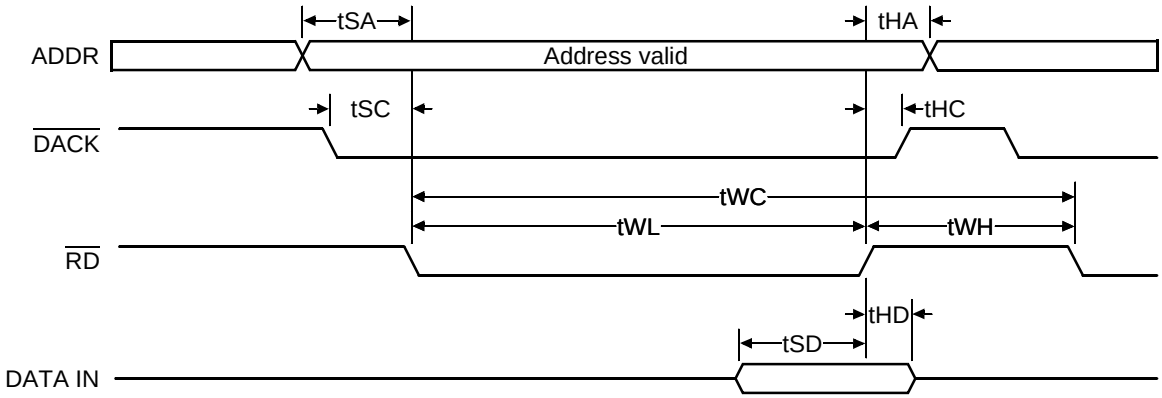


FIGURE 7. Single-address DMA Write Operation

TABLE 6. Single-address DMA Read Operation (applies to FIFO accesses only.)

Parameter	Comments	Min	Typ	Max	Unit
tDRD	Data access	5	-	-	nS
tHZRD	Data hold	-	-	5	nS
tSC	$\overline{CS}$ to $\overline{RD}$ setup	0	-	-	nS
tSA	Address setup	2	-	-	nS
tHC	$\overline{CS}$ hold	0	-	-	nS
tHA	Address hold	0	-	-	nS
tRH	Read inactive pulse width	18.5	-	-	nS
tRL	Read active pulse width	18.5	-	-	nS
tRC	Read Cycle time	37	-	-	nS

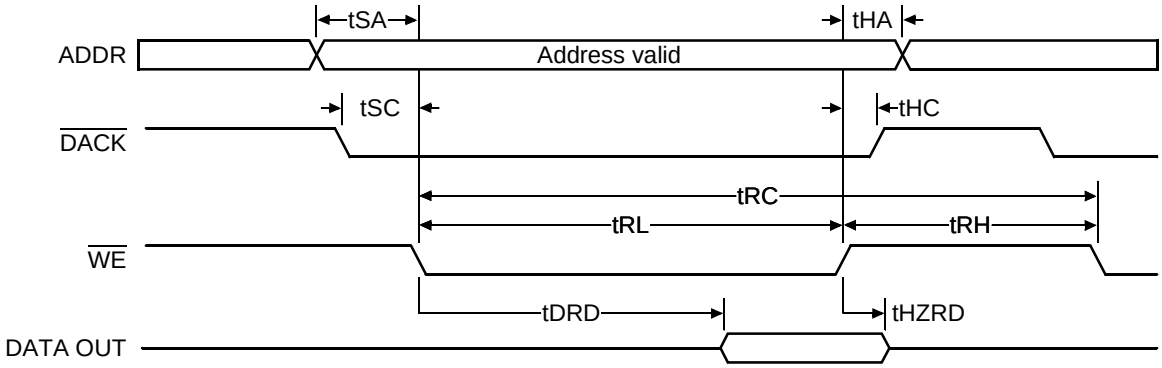


FIGURE 8. Single-address DMA Read Operation

TABLE 7. Chip-Select mode DMA Write Operation (applies to FIFO accesses only.)

Parameter	Comments	Min	Typ	Max	Unit
tSD	Data setup	2	-	-	nS
tHD	Data hold	1	-	-	nS
tSC	$\overline{CS}$ to $\overline{RD}$ setup	0	-	-	nS
tHC	$\overline{CS}$ hold	0	-	-	nS
tWH	Write inactive pulse width	18.5	-	-	nS
tWL	Write active pulse width	18.5	-	-	nS
tWC	Write Cycle time	37	-	-	nS

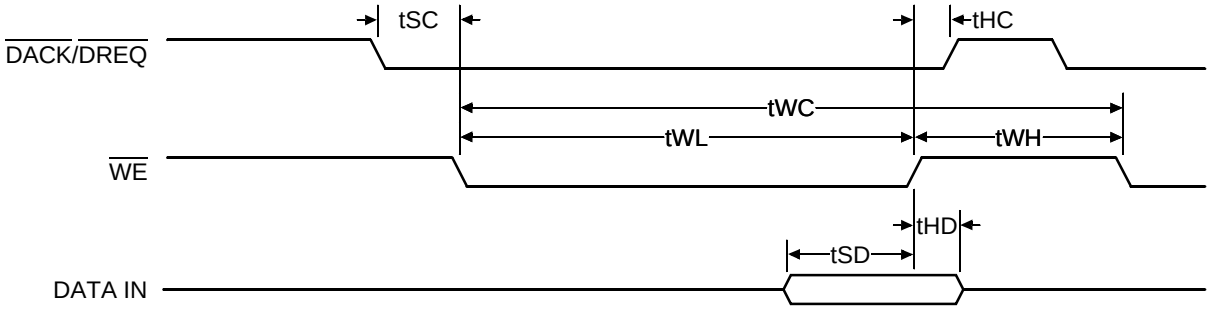


FIGURE 9. Chip-Select mode DMA Write Operation

TABLE 8. Chip-Select mode DMA Read Operation (applies to FIFO accesses only.)

Parameter	Comments	Min	Typ	Max	Unit
tDRD	Data access	5	-	-	nS
tHZRD	Data hold	-	-	5	nS
tSC	$\overline{CS}$ to $\overline{RD}$ setup	0	-	-	nS
tHC	$\overline{CS}$ hold	0	-	-	nS
tRH	Read inactive pulse width	18.5	-	-	nS
tRL	Read active pulse width	18.5	-	-	nS
tRC	Read Cycle time	37	-	-	nS

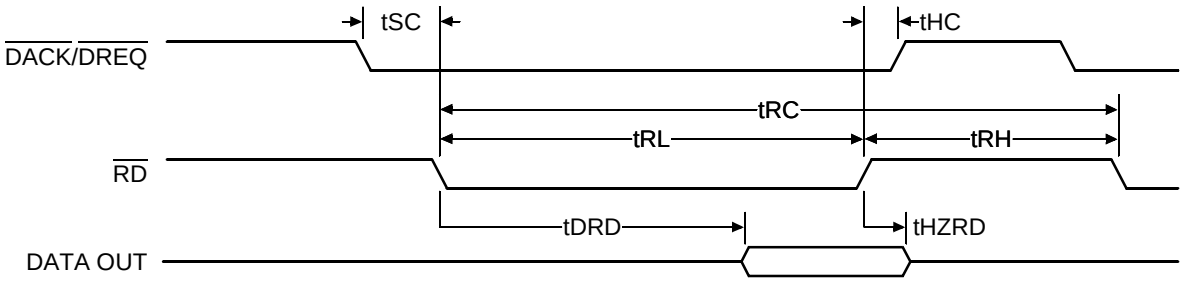
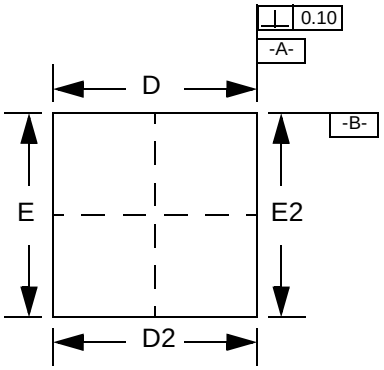


FIGURE 10. Chip-Select mode DMA Read Operation

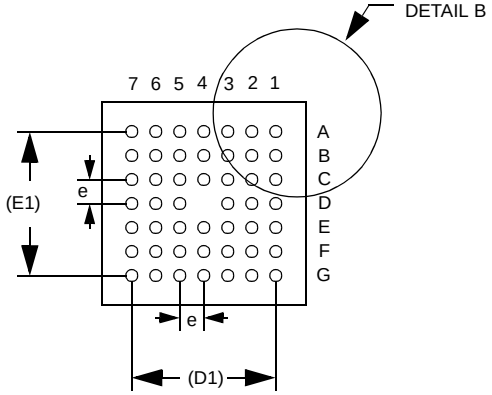
Pin Assignments
7x7mm 48-Lead fpBGA 0.80mm pitch

#	Pin name	#	Pin name	#	Pin name	#	Pin name
A1	ADDR5	B6	$\overline{CS}$	D5	$\overline{WE}$	F3	IOVSS
A2	ADDR0	B7	IOVSS	D6	VDD	F4	$\overline{RESET}$
A3	$\overline{ACK}$	C1	DATA14	D7	VSS	F5	IOVDD
A4	IOVDD	C2	DATA15	E1	DATA13	F6	DATA6
A5	$\overline{DREQ}$	C3	ADDR4	E2	DATA12	F7	IOVDD
A6	$\overline{RD}$	C4	ADDR1	E3	CLKIN	G1	VDD
A7	DATA0	C5	DATA1	E4	DATA7	G2	IOVDD
B1	ADDR3	C6	IOVDD	E5	DATA4	G3	DATA9
B2	ADDR2	C7	DATA2	E6	IOVSS	G4	LD
B3	$\overline{IRQ}$	D1	IOVDD	E7	DATA3	G5	DATA8
B4	IOVSS	D2	IOVSS	F1	VSS	G6	IOVSS
B5	$\overline{DACK}$	D3	DATA10	F2	DATA11	G7	DATA5

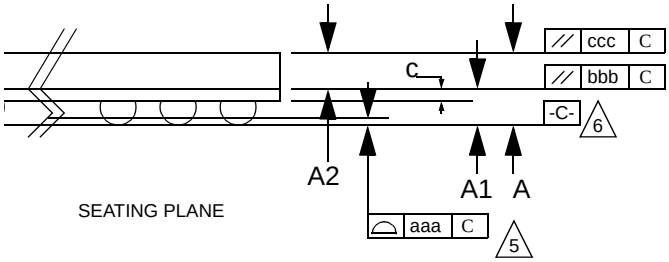
48-LEAD fpBGA 7x7mm
0.80mm ball pitch



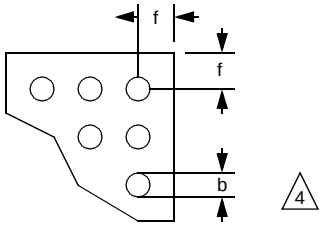
TOP VIEW



BOTTOM VIEW



SEATING PLANE



DETAIL B

DIMENSIONAL REFERENCES			
REF	**MIN**	**NOM**	**MAX**
A	1.00 (1.15)	1.10 (1.25)	1.20 (1.35)
A1	0.10 (0.25)	0.15 (0.30)	0.20 (0.35)
A2	0.65	0.70	0.75
D	6.80	7.00	7.20
D1		4.80 BSC	
D2	6.80	7.00	7.20
E	6.80	7.00	7.20
E1		4.80 BSC	
E2	6.80	7.00	7.20
b	0.25 (0.35)	0.30 (0.40)	0.35 (0.45)
c		0.25	
aaa			0.15
bbb			0.20
ccc			0.25
e	0.725	0.80	0.875
f	1.00	1.10	1.20
M		7	
N		48	

Notes:

1. All dimensions are in millimeters
2. 'e' Represents the basic solder ball grid pitch
3. 'M' Represents the basic solder ball matrix size.
4. 'b' is measurable at the maximum solder ball diameter
5. Dimension 'ccc' is measured parallel to primary datum -C-
6. Primary datum -C- and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be matte finish
8. Package centering to substrate shall be 0.0750 mm max.
9. Package warp shall be 0.050 mm maximum
10. Substrate material base is BT resin
11. The overall package thickness 'A' already considers collapse balls