0.5 Micron CMOS Pad Library Datasheets
AMI500HXPF 5.0 Volt
Section 4
Revision 1.1

Input Drive Pieces

Pull Pieces

Output Drive Pieces

Selection Guide

AMI500HXPF 0.5 micron CMOS Pad Library

Power Pad Cells

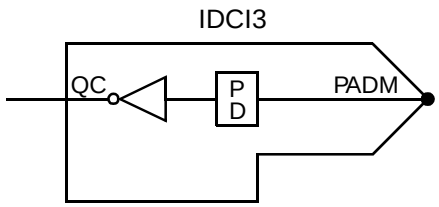
Special Pad Cells

DATASHEETS

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	5.80 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	20.149	nA
EQL_{pd}	12.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.589 0.767	0.680 0.872	0.769 0.980	0.845 1.076	0.925 1.179

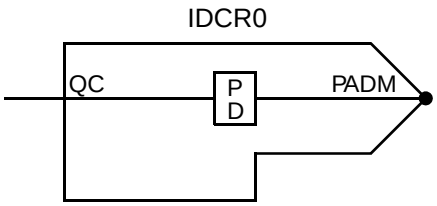
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	5.80 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.488	nA
EQL_{pd}	1.4	Eq-load

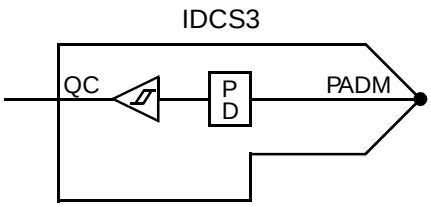
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	5.80 pF

HDL Syntax

Verilog ..... IDCS3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.590	nA
EQL_{pd}	16.3	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.470 1.000	1.584 1.165	1.683 1.271	1.762 1.349	1.839 1.422

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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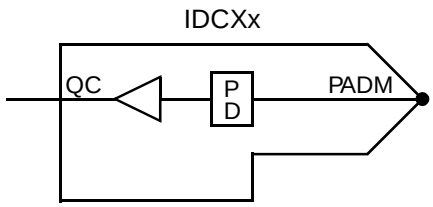
Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	5.80	5.80

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	0.0	19.459	9.8
IDCX6	0.0	22.384	17.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

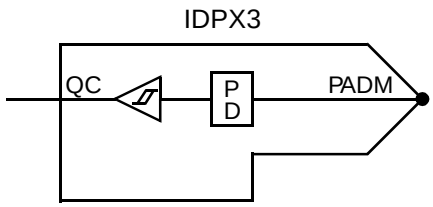
	Number of Equivalent Loads		1	11	22	32	43 (max)
IDCX3	From: PADM To: QC	t_{PLH} t_{PHL}	0.762 0.583	0.856 0.686	0.953 0.798	1.037 0.894	1.128 0.992
	Number of Equivalent Loads		**1**	**11**	**22**	**32**	**43 (max)**
IDCX6	From: PADM To: QC	t_{PLH} t_{PHL}	0.628 0.527	0.669 0.642	0.723 0.705	0.776 0.748	0.838 0.788

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load
	IDPX3
PADM (pF)	5.80

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	0.0	19.401	11.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
IDPX3	From: PADM	t_{PLH}	0.599	0.758	0.864	0.941	1.016
	To: QC	t_{PHL}	0.753	0.860	0.955	1.043	1.141

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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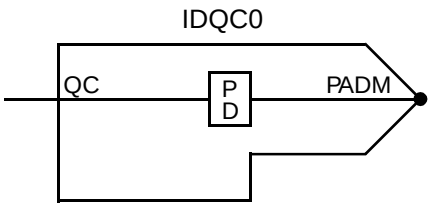
Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	5.80 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);
VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.488	nA
EQL_{pd}	1.3	Eq-load

See page 2-13 for power equation.

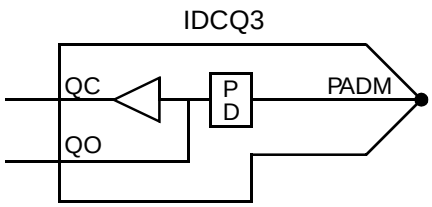
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

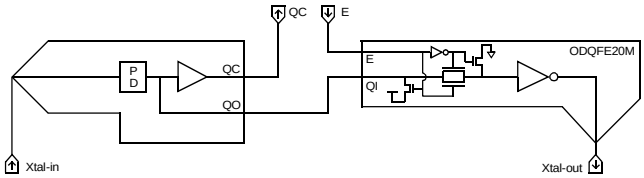
Description

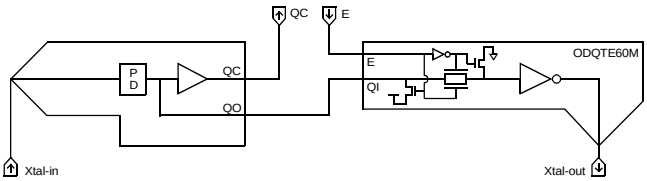
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	5.80 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.459	nA
EQL_{pd}	10.9	Eq-load

See page 2-13 for power equation.

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Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.773 0.522	0.854 0.681	0.949 0.788	1.031 0.885	1.113 0.998
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

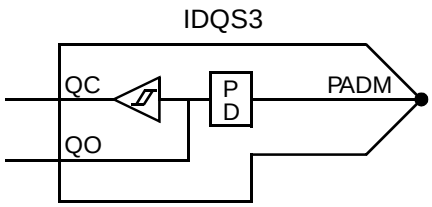
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

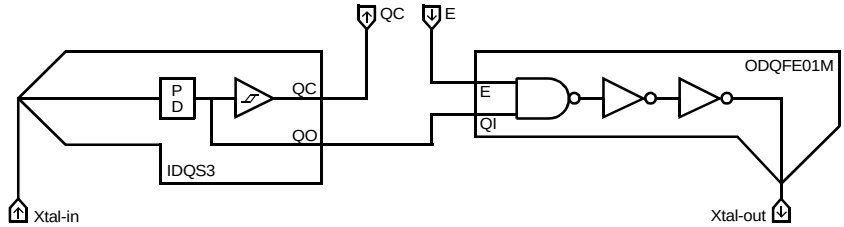
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load	
PADM	5.80	pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.590	nA
EQL_{pd}	17.4	Eq-load

See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.497 1.065	1.594 1.156	1.688 1.272	1.768 1.385	1.853 1.514
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

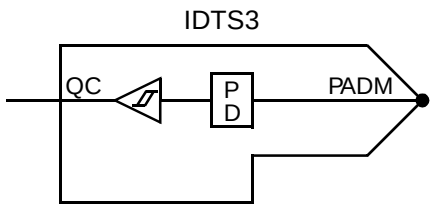
Design Notes:

The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

Description

IDTS3 is a non-inverting, TTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	5.80 pF

HDL Syntax

Verilog ..... IDTS3 inst_IDTS3 (QC, PADM);
VHDL..... inst_IDTS3 : IDTS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.078	nA
EQL_{pd}	15.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.884 1.598	0.961 1.789	1.063 1.936	1.163 2.045	1.280 2.147

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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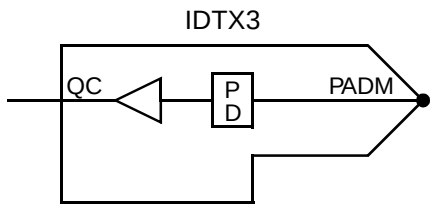
Description

IDTXx is a family of non-inverting, TTL-level, input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDTXx *inst_name (*QC, PADM);
VHDL..... *inst_name*: IDTXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDTX3	IDTX6
PADM (pF)	5.80	5.80

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDTX3	0.0	18.976	9.7
IDTX6	0.0	21.419	17.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

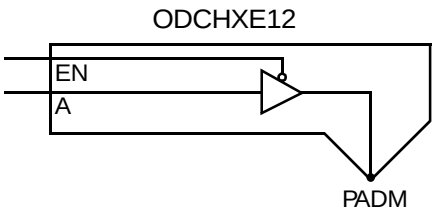
IDTX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.532 0.669	0.657 0.830	0.752 0.962	0.837 1.059	0.931 1.147
IDTX6	Number of Equivalent Loads		1	21	42	62	83 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.478 0.639	0.599 0.813	0.697 0.902	0.780 1.005	0.863 1.141

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCHXE12 is a high performance, 12 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.0 eql
EN	5.8 eql
PADM	5.82 pF

HDL Syntax

Verilog ..... ODCHXE12 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE12 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	69.357	nA
EQL_{pd}	298.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.055 1.162	1.676 1.731	2.544 2.617	4.268 4.400	6.033 6.109
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.953 0.929 0.897 1.072	 1.513 1.691	 2.386 2.594	 4.129 4.338	 5.873 6.118

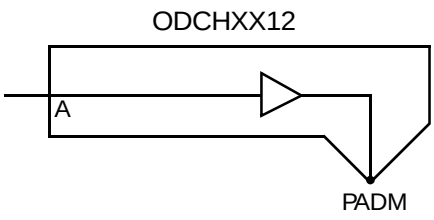
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODCHXX12 is a high performance, 12 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.0 eql

HDL Syntax

Verilog ..... ODCHXX12 *inst_name* (PADM, A);
VHDL..... *inst_name*: ODCHXX12 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	61.472	nA
EQL_{pd}	250.7	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

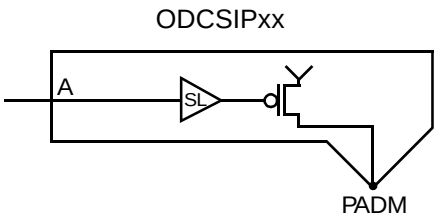
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.621 0.779	1.255 1.413	2.141 2.299	3.867 4.042	5.621 5.813

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCSIPxx is a family of 4 to 12 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSIP04	ODCSIP08	ODCSIP12
A (eq-load)	3.5	3.5	3.5
PADM (pF)	5.81	5.81	5.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	66.889	223.1
ODCSIP08	8	66.889	237.5
ODCSIP12	12	66.889	252.0

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.601	6.241	11.428	21.782	32.158
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.716	3.611	6.278	11.550	16.902
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.757	2.720	4.443	7.978	11.432

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

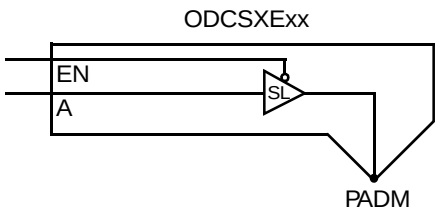
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Cell		
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**
A	PADM	t_{HZ}	0.752	1.006	1.260

Description

ODCSXExx is a family of 4 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSXE04	ODCSXE08	ODCSXE12
A (eq-load)	1.9	1.9	1.9
EN (eq-load)	6.6	6.6	6.6
PADM (pF)	5.81	5.81	5.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	68.376	253.2
ODCSXE08	8	68.376	275.2
ODCSXE12	12	68.376	297.0

a. See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	3.278 3.181	6.855 6.932	11.602 12.311	20.690 23.028	29.573 33.682
	From: EN To: PADM	t_{ZH} t_{ZL}	2.920 2.949	6.512 6.696	11.290 12.078	20.363 22.813	29.252 33.477
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	2.306 2.320	4.206 4.127	6.867 6.690	11.900 11.910	16.512 17.269
	From: EN To: PADM	t_{ZH} t_{ZL}	1.889 2.059	3.824 3.858	6.548 6.444	11.541 11.777	16.187 16.963
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	2.005 2.082	3.265 3.229	5.093 4.977	8.573 8.603	11.851 12.001
	From: EN To: PADM	t_{ZH} t_{ZL}	1.731 1.764	2.962 3.036	4.685 4.825	8.208 8.345	11.472 11.871

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

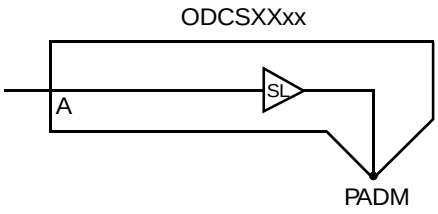
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12
EN	PADM	t_{HZ} t_{LZ}	0.788 0.927	1.043 1.098	1.298 1.267

Description

ODCSXXxx is a family of 4 to 12 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSXX04	ODCSXX08	ODCSXX12
A (eq-load)	8.9	8.9	8.9

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	64.722	232.2
ODCSXX08	8	64.722	254.1
ODCSXX12	12	64.722	276.0

a. See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

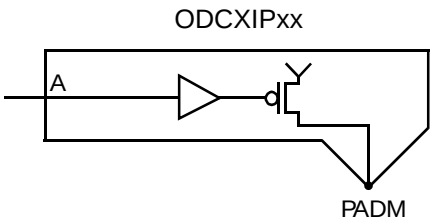
ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.363 2.570	5.996 6.298	11.140 11.610	21.074 22.288	30.723 33.033
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.528 1.550	3.365 3.397	6.017 6.081	11.305 11.268	16.548 16.580
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.341 1.411	2.539 2.638	4.269 4.390	7.725 7.885	11.234 11.414

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCXIPxx is a family of 1 to 12 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
A (eq-load)	2.2	2.2	2.2	3.3	3.3
PADM (pF)	5.80	5.80	5.81	5.81	5.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	56.213	183.1
ODCXIP02	2	56.732	188.3
ODCXIP04	4	57.280	198.1
ODCXIP08	8	58.348	215.5
ODCXIP12	12	59.415	231.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXIP01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{ZH}	4.489	6.578	8.659	11.781	16.996

AMI500HXPF 0.5 micron CMOS Pad Library

ODCXIP02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{ZH}	2.535	6.178	8.772	11.361	16.532
ODCXIP04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.827	3.522	6.084	11.283	16.422
ODCXIP08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.300	2.258	3.568	6.258	8.881
ODCXIP12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.151	1.872	2.793	4.533	8.881

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

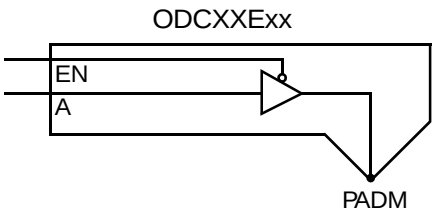
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
APADM		t_{HZ}	0.831	0.824	1.071	1.432	1.670

Description

ODCXXExx is a family of 1 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
A (eq-load)	5.1	7.3	7.3	1.9	1.9
EN (eq-load)	3.4	4.7	4.7	4.7	4.7
PADM (pF)	5.80	5.81	5.81	5.81	5.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	57.526	189.5
ODCXXE02	2	59.041	199.4
ODCXXE04	4	59.041	211.7
ODCXXE08	8	65.574	260.9
ODCXXE12	12	65.574	281.1

a. See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	4.489 4.969	6.606 7.102	8.717 9.229	11.853 12.430	17.003 17.808
	From: EN To: PADM	t_{ZH} t_{ZL}	4.652 4.884	6.776 6.991	8.870 9.121	11.976 12.348	17.088 17.782
ODCXXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.466 2.724	6.029 6.451	8.633 9.107	11.234 11.777	16.395 17.167
	From: EN To: PADM	t_{ZH} t_{ZL}	2.748 2.760	6.315 6.505	8.888 9.133	11.482 11.782	16.711 17.214
ODCXXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.602 1.844	3.446 3.752	6.062 6.430	11.218 11.771	16.396 17.134
	From: EN To: PADM	t_{ZH} t_{ZL}	1.790 1.823	3.585 3.726	6.211 6.428	11.436 11.795	16.510 17.126
ODCXXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.775 1.611	2.813 2.529	4.161 3.835	6.717 6.463	9.485 9.087
	From: EN To: PADM	t_{ZH} t_{ZL}	1.541 1.397	2.529 2.364	3.840 3.725	6.481 6.371	9.174 8.922
ODCXXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.700 1.577	2.389 2.234	3.340 3.130	5.128 4.863	6.811 6.648
	From: EN To: PADM	t_{ZH} t_{ZL}	1.452 1.421	2.162 2.067	3.049 2.953	4.785 4.726	6.568 6.504

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

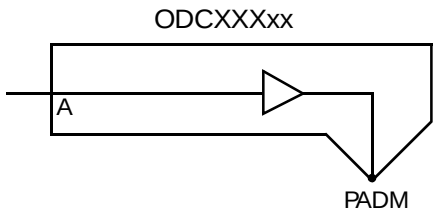
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
EN	PADM	t_{HZ} t_{LZ}	1.210 0.439	1.110 0.418	1.596 0.609	1.283 1.167	1.639 1.390

Description

ODCXXXxx is a family of 1 to 12 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12
A (eq-load)	3.8	3.8	5.7	7.8	7.7

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	56.116	183.9
ODCXXX02	2	56.116	190.1
ODCXXX04	4	57.153	202.3
ODCXXX08	8	58.247	227.5
ODCXXX12	12	58.247	247.7

a. See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

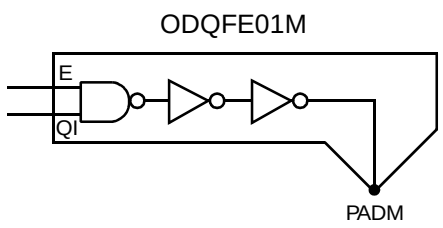
ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.430 4.763	6.515 6.896	8.598 9.032	11.722 12.241	16.925 17.601
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.514 2.709	6.107 6.406	8.701 9.079	11.298 11.772	16.469 17.203
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.460 1.609	3.272 3.480	5.868 6.155	11.020 11.503	16.202 16.849
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.205 1.221	2.140 2.182	3.472 3.515	6.130 6.109	8.774 8.756
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To PADM	t_{PLH} t_{PHL}	1.110 1.283	1.811 1.981	2.741 2.982	4.488 4.923	6.235 6.806

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

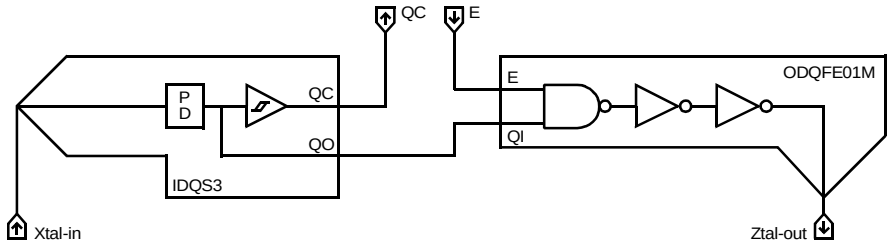
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	6.0 eql
QI	4.9 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	57.305	nA
EQL_{pd}	194.7	Eq-load

See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	4.998 4.692	7.089 6.816	9.169 8.949	12.289 12.159	17.506 17.533
QI	PADM	t_{PLH} t_{PHL}	4.181 4.672	6.316 6.797	8.429 8.910	11.554 12.097	16.674 17.490

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

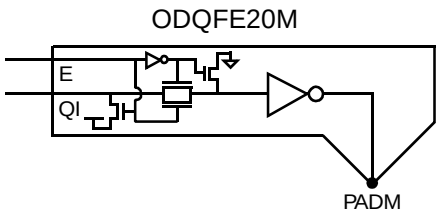
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

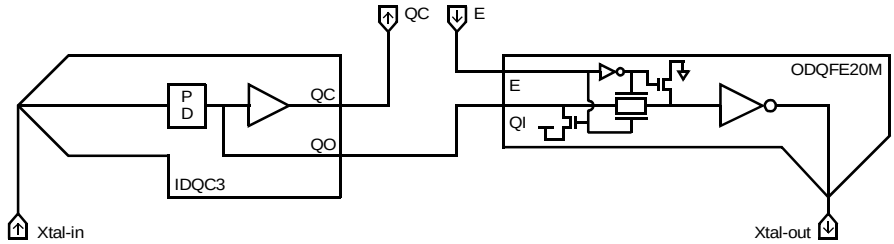
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.0 eql
QI	4.9 eql

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.453	nA
EQL_{pd}	200.7	Eq-load

See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	3.445 2.649	6.884 6.270	9.429 8.967	12.028 11.658	17.340 16.974
QI	PADM	t_{PLH} t_{PHL}	2.360 2.647	5.941 6.377	8.514 9.046	11.098 11.716	16.292 17.062

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

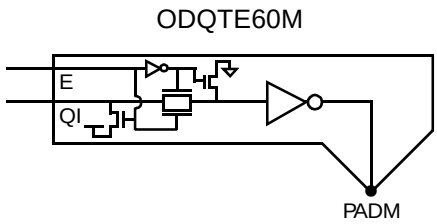
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

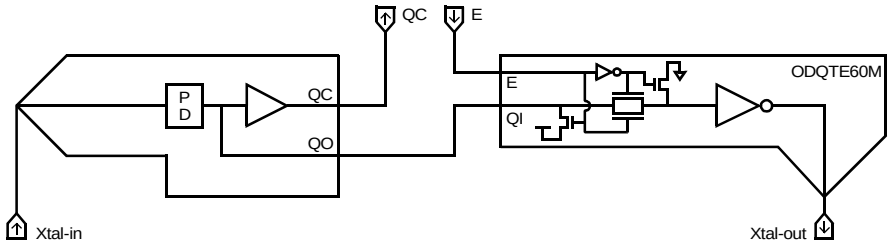
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.0 eql
QI	4.9 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.453	nA
EQL_{pd}	213.0	Eq-load

See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	2.612 1.573	4.421 3.451	7.082 6.144	12.299 11.508	17.329 16.837
QI	PADM	t_{PLH} t_{PHL}	1.475 1.689	3.314 3.577	5.906 6.266	11.069 11.617	16.235 16.933

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

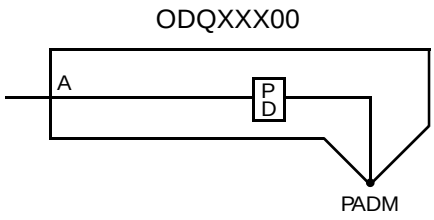
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.0 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.972	nA
EQL_{pd}	174.4	Eq-load

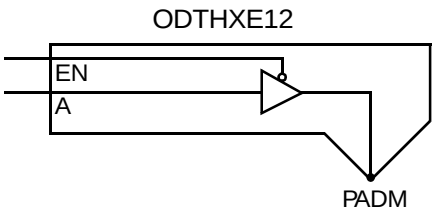
See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTHXE12 is a high performance, 12 mA, non-inverting, LVTTL-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.0 eql
EN	5.8 eql
PADM	5.82 pF

HDL Syntax

Verilog ..... ODTHXE12 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTHXE12 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	69.357	nA
EQL_{pd}	298.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

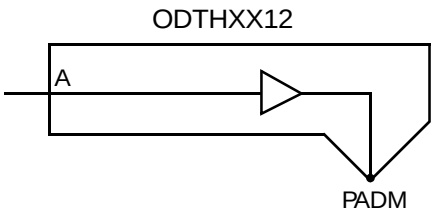
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.880 1.425	1.220 2.343	1.695 3.724	2.629 6.556	3.551 9.305
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.953 0.929 0.713 1.314	1.051 2.298	1.531 3.701	2.474 6.502	3.401 9.302

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODTHXX12 is a high performance,12 mA, non-inverting, LVTTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.0 eql

HDL Syntax

Verilog ..... ODTHXX12 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTHXX12 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	61.472	nA
EQL_{pd}	250.7	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.513	0.830	1.283	2.211	3.157
		t_{PHL}	1.106	2.079	3.473	6.268	9.066

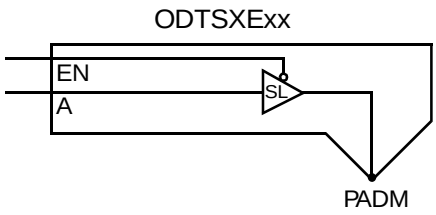
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTSXExx is a family of 4 to 12 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODTSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODTSXE**04**	ODTSXE**08**	ODTSXE**12**
A (eq-load)	1.9	1.9	1.9
EN (eq-load)	6.6	6.6	6.6
PADM (pF)	5.81	5.81	5.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXE**04**	4	68.376	253.2
ODTSXE**08**	8	68.376	275.2
ODTSXE**12**	12	68.376	297.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODTSXE**04**	From: A To: PADM	t_{PLH} t_{PHL}	2.215 4.452	4.173 10.356	6.972 18.826	12.558 35.497	18.134 51.652
	From: EN To: PADM	t_{ZH} t_{ZL}	1.908 4.256	3.875 10.088	6.639 18.637	12.191 35.276	17.809 51.491
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE**08**	From: A To: PADM	t_{PLH} t_{PHL}	1.777 2.912	2.804 5.841	4.205 9.972	7.031 18.320	9.938 26.778
	From: EN To: PADM	t_{ZH} t_{ZL}	1.496 2.652	2.482 5.583	3.898 9.775	6.788 18.167	9.608 26.542
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE**12**	From: A To: PADM	t_{PLH} t_{PHL}	1.690 2.374	2.382 4.362	3.330 7.207	5.207 12.863	7.089 18.406
	From: EN To: PADM	t_{ZH} t_{ZL}	1.382 2.245	2.060 4.224	3.022 7.021	4.926 12.621	6.764 18.240

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

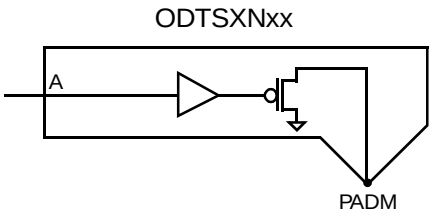
Delay (ns) From	To	Parameter	Cell ODTSXE**04**	ODTSXE**08**	ODTSXE**12**
EN	PADM	t_{HZ} t_{LZ}	0.788 0.927	1.043 1.098	1.298 1.267

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTSXNxx is a family of 4 to 12 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODTSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODTSXN**04**	ODTSXN**08**	ODTSXN**12**
A (eq-load)	5.3	5.3	5.3
PADM (pF)	0.30	6.00	5.85

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXN**04**	4	59.239	37.1
ODTSXN**08**	8	48.452	51.8
ODTSXN**12**	12	48.468	53.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

ODTSXN**04**	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	0.000	0.000	0.000	0.000	0.000

ODTSXN**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.714	4.533	8.457	16.071	23.458
ODTSXN**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.326	3.239	5.943	11.230	16.306

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

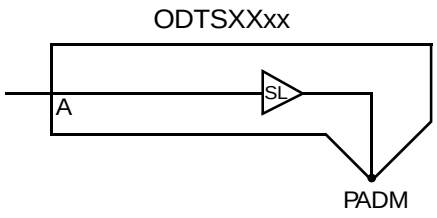
Delay (ns) From	To	Parameter	Cell ODTSXN**04**	ODTSXN**08**	ODTSXN**12**
A	PADM	t_{LZ}	0.064	0.821	0.945

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTSXXxx is a family of 4 to 12 mA, non-inverting, LVTTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODTSXXxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODTSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODTSXX**04**	ODTSXX**08**	ODTSXX**12**
A (eq-load)	8.9	8.9	8.9

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXX**04**	4	64.722	232.2
ODTSXX**08**	8	64.722	254.1
ODTSXX**12**	12	64.722	276.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

ODTSXX**04**	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PLH}	1.419 3.828	3.367 9.404	6.149 17.095	11.688 32.116	17.296 47.205
ODTSXX**08**	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PLH}	1.047 2.304	2.011 5.177	3.427 9.095	6.291 16.692	9.129 24.143
ODTSXX**12**	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PLH}	0.976 1.798	1.614 3.806	2.534 6.592	4.394 11.783	6.270 16.835

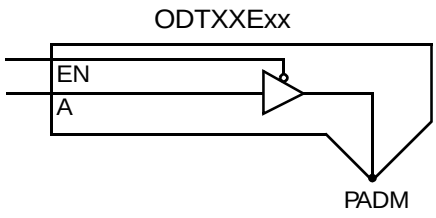
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTXXExx is a family of 1 to 12 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODTXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODTXXE**01**	ODTXXE**02**	ODTXXE**04**	ODTXXE**08**	ODTXXE**12**
A (eq-load)	5.1	7.3	7.3	1.9	1.9
EN (eq-load)	3.4	4.7	4.7	4.7	4.7
PADM (pF)	5.80	5.81	5.81	5.81	5.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXE**01**	1	57.526	189.5
ODTXXE**02**	2	59.041	199.4
ODTXXE**04**	4	59.041	211.7
ODTXXE**08**	8	65.574	260.9
ODTXXE**12**	12	65.574	281.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXE**01**	From: A To: PADM	t_{PLH} t_{PHL}	2.602 7.355	3.694 10.688	4.827 13.995	6.531 19.012	9.309 27.621
	From: EN To: PADM	t_{ZH} t_{ZL}	2.782 7.353	3.920 10.756	5.042 14.145	6.703 19.209	9.432 27.615
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODTXXE**02**	From: A To: PADM	t_{PLH} t_{PHL}	1.478 3.806	3.448 9.774	4.850 13.995	6.247 18.212	9.023 26.682
	From: EN To: PADM	t_{ZH} t_{ZL}	1.641 3.953	3.631 9.866	5.052 14.077	6.452 18.298	9.186 26.785
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE**04**	From: A To: PADM	t_{PLH} t_{PHL}	1.159 2.447	2.149 5.405	3.534 9.680	6.309 18.151	9.085 26.588
	From: EN To: PADM	t_{ZH} t_{ZL}	1.285 2.473	2.317 5.457	3.737 9.713	6.478 18.184	9.297 26.614
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE**08**	From: A To: PADM	t_{PLH} t_{PHL}	1.494 1.932	2.069 3.397	2.817 5.493	4.223 9.680	5.673 13.868
	From: EN To: PADM	t_{ZH} t_{ZL}	1.218 1.699	1.803 3.228	2.545 5.355	3.943 9.493	5.405 13.742
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE**12**	From: A To: PADM	t_{PLH} t_{PHL}	1.517 1.830	1.955 2.862	2.461 4.251	3.413 6.981	4.371 9.864
	From: EN To: PADM	t_{ZH} t_{ZL}	1.230 1.527	1.681 2.593	2.200 4.057	3.158 6.878	4.103 9.613

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

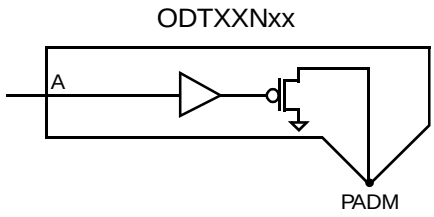
Delay (ns) From	To	Parameter	Cell				
			ODTXXE**01**	ODTXXE**02**	ODTXXE**04**	ODTXXE**08**	ODTXXE**12**
EN	PADM	t_{HZ} t_{LZ}	1.210 0.439	1.110 0.418	1.596 0.609	1.283 1.167	1.639 1.390

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTXXNxx is a family of 1 to 12 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODTXXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTXXN**01**	ODTXXN**02**	ODTXXN**04**	ODTXXN**08**	ODTXXN**12**
A (eq-load)	3.8	3.8	3.8	7.8	7.8
PADM (pF)	5.80	5.80	5.81	5.81	5.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXN**01**	1	56.067	178.7
ODTXXN**02**	2	56.067	180.9
ODTXXN**04**	4	56.067	185.1
ODTXXN**08**	8	58.198	194.8
ODTXXN**12**	12	58.198	201.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXN**01**	From: A To: PADM	t_{ZL}	13.988	20.592	27.190	37.244	54.511

ODTXXN**02**	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZL}	4.749	12.644	18.368	24.051	35.185
ODTXXN**04**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.129	5.093	9.329	17.792	26.238
ODTXXN**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.282	2.772	4.846	9.023	13.247
ODTXXN**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.112	2.224	3.754	6.813	9.866

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

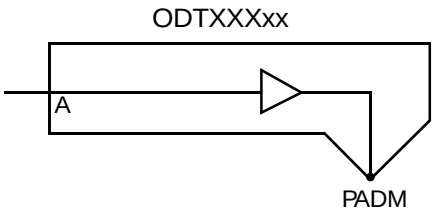
Delay (ns) From	To	Parameter	Cell				
			ODTXXN**01**	ODTXXN**02**	ODTXXN**04**	ODTXXN**08**	ODTXXN**12**
A	PADM	t_{LZ}	0.258	0.358	0.551	0.630	0.783

AMI500HXPF 0.5 micron CMOS Pad Library

Description

ODTXXXxx is a family of 1 to 12 mA, non-inverting, LVTTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODTXXXxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODTXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTXXX**01**	ODTXXX**02**	ODTXXX**04**	ODTXXX**08**	ODTXXX**12**
A (eq-load)	3.8	3.8	5.7	7.8	7.7

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXX**01**	1	56.116	183.9
ODTXXX**02**	2	56.116	190.1
ODTXXX**04**	4	57.153	202.3
ODTXXX**08**	8	58.247	227.5
ODTXXX**12**	12	58.247	247.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXX**01**	From: A To: PADM	t_{PLH} t_{PHL}	2.460 7.278	3.594 10.621	4.729 13.992	6.419 19.087	9.194 27.647

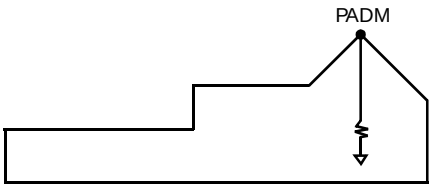
ODTXXX**02**	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.487 3.990	3.437 9.902	4.827 14.142	6.219 18.376	9.014 26.808
ODTXXX**04**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.987 2.304	1.990 5.229	3.379 9.445	6.153 17.905	8.941 26.356
ODTXXX**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.864 1.564	1.416 3.038	2.159 5.154	3.602 9.347	5.006 13.498
ODTXXX**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.885 1.574	1.306 2.651	1.829 4.196	2.801 7.258	3.730 10.273

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLD3  	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

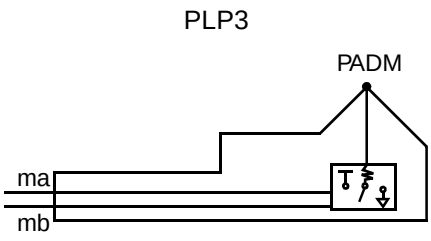
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	17.586	nA
EQL_{pd}	174.0	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.3 eql
MB	1.9 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

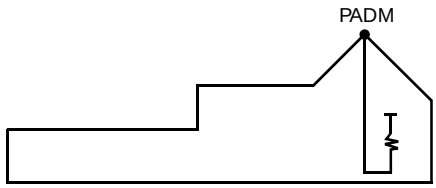
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	17.586	nA
EQL_{pd}	171.0	Eq-load

See page 2-13 for power equation.

AMI500HXPF 0.5 micron CMOS Pad Library

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3  	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

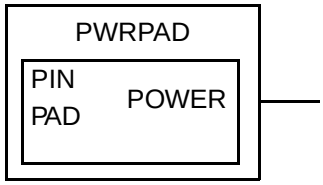
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	17.595	nA
EQL_{pd}	174.0	Eq-load

See page 2-13 for power equation.

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

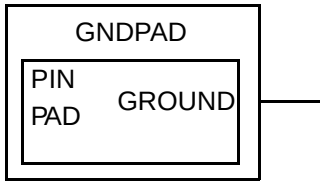
- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

GNDPAD

AMI500HXPF 0.5 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
          port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

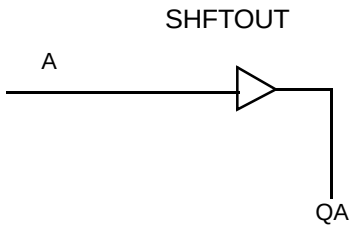
where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 3.3V core to a 5.0V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	4.1

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.976	nA
EQL_{pd}	8.2	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.246 0.236	0.274 0.277	0.317 0.329	0.373 0.391	0.416 0.434

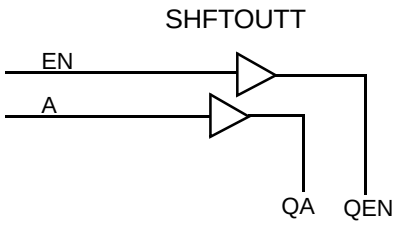
SHFTOUTT

AMI500HXPF 0.5 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 3.3V core to a 5.0V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	3.3
EN(eql)	3.0

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.885	nA
EQL_{pd}	10.5	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	6	8 (max)
A	QA	t_{PLH} t_{PHL}	0.293 0.280	0.319 0.319	0.368 0.390	0.421 0.457	0.481 0.522
EN	QEN	t_{PLH} t_{PHL}	0.270 0.273	0.298 0.310	0.351 0.381	0.405 0.449	0.457 0.517