0.5 Micron CMOS Standard Cell Data Book AMI500XXXX 5.0 Volt Revision 1.1

AMI SEMICONDUCTOR

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GENERAL INTRODUCTION

On-line updates to this information

The information contained herein is the most current and accurate available at this time. In order to assist in the design of ASICs, AMIS has published several application notes on a wide range of design topics that can be accessed on-line at http://www.amis.com/tech_info. Please visit the AMIS web site to ensure that you have the most current information prior to beginning the design of your ASIC.

AMI Semiconductor - Providing customers the best total ASIC solution for more than 30 years

AMI Semiconductor (AMIS) pioneered the development of the world's first custom MOS ICs in 1966. With more experience than any other ASIC vendor, you can be assured that when you bring your ASIC development project to AMIS, you are working with a dependable team that has the depth of experience to provide you with an optimum solution, on time and on budget.

The vision shared by all employees at AMIS is expressed in our mission statement:

> *Through the smart application of mixed-signal and digital ASIC technology, AMIS makes it easier for its customers to get to market faster and more economically with better end products.*

AMIS strives to realize this vision by offering a range of products and services aimed at improving cycle time, reducing overall design cost, achieving world-class quality and reliability, and designing to customer needs.

AMIS provides a full range of digital and mixed-signal ASICs, including high voltage and sensor interface ASICs, low data rate RF products, system level integration, FPGA-to-ASIC conversion, and modular foundry services.

AMIS operates globally with world wide headquarters in Pocatello, Idaho and European headquarters in Oudenaarde, Belgium. AMIS also owns a wafer sort and final test facility in Manilla, Philippines.

Markets

- Automotive
- Medical
- Industrial
- Military
- Communications
- Computer

Sales and Distribution

- Full-service sales and technical support offices are located in key markets throughout North America, Europe, and the Asia Pacific region.
- Technical service centers located in North America and Europe offer customers a full range of digital and mixed-signal ASIC design resources and services.
- For the most current sales information, go to www.amis.com/sales.

SECTION 2
OVERVIEW

Description

Features

- **Minimum drawn length: 0.6µ**
- **Excellent performance:**
  – 590 MHz maximum toggle rate on clocked flip-flops (T_J = 135°C)
  – 218 ps delay (FO=2; L=2mm) for a 2-input NAND gate
  – 103 ps delay (FO=2; L=0mm) for a 2-input NAND gate
  – 6 ns clock to out performance (CL = 35 pF)
- **Unparalleled temperature ranges:**
  Operating temperatures range from -55 to 125°C.
- **Clock Tree Synthesis:**
  Clock drivers are placed to minimize clock skew and latency effects on circuit performance. Parameterized clock buffers model the clock trees before layout. AMIS matches the simulation parameters of the prelayout models with a physical clock tree during layout.
- **Cost driven architecture:**
  A choice of 2 or 3 level metal interconnect provides the lowest device cost for the number of gates and pads required.
- **Extensive library for quick design:**
  – Complete primary cell and I/O library
  – Synchronous ROM compiler from 64x1 to 16Kx32 bits
  – Megacells include processors, peripherals, and datapath synthesizers
  – 100% compatible with AMI Semiconductor's proven ASIC Library
- **Extensive RAM support:**
  – Asynchronous, synchronous, single, dual, and n-port
  – Build from any configuration of 16x1 and 256x8, 512x4, 1024x2, and 2048x1 blocks up to the maximium gate count of the array
- **Extensive I/O cell options:**
  – User-configurable pad cells with predefined components
  – 1 to mA per single I/O cell
  – Custom configurations for I/O drive up to 96 mA
  – Standard and slew rate limited available
  – PCI 33 MHz compliant
  – CMOS, TTL, LVCMOS, LVTTL, PCI (33MHz) levels
- **Mixed voltage operation:**
  – Split power supply bussing between core and pads
  – V core operation
  – Mixed V and V I/O pads
  – 5V input tolerance on 3.3V pads
  – 5V output drive with 5.0V power pads
- **Extensive packaging capabilities:**
  – QFPs, CQFPs, TQFPs, PLCCs, LCCs, JLCCs, PBGA, BGAs, PGAs, CPGAs, SOICs, TSOPs, PDIPs, PQZs, M-QUADs, individual die
  – Burn-in capability as required
- **Automatic Test Program Generation:**
  Scan macros (NETSCAN™) for high fault coverage
- **JTAG Boundary Scan macro support**
- **Full operating voltage range from 2.7V to 5.5V**
- **ESD protection > 2kV; latchup > 100 mA**
- **Power dissipation:**
  1.58µW/MHz/gate (FO=1; V_{DD}=V)

MIXED VOLTAGE I/O MACROS FOR 5 VOLT TOLERANT AND 5 VOLT COMPATIBILITY

- Technology continues to drive down the maximum core and I/O operating voltages of ASICs. Since board level compatibility with the older interface standards continues to exist, ASICs must be able to provide a mixed voltage I/O solution on the same design. The two industry terms that describe these interface requirements are 5 volt tolerant and 5 volt capable. In the following explanations of mixed voltage I/O the two voltages used are 5V and 3.3V, however, the same explanations apply to any mixed voltage I/O application (i.e. 3.3V and 2.5V).
- **5 VOLT TOLERANT:** When operating at 3.3V, special output pad cells are required to drive 3.3V levels and withstand 5V during input or tri-state mode. When receiving signals above 3.3V, these I/O cells must be used to prevent damage to the circuit or disruption of normal circuit operation. The TTL input portion of the I/O cell are programmed to achieve proper switching levels for either 5V or 3.3V inputs but not both. Maximum drive of these cells is less than non 5 volt tolerant macros in the library since many of the output devices in the pad are used to construct the 5 volt tolerant circuitry.
- **5 VOLT CAPABLE:** 5 volt capable I/O requires the cell both accept and drive 5V signals. Separate power pins are required for each of the core and I/O voltages. One or more power pins are used for core and low voltage pad macros and additional power pins are used for high voltage pad macros. All core macros and low voltage pad macros are tied to the 3.3V supply. 5 volt capable pad macros must be used when receiving/driving signals above 3.3V. Each I/O cell has voltage level shifters to allow either 5V or 3.3V external signals to interface to the 3.3V core logic.

Product Applications

PLD OR FPGA CONVERSION: For high volume products, AMI Semiconductor's NETRANS® converts netlists from PLDs and FPGAs to more cost and performance effective AMI designs.

2ND SOURCE FOR EXISTING PRODUCTS: AMI Semiconductor's netlist conversion capabilities allow AMI to be a cost-effective, alternate supply for existing high volume products.

PROCESS UPGRADE: AMIS ASICs designed in 1.25µm, 1.0µm, 0.8µm, 0.6µm processes can be easily upgraded to the AMI family. The AMIS ASIC Library provides a common netlist design base.

ADDING CUSTOM BLOCKS: AMIS specializes in adding custom logic and simple analog functions to ASIC designs.

ASIC Design Tools and Methodology

AMIS ASICs are supported on many third party software platforms:

- Cadence®
- Mentor Graphics™
- Synopsys®
- Viewlogic®
- Veribest®
- Motive™
- Exemplar Leonardo™
- SDF back-annotation
- VHDL Vital simulation™ (sign-off pending)
- Verilog® simulation (sign-off)

AMI Semiconductor's proprietary expert-system software, ACCESS Design Tools™, is an integrated suite of software tools for digital ASIC verification, FPGA migration, and ASIC second sourcing. ACCESS allows greatly shortened development spans, lower NRE, and increased first silicon success. AMI Semiconductor's software support methodology ensures a tight, well-coupled design to the fabrication process. AMI Semiconductor's dedicated, experienced engineering staff can assist at any step in the design process.

ASIC Design Flow

(See Figure 1: "ASIC Design Flow" on page 2-6) To help customers design their ASICs, AMIS supplies a design kit with a cell library containing symbols, simulation models, and software for design verification, timing calculation, and netlist generation. Prelayout timing simulations use capacitance and resistance values derived from statistical averages of known layouts. After the actual layout is completed by AMIS, a post-layout interconnect capacitance and resistance table is supplied for final validation of device timing.

Working with an AMIS design center, customers capture and verify their designs using AMI Semiconductor'sAMI Semiconductor's ASIC Library. They also create test vectors for the logical part of their manufacturing test. AMIS provides automatic test program generation software, megacells, and netlist rule checkers to greatly speed up the design. A fault coverage check of the test vector set is an optional service.

A "Design Start Package" is completed by the customer and submitted to AMIS engineers for review. The Start Package contains the device specification, netlist, pin list, critical timing paths, and test vectors. The design is pre-screened using AMI Semiconductor's ACCESS Design Tools and then resimulated on Verilog (AMI Semiconductor's sign-off simulators). The results are compared to the customer's simulation results.

Once the design has passed the initial screening, it is ready for layout. The layout begins by placing memory and megacells, assigning priority to critical paths, and designing the distribution and buffering of clocks. Layout is completed with automatic place-and-route on the balance of the circuit.

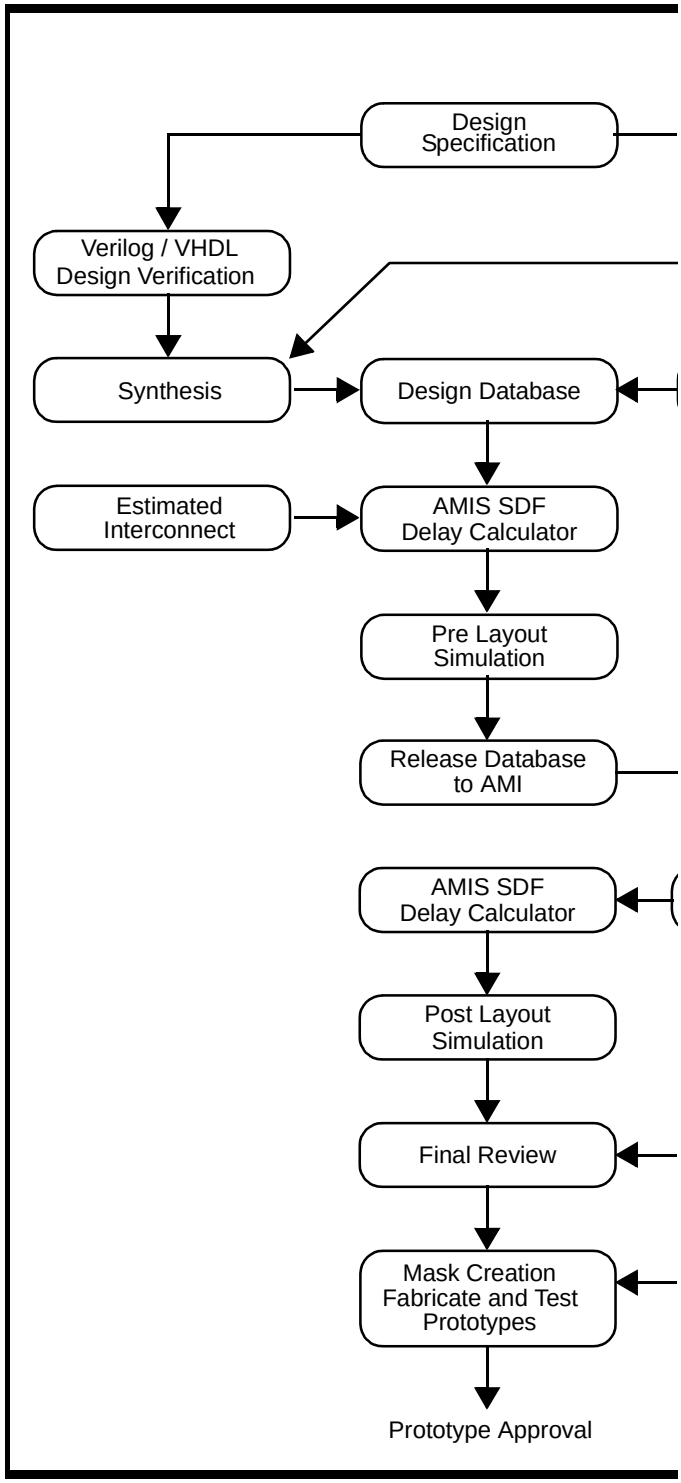
After layout is complete, the interconnect data is extracted from the physical layout and fed back to the sign-off simulator for final circuit verification. The post layout interconnect data is sent to the customer for final validation on their simulator. When the post-layout simulation is complete and approved by the customer, the design is released for mask and wafer fabrication.

The test program is developed in parallel with the design using automatic test program generation software. This allows prototypes to be tested before they are shipped.

AMIS uses Verilog/VHDL to speed ports between various software products.

AMI500xxxx 0.5 micron CMOS Standard Cell

Figure 1: ASIC Design Flow



The Design Library

AMI Semiconductor's design library provides a robust collection of building blocks for the AMI family. A broad range of primary cells is complemented with memory cell compilers and useful megafunctions. Custom cells are quickly designed by AMI Semiconductor's extensive, US-based design team.

The AMIS ASIC Library

The AMIS ASIC Library contains a rich set of core cells and configurable pad cells. The library is portable across all of AMI Semiconductor's gate array and standard cell families.

AMI's Innovative Pad-Piece Methodology

AMI Semiconductor's ASIC Library provides an innovative approach to I/O pad cell design. Thousands of different I/O cell configurations are possible by choosing from an array of input, output, and pullup/pulldown pad piece cells and making the appropriate schematic or HDL connections. In addition, AMIS conversion libraries can easily migrate netlist designs from older technologies that use ASIC Standard pad cells. AMI Semiconductor's ACCESS Design Tools software maps pad cells to their functional (fundamental), pad-piece blocks. Custom configurations are made by combining the pieces. Pad-piece design benefits AMIS customers by drastically reducing the need for workstation simulation models of I/O pad cells that do not yet exist. For detailed information of pad-piece usage, see the AMIS applications note *Pad Pieces* (4401035).

Memories

Customers supply cell specifications to AMI, and then receive simulation timing specifications overnight, and full simulation models for any AMIS supported software within five working days. See AMI Semiconductor's web page (www.amis.com) for more information.

Megacells

The AMIS gate array and standard cell families offer megacells for many popular functions, including: Core Processors, Peripherals, FIFOs, and Datapath (see Tables 3, 4, 5, and Table 6, "Peripherals," on page 2-9). AMIS core processors and peripherals duplicate the function of industry standard parts. Data path and FIFO megacells are developed using parameterized logic synthesizers. Most of AMI Semiconductor's megacells are "soft" or "firm" cores that are technology independent and can be customized for specific applications. Detailed functional information can be found in AMI Semiconductor's standard device data sheets.

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DC Specifications

Table 1: Operating Specifications

Parameter		Minimum	Maximum	Units
V_{DD} Supply Voltage		2.7	5.5	Volts
Ambient Temperature	- Military	-55	125	°C
	- Commercial	0	70	°C
Junction Temperature	- Military	-55	135	°C
	- Commercial	0	85	°C
CMOS Input Specifications (V<VDD<V; 0°C<T<70°C)				
Vil	Low Level Input Voltage		$0.3*V_{DD}$	Volts
Vih	High Level Input Voltage	$0.7*V_{DD}$		Volts
Iil	Low Level Input Current		-1.0	µA
Iih	High Level Input Current		1.0	µA
Iil	Input Pull-Up Current	-30	-110	µA
Iih	Input Pull-Down Current	30	135	µA
Vt-	Schmitt Negative Threshold	$0.2*V_{DD}$		Volts
Vt+	Schmitt Positive Threshold		$0.8*V_{DD}$	Volts
Vh	Schmitt Hysteresis	1.0		Volts
TTL Input Specifications (V<VDD<V; 0°C<T<70°C)				
Vil	Low Level Input Voltage		0.8	Volts
Vih	High Level Input Voltage	2.0		Volts
Iil	Low Level Input Current		-1.0	µA
Iih	High Level Input Current		1.0	µA
Iil	Input Pull-Up Current	-30	-110	µA
Iih	Input Pull-Down Current	30	135	µA
Vt-	Schmitt Negative Threshold	0.7		Volts
Vt+	Schmitt Positive Threshold		2.1	Volts
Vh	Schmitt Hysteresis	0.4		Volts

Table 2: Output Operating Specifications (V<VDD<V; 0°C<T<70°C)

Driver[1]	Vol Maximum	Voh Minimum	Iol Maximum	Ioh Maximum
1 mA Driver	0.4	2.4	1.0	-1.0
2 mA Driver	0.4	2.4	2.0	-2.0
4 mA Driver	0.4	2.4	4.0	-4.0
8 mA Driver	0.4	2.4	8.0	-8.0
16 mA Driver	0.4	2.4	16.0	-16.0

1. See “DC Characteristics” on page 2-10 for specific output requirements.

Vol = Low Level Output Voltage given in Volts

Voh = High Level Output Voltage given in Volts

Iol = Low Level Output Current given in mA

Ioh = High Level Output Current given in mA

Table 3: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
V_{DD}, Supply voltage		-0.3		Volts
Input pin voltage		-0.3	V_{DD}+0.3	Volts
Input pin current		-10.0	10.0	mA
Storage temperature	- Plastic packages	-55	125	°C
	- Ceramic packages	-65	150	°C
Lead temperature			300	°C for 10 sec.

Note: The specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long term reliability of the device.

DC Characteristics

(V_{DD} = V, T = 25°C, Typical Process)

N-Channel Output Driver

N-Channel Pull-Down Device

P-Channel Output Driver

P-Channel Pull-Up Device

DC Derating Information

The DC Characteristics shown on page 2-10 can be derated to obtain values at other operating conditions using the formula:

$$I_{DC} = (I_{DC}(typ) \cdot K_{PDC} \cdot K_{VDC} \cdot K_{TDC})$$

where: I_{DC}(typ) is a value from the DC characteristic current curves on page 2-10; K_{PDC} is the DC process derating coefficient determined at the processing limits; K_{VDC} is the DC voltage derating coefficient; and K_{TDC} is the DC temperature derating coefficient. The N-channel driver has a different set of coefficients for K_{PDC} and K_{TDC} due to the ESD protection structures.

Table 4: DC Variations with Process (KPDC)

	N-Channel Output Driver (Vol = 0.4V)			N-Channel Pull-Down Device (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
Process	WCS	TYP	WCP	WCS	TYP	WCP	WCS	TYP	WCP
K_{PDC}	0.62	1.00	1.18	0.63	1.00	1.19	0.74	1.00	1.27

Table 5: DC Variations with Voltage (K_{VDC})

	All N-Channel (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
V_{DD}	4.5	5.0	5.5	4.5	5.0	5.5
K_{VDC}	0.98	1.00	1.01	0.80	1.00	1.21

DC Variations with Temperature for the N-Channel Output Driver (K_{TDC})

DC Variations with Temperature for all other N-Channel and P-Channel Devices

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Delay Derating Information

The propagation delays listed in the data sheets are for typical temperature (25°C), typical supply voltage (V), and typical processing conditions. To calculate the delay at other conditions, use the following equation:

$$T_{pdx} = T_{pdx}(\text{typ}) \cdot K_P \cdot K_V \cdot K_T$$

where T_{pdx}(typ) is given in the data sheets; K_P is the process derating coefficient (determined at the processing limits); K_T is the temperature derating coefficient; and K_V is the supply voltage derating coefficient.

Delay Variations with Temperature (K_T)

Delay varies linearly with temperature. K_T, the temperature derating coefficient, is determined by the following formula and table of common operating point values:

Temp	K_T
-55°C	0.79
-25°C	0.86
0°C	0.96
25°C	1.00
70°C	1.13
100°C	1.22
125°C	1.29

Temp. Range	K_T Formula
-55°C to 140°C	$K_T = 1.0 + (T_J\text{-}25)(2.756E\text{-}3)$

Where T_J is the temperature (in °C) at the silicon junction.

Delay Variations with Process (K_P)

Delay variations with process are fixed constants determined at the limits of acceptable processing. Values for K_P, the process derating coefficient, are shown below:

Derating Coefficient (K_P)	Process Variation Point
1.30	Delay increase due to “Worst Case Speed” (WCS) processing
1.00	Typical delay; Processing target
0.70	Delay reduction due to “Worst Case Power” (WCP) processing

Delay Variations with Voltage (K_V)

Delay varies nonlinearly with voltage. Values of K_V for common operating points are shown below, and a characteristic curve is shown at right.

V_{DD}	K_V
2.7V	1.75
3.0V	1.54
3.3V	1.39
4.5V	1.07
5.0V	1.00
5.5V	0.95

Description of Data Sheet Features

CELL NAME: AMI Semiconductor's cell name.

LIBRARY TYPE: Designates the minimum transistor gate length and library type, such as standard cell or gate array.

DESCRIPTION: Describes the function of the cell.

LOGIC SYMBOL: Shows a picture of the symbol as it appears in the workstation design kits.

TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels.

Types of logic levels found in the logic tables are as follows:

H = High level steady state,
L = Low level steady state,
↑ = Transition from low level to high level,
↓ = Transition from high level to low level,
X = Any level including transitions,
NC = No change in output level for a given set of input levels,
IL = The output level is unknown for this set of illegal input levels,
Z = High impedance level,
UN = Un-driven node or input,
Q(n) = The level of Q before an active transition on the affecting node, and
QN(n) = The level of QN before an active transition on the affecting node.

EQUIVALENT GATES: The cell area normalized to the area of the NA21, 2-input NAND gate.

HDL SYNTAX: Verilog and VHDL instantiation syntax.

EQUIVALENT LOAD: An equivalent load is defined as the capacitive pin load of an NA21 cell "A" pin. It is equal to 30.9 fF. In the propagation delay tables 13 fF of interconnect capacitance is added to each equivalent load. For a more accurate estimation of interconnect capacitance see Table 6, "Interconnect Load Estimation," on page 2-15**.**

PIN LOADING: A table of cell input loads in units of equivalent loads (the input load normalized to the input load of an NA21, 2-input NAND gate).

POWER CHARACTERISTICS: Power for the cell can be described in three parts, as shown by the three terms in the Power Equation for Core Cells and Input Buffers below. First, the power dissipated due to Static I_{DD} across the channels and through the formed diodes. Second, the power due to the switching voltage across loads on the internal nodes of the cell. Third, the power due to the switching voltage across a load that a cell is driving.

The power characteristics table provides Static I_{DD} for a junction temperature of 85°C, and the dissipative load for all the switching nodes in the cell in terms of equivalent loads.The load that a cell drives is calculated by adding up input loads, and then adding the estimated load from the Load Estimation table on page 2-15. Below are equations for calculating the power dissipation:

Core Cells and Input Buffers

$$\text{POWER} = (\text{Static } I_{DD})\ V_{DD} + (30.9\text{fF})EQL_{pd}V_{DD}^2 f + (30.9\text{fF})EQL_I V_{DD}^2 f$$

Output Buffers

$$\text{POWER} = (\text{Static } I_{DD})\ V_{DD} + (30.9\text{fF})EQL_{pd}V_{DD}^2 f + C_{ol}V_{DD}^2 f$$

where:

Static I_{DD} = Static leakage current of the cell
V_{DD} = Operating voltage
EQL_{pd} = Load of the switching nodes in the cell
f = Frequency of operation
C_{ol} = Load in farads on the output buffer
EQL_I = Load of the driven interconnect and driven input pins

Description of Data Sheet Features (continued):

The frequency term of the power equation dominates, making the static current term insignificant, except to give the standby current.

Three types of buffers (input, output, and bidirectional) may be assembled using pad piece cells. Calculating power characteristics for pad pieces is dependent on the buffer type. The power dissipated by a buffer is the cumulative power dissipated by its component pad pieces.

- *ID pieces* use the input buffer equation. (The input and output buffer equations are described on the previous page).
- *Output pieces* use the output buffer equation. C_{OL} does not include any PADM pin loading of ID or PL pad piece cells that may be connected to the OD piece.
- *PL pieces* use the output buffer equation. C_{OL} does not include any PADM pin loading of ID or OD pad piece cells that may be connected to the PL piece.

PROPAGATION DELAYS : The Propagation Delays table in a data sheet contains timing data for the various input to output paths in the cell. The path for the delay is identified by two pins. Delay values are given for each path's propagation delay or timing parameters corresponding to each of the five equivalent loads. The equivalent loads are given over the range of allowed loading for the cell, up to the maximum load the cell can drive. The output buffer loading is in picofarads. To find the delay for a cell, add up the loads of all the inputs that the cell is driving, then add the estimated interconnect load from the Load Estimation table on page 2-15. Finally, look up the value for the desired timing parameter corresponding to the load on the cell. Interpolate to find values in between load columns.

The Delay Characteristics table in a data sheet may contain the following propagation delays and timing parameters:

t_{PLH} = Input to output propagation delay for a rising edge on the output

t_{PHL} = Input to output propagation delay for a falling edge on the output

t_{ZH} = High impedance to high level delay

t_{ZL} = High impedance to low level delay

t_{HZ} = High level to high impedance delay

t_{LZ} = Low level to high impedance delay

t_{su} = Input setup time with respect to clock

t_{h} = Input hold time

t_{w} = Input pulse width

AMIS models the effects of input slew, and output resistive and capacitive loading for a particular cell's path delay. The delay in the data sheets represents a typical load on the inputs of the cell. Due to differing capabilities of logic simulators, the delay modeling method varies and may still be a linear model. Loads beyond the maximum load are an extrapolation of the model, and their accuracy is not guaranteed. More accurate delays can be determined using an AMIS workstation kit. Contact your sales representative or the factory about modeling for specific workstation kits and simulators.

Interconnect estimation

For pre layout simulation, AMIS provides an estimated interconnect value based on statistical data. Table 12 provides data points from those non-linear equations to enable the designer to estimate timing based on data book information.

Table 6: Interconnect Load Estimation

	Fan Out (Equivalent Loads)							
	1	3	6	9	12	20	35	50
100	0.3	1.2	2.3	3.4	4.5	7.2	11.9	16.4
125	0.4	1.3	2.6	3.8	5.0	8.0	13.2	18.1
150	0.4	1.4	2.8	4.2	5.4	8.6	14.3	19.6
175	0.4	1.6	3.1	4.5	5.8	9.3	15.3	21.0
200	0.5	1.7	3.3	4.8	6.2	9.8	16.3	22.3
225	0.5	1.8	3.4	5.0	6.5	10.4	17.1	23.5
250	0.6	1.9	3.6	5.3	6.9	10.9	18.0	24.7
300	0.6	2.0	3.9	5.7	7.5	11.8	19.5	26.8
350	0.7	2.2	4.2	6.2	8.0	12.7	20.9	28.7
400	0.7	2.3	4.5	6.5	8.5	13.4	22.2	30.4
450	0.8	2.5	4.8	6.9	9.0	14.2	23.3	32.0
500	0.8	2.6	5.0	7.2	9.4	14.9	24.5	33.6
550	0.9	2.7	5.2	7.6	9.8	15.5	25.5	35.0
600	0.9	2.8	5.4	7.9	10.2	16.1	26.5	36.4
650	1.0	3.0	5.6	8.2	10.6	16.7	27.5	37.7

The equivalent loads that are provided in the propagation delay tables within the data sheets include 13 fF of interconnect capacitance for each equivalent load. Table 6 was created from a non-linear statistical model and provides a more accurate representation of estimated interconnect for the various die sizes, base arrays and fanout. To compute equivalent loads driven by a given cell use the following formula:

$$\text{total\_eq\_loads} = \Sigma \text{ fanout loads (from pin loading tables)} + \text{estimated interconnect value (table 6)}$$

The equivalent loads in the propagation delay tables need to be scaled by multiplying each equivalent load by 1.42.

Packaging

A variety of popular packages is available for the AMIS gate array and standard cell families.

For information on special packages or packaging requirements, contact an AMIS sales representative.

Table 7: Package Offering

Package Type	Pin Count
Plastic Quad Flatpack, PQFP	44, 52, 64, 80, 100, 120, 128, 144, 160, 184, 208, 240, 256, 304
Low/Thin Quad Flatpack, LTQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 208
Metal Quad Flatpack, MQUAD®	128, 144, 208
Power Quad 2, PQ2	128, 144, 160, 208, 304
Ceramic Quad Flatpack, CQFP	40, 44, 52, 64, 84, 100, 132, 144, 172, 196, 256, 352
Plastic Leaded Chip Carrier, PLCC	20, 28, 32, 44, 52, 68, 84
Ceramic Leaded Chip Carrier, JLDCC	28, 44, 52, 68, 84
Ceramic Pin Grid Array, CPGA	65, 68, 69, 84, 85, 101, 109, 121, 132, 145, 155, 177, 181, 208, 225, 257, 299, 476
Ball Grid Array, BGA	121, 169, 208, 225, 256, 313, 316, 352, 388,420, 432, 456, 484, 560, 676, 680, 728, 900
Low Profile Fine Pitch BGA, LFBGA	36, 40, 56, 64, 81, 84,100, 108, 128, 144, 160, 176, 208, 256

ON-LINE APPLICATION NOTES

AMIS provides a collection of application notes to aid the engineer in the design of gate array and standard cell Application Specific Integrated Circuits (ASICs). Each of the topics found on AMI Semiconductor's web site http://www.amis.com/tech_library provides supplemental information to those found in this book in addition to other very useful guidelines and helps. Some of the subjects currently available are Boundary Scan, internal scan, clocking schemes, crystal oscillators usage, guidelines for supplying test vector simulation, using megacells and memories, sequential device metastability, on-chip pull-up/pull-down resistors, using pad pieces, power estimation, Programmable Phase Locked Loop (PLL) , standard test philosophy, synchronous design, thermal resistance of packages, using nand tree circuits for Input parametric testing, and VHDL based design methodology. This site will be continually updated with useful information to assist the designer.

SECTION 3
CORE LOGIC

This process has multiple cores libraries available. Select the appropriate library that will meet your specific design requirements. The core libraries can be found at @ http://www.amis.com/tech_info.

	AMIS Fab Process	Separate Substrate	Core Voltages	Core Cells	Density (gates/mm^2)	Power (uW/MHz/gate) @ 5.0V	Power (uW/MHz/gate) @ 3.3V	Power (uW/MHz/gate) @ 2.5V	Speed NA22 => 1 fo-0mm	Speed NA22 => 2 fo-0mm	Speed NA22 => 2 fo-2mm	Toggle Rate (MHz)
AMI500HXSC	C5	N	5.0/3.3	349	7.35K	1.58	0.69	NA	82	103	218	590
AMI500SXSC	C5	Y	5.0/3.3	332	6.92K	1.58	0.69	NA	82	103	218	590
AMI500MXSC	C5	Y	5.0/3.3/2.5	332	14.4K	0.63	0.28	0.16	101	128	561	440
Notes			(1)		(2)	(3)	(4)	(5)	(6)	(6)	(6)	(7)

Notes:

1) Voltage for which the library has been characterized
2) These numbers are for comparison purposes only and indicate the raw (unrouted) densities. Routing density varies with number of routing layers, library cells, and total gates. Consult factory for more information.
3) Power numbers for library characterized at the first core voltage listed
4) Power numbers for library characterized at the second core voltage listed
5) Power numbers for library characterized at the third core voltage listed
6) All performance numbers are at typical first core voltage listed with typical temperature and process, result in pS
7) Toggle rates are first core voltage listed- 10%, worst case temperature of 135C, and WCS process corner

SECTION 4
PAD LOGIC

This process has multiple pad libraries available. Select the appropriate library that will meet your specific design requirements. The pad libraries can be found at @ http://www.amis.com/tech_info

	AMIS Fab Process	Mixed Signal Enhancements	Min. Drawn Gate Length (um)	5V I/O Tolerant	5V I/O Capable	Mixed Voltage Ready	PCI 33MHz	Inline Pad Pitch (um)	Staggered Pad Pitch (um)	Pad Height (un/mil)	Max Output per Pad (mA)	Balanced Output per Pad (mA)	Pad Window Opening (um)	Pad Node Capacitance (pF)
AMI500HXPR	C5	N	0.6	N	Y	Y	Y	86	60	718/82.3	24	16	74	4.9
AMI500HXPS	C5	N	0.6	N	Y	Y	N	86	60	558/22.0	12	10	74	4.9
AMI500XHPF	C5	Y	0.6	N	Y	Y	N	135	NA	388/15.3	12	12	74	5.8
AMI500HXPM	C5	Y	0.6	N	Y	Y	N	86	NA	567/22.3	12	10	74	4.9

SECTION 5
Megacell

Please refer to application notes which have either been included on the CD with this databook or at AMIS website http://www.amis.com/tech_info **for megacells available.**

SECTION 6
MEMORIES

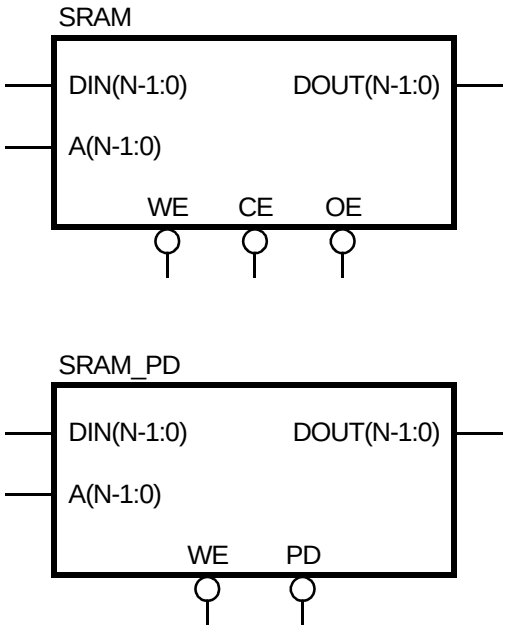
Selection Guide

Memories Selection Guide

Features

- 6-T memory cell design
- Simple combinational logic decoding
- Small bitline differential in read mode eliminates precharge delay
- Fast ATD circuit turns on wordlines and sense amps only as needed to save power while allowing asynchronous operation

Logic Symbol



SRAM
High Speed Low-Power Single Port

CMOS ASIC Standard Cell Memories

SRAM: High Speed Low-Power Single Port Description

AMI Semiconductor's high speed, low power CMOS RAM is available in both single and dual port versions. Column select passgates provide a cascode gain stage, followed by a differential voltage sense amp. The memory array columns may be multiplexed to optimize the aspect ratio. Multiplexing of columns, or column folding, shortens the bitline length (reduces the number of rows in the array) while increasing the width of the memory array. No change in the total memory bit count occurs.

The zero_out option sets all outputs to to 'zero'. This operation is controlled by the PD signal.

The RAM draws current only in response to changing inputs, minimizing power consumption and allowing complete IDDQ testing. In addition to normal CMOS transient current, address changes activate the sense amps and one row of memory cells for a period of time longer than access time. The current drawn by each sense amp is comparable to the read current of each memory cell.þ

Signal Summary

INPUTS		OUTPUTS	
PORT LABEL	**FUNCTION**	**PORT LABEL**	**FUNCTION**
A	Address	DOUT	Output Data
DIN	Input Data		
CE	Chip Enable, avtive low		
WE	Write Enable, active low		
OE	Output Enable, active low, tristated output control		
PD	Power Down, active high, read and write cycles disabled and output driven to zero (0) when active		

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
N	bits per word	Integer	1 -144
WORDS	number of words	Integer	8 -16384
M	address size	Integer	3 - 14
BPC	bits per column	Integer	2, 4, 8, 16, 32
FLOORPLAN	auto floorplan	Integer	0, 1
BUFFER_SIZE	buffer size	String	1-6
FREQUENCY	frequency in MHz	Integer	1-100
VDROP	voltage drop in millivolts	Integer	1-249

Block height range is 4-512; block width range is 4-288; max total bits is 144K (16K x 9).

Bits Per Column (BPC) Options

BPC VALUE	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT	MINIMUM BITS	MAXIMUM BITS
2	8	1024	4	1	144
4	16	2048	8	1	72
8	32	4096	16	1	36
16	64	8192	32	1	18
32	128	16384	64	1	9

SRAM
High Speed Low-Power Single Port

CMOS ASIC Standard Cell Memories

Parts

PART NAME	PINS
sram	A, CE, DIN, OE, WE, DOUT
sram_pd	A, DIN, PD, WE, DOUT

Truth Table

zero-out option false

INPUTS					OUTPUTS	COMMENT
A	CE	OE	DIN	WE	DOUT	
0/1	0	0	X	1	Data	Read
X	0	1	X	1	Z	Output Disabled (standard) - RAM Active
X	1	1	X	X	Z	Output Disabled (standard) - RAM Disabled
X	1	0	X	X	Data	Output Stable, RAM disabled
0/1	0	0	0/1	0	Data	Write with Write-Through
0/1	0	1	0/1	0	Z	Write

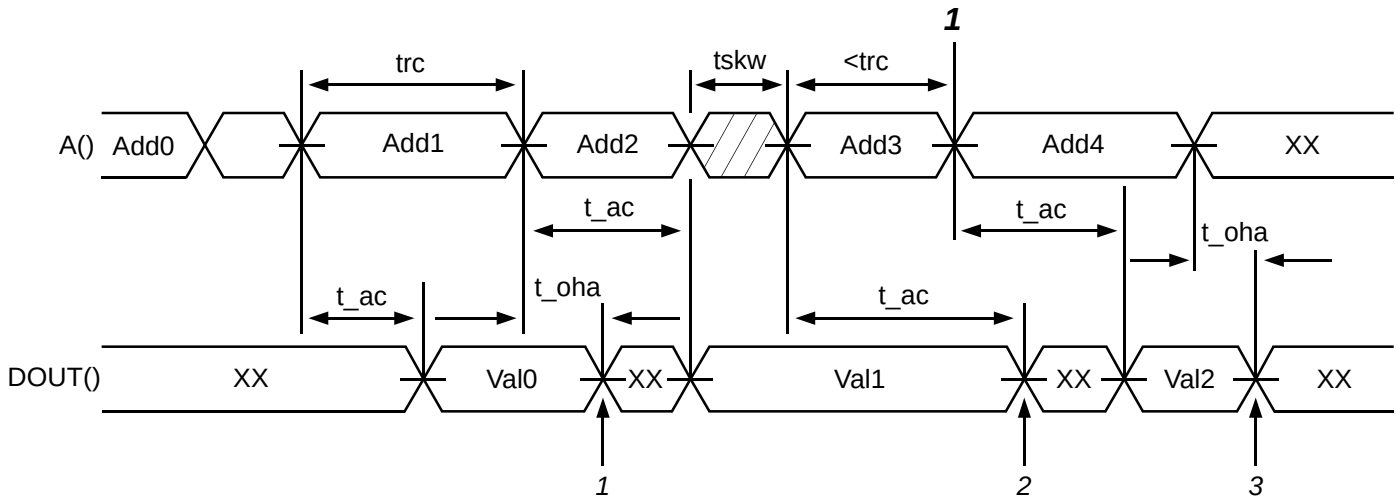
zero-out option true

INPUTS				OUTPUTS	COMMENT
A	PD	DIN	WE	DOUT	
X	1	X	X	0	Output Disabled (zero_out), RAM disabled
0/1	0	X	1	Data	Read
0/1	0	0/1	0	Data	Write with Write-Through

SWITCHING TIME WAVEFORMS

Single Port RAM Read Cycle 1

sram :CE = '0', OE = '0', WE = '1'
sram_pd:PD='0', WE='1'



Notes: t_ac : Address Access Time (maximum of Rise/Fall)
trc : Read Cycle Time
t_oha : Output Hold Time from Address Change (minimum of Rise/Fall)
tskw : All addresses must complete transition within this time

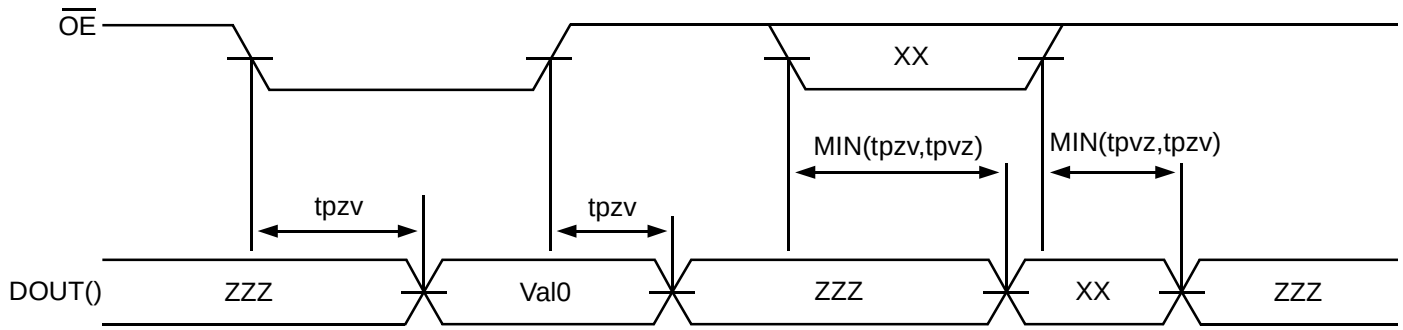
1. t_oha delay will only be applied to the last data accessed, otherwise, t_ac will be used for the pin-to-pin delay.
2. trc <= t_ac. If Add3 width is less than trc, DOUT() goes to 'X'.
3. If A() becomes 'X', DOUT() goes 'X' after time t_oha.

***1**. Error: Illegal Address input: Address cycle time is smaller than minimum trc.*

CMOS ASIC Standard Cell Memories

Single Port RAM Read Cycle 2

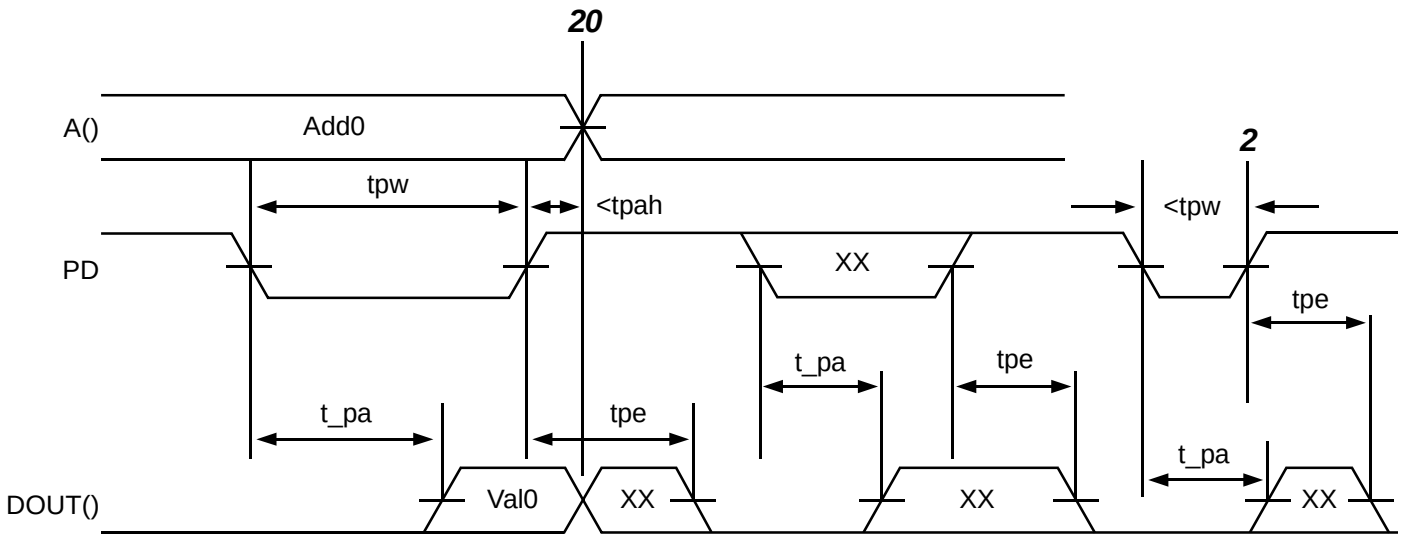
sram: CE = '0', WE = '1'



Notes: tpvz : Delay to propagate valid DOUT() to high impedance
tpzv : Delay to propagate high impedance to valid DOUT()

Single Port RAM Read Cycle 3

sram_pd: WE = '1'

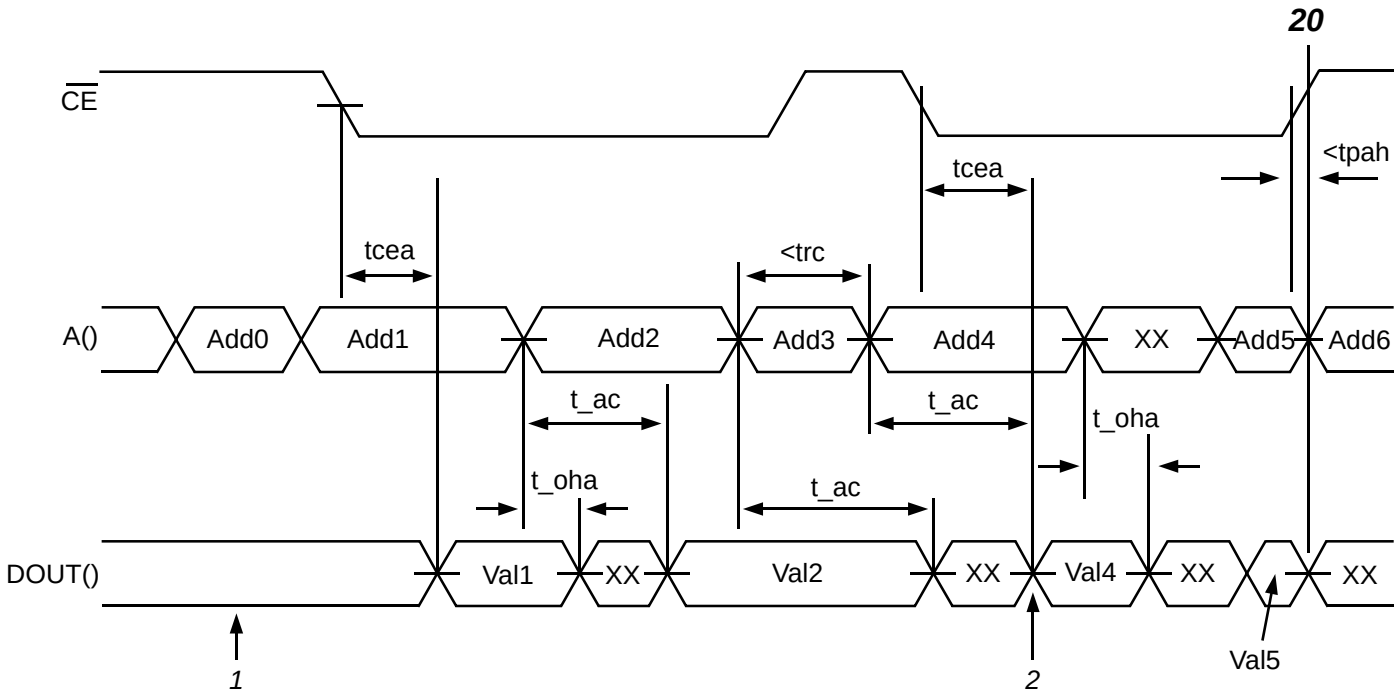


Notes: t_pa : Access time from PD
tpe : PD shutting off to DOUT() Fall
tpw : Minimum pulse width for PD
tpah : Address hold time from PD rising

***2**. Error: Illegal PD input: PD "Low" width time smaller than min. tpw.*
***20**. Error: Illegal address input: hold time to PD is smaller than min. tpah.*

Single Port RAM Read Cycle 4

sram: OE = '0', WE = '1'



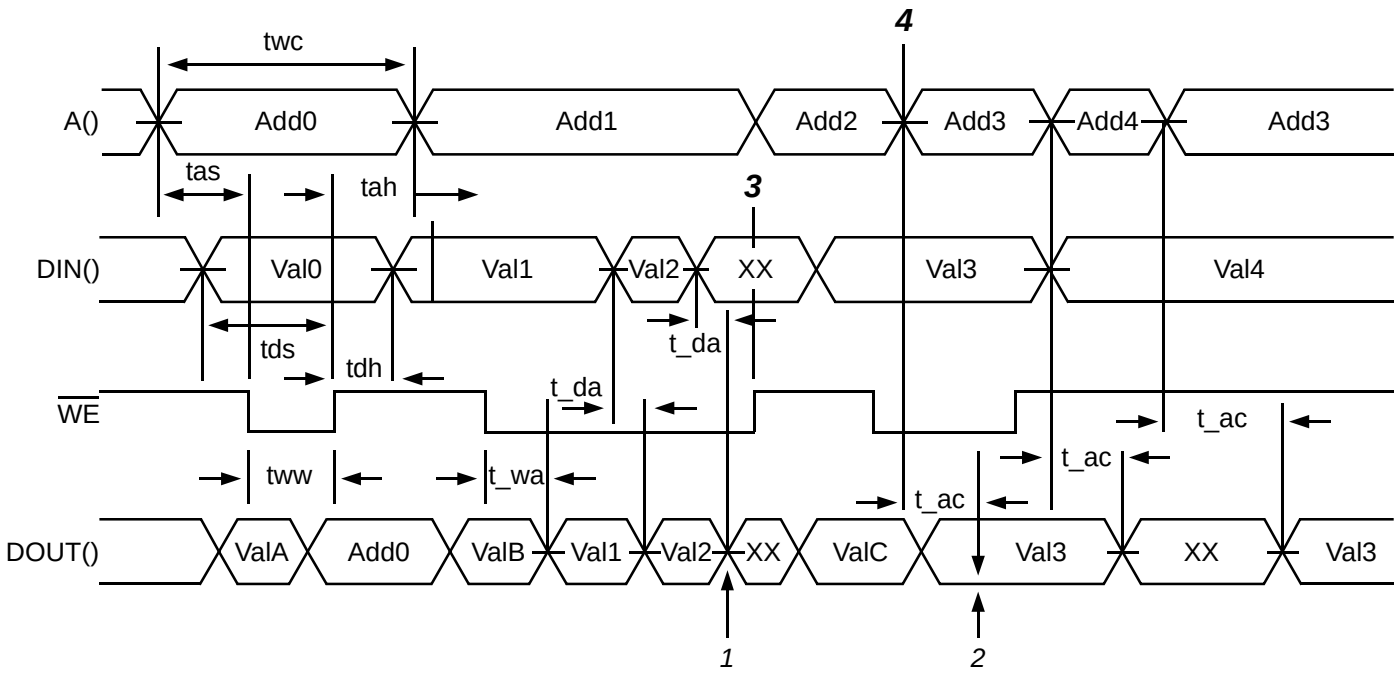
Notes: t_ac : Address access time
tcea : CE Access Time (maximum of Rise/Fall)
tpah : Address hold time from PD or CE rising
trc : Min. ready cycle time
t_oha : Output hold time from address change (minimum of Rise/Fall)

1. Normal DOUT() change due to address change is locked out by 'CE' pin set to '1'.
2. Output becomes valid after the MAX of t_ac or tcea. Note that the 'CE' pin rising does not trigger a RAM access.

***20**. Error: Illegal address input: hold time to CE/PD is smaller than min. tpah.*

Single Port RAM Write Cycle 1

sram : CE = '0', OE = '0'
sram_pd : PD = '0'



Notes:
- t_da : Output delay time from Data (t_da < t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from WE (MAX of Rise/Fall)
- t_ac : Address access time
- tas : Address setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tww : Write pulse width low
- twc : Write cycle time

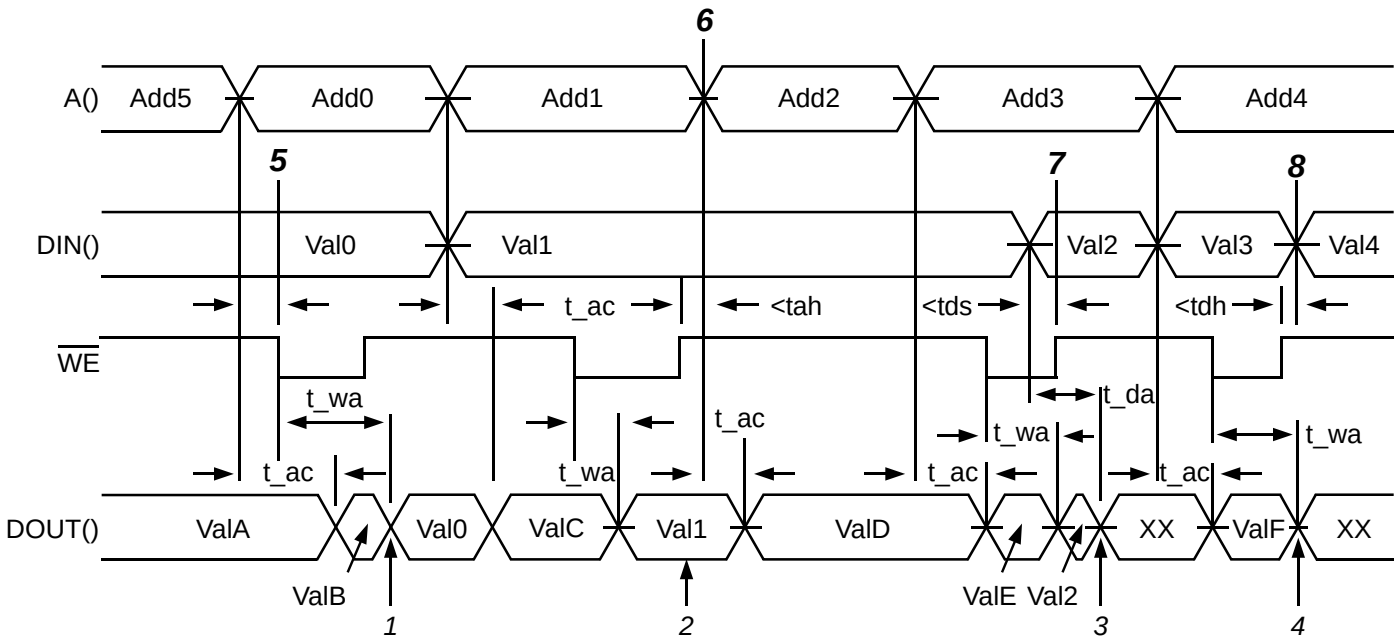
ValA, ValB, and ValC are previously retained in address Add0, Add1, and Add2

1. Data retained in Add1 is overwritten by 'X' at this time.
2. Data retained in all words is overwritten by 'X' at this time. Writing Val3 into Add3 should be successful.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of WE*
***4**. Error: Illegal Operation: Address was changed while WE low*

Single Port RAM Write Cycle 2

sram : CE = '0', OE = '0'
sram_pd : PD = '0'



Notes:
t_da : Output delay time from Data (t_da < t_ac) (MAX of Rise/Fall)
t_wa : Output delay time from WE (MAX of Rise/Fall)
t_ac : Address access time
tah : Address hold time
tds : Data setup time
tdh : Data hold time
tas : Address setup time

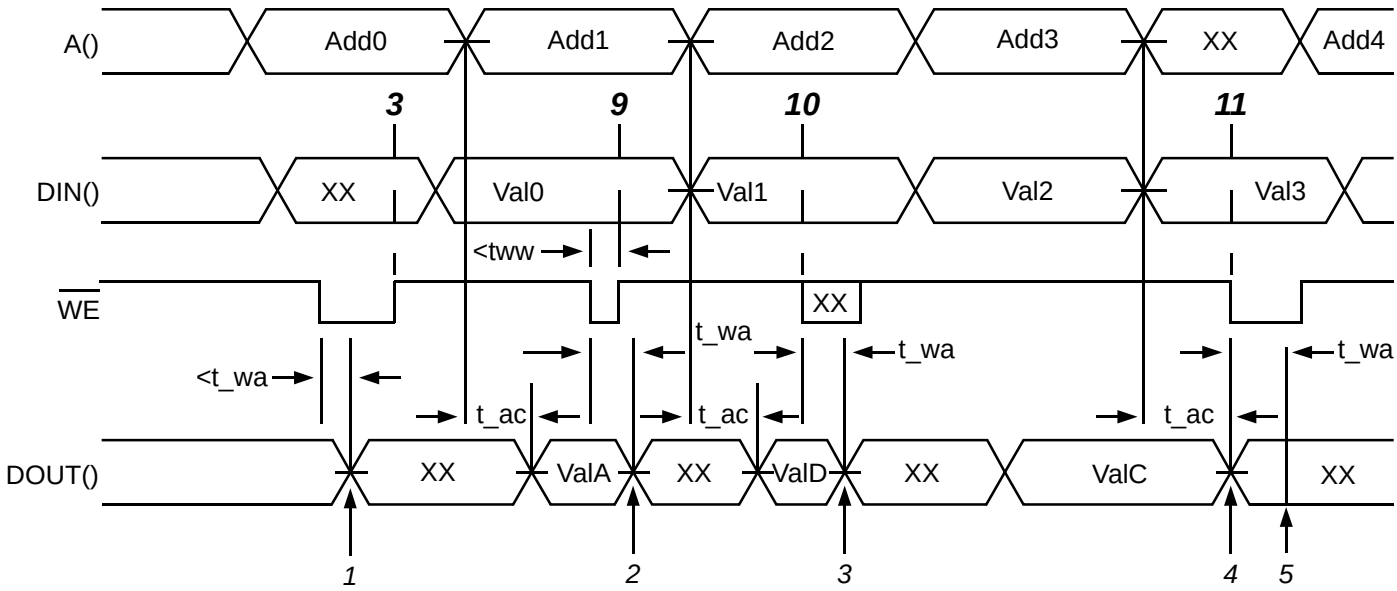
ValA-ValF are previously retained in Add5-Add4.

1. Data retained in all words is overwritten by 'X' at this time. Writing Val0 into Add0 should be successful.
2. Data retained by all words is overwritten by 'X' at this time.
3. Data retained in Add3 is overwritten by 'X' at this time.
4. Data retained in Add4 is overwritten by 'X' at this time.

***5**. Error: Illegal Address Input: Address setup time to WE is smaller than Min tas.*
***6**. Error: Illegal Address Input: Address hold time to WE is smaller than Min tah.*
***7**. Error: Illegal Data Input: DIN setup time to WE is smaller than Min tds.*
***8**. Error: Illegal Data Input: DIN hold time to WE is smaller than Min tdh.*

Single Port RAM Write Cycle 3

sram : CE = '0', OE = '0'
sram_pd : PD = '0'

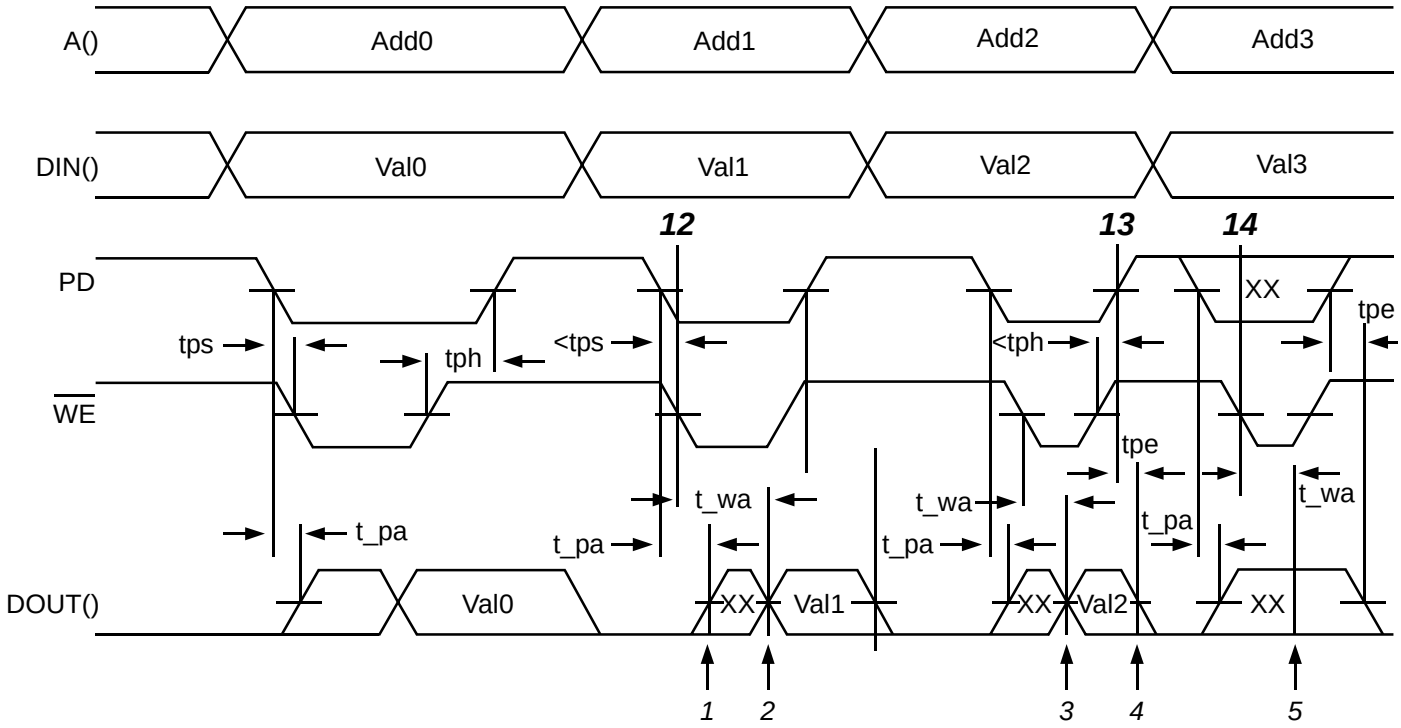


Notes: t_wa : Ouput delay time from $\overline{WE}$ (MAX of Rise/Fall)
t_ac : Address access time
tww : Write pulse width low

1. Data retained in Add0 is overwritten by 'X' at this time.
2. Data retained in Add1 is overwritten by 'X' at this time.
3. Data retained in Add2 is overwritten by 'X' at this time.
4. DOUT() becomes 'X' after t_ac time from leading edge of address 'X'.
5. Data retained in all words is overwritten by 'X' after t_wa time from falling edge of $\overline{WE}$.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{WE}$.*
***9**. Error: Illegal $\overline{WE}$ Input: $\overline{WE}$ "Low" width time is smaller than Min tww.*
***10**. Error: Illegal Operation: $\overline{WE}$ input went to "X".*
***11**. Error: Illegal Operation: Address was "X" at the falling edge of $\overline{WE}$.*

Single Port RAM Write Cycle 4 (sram_pd)



Notes: tps : $\overline{CE}$/PD setup time (PD pin used for zero_out function)
tph : $\overline{CE}$/PD hold time (PD pin used for zero_out function)
t_wa : Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
t_pa : Access time from $\overline{CE}$/PD
tpe : $\overline{CE}$/PD shutting off to DOUT() Fall

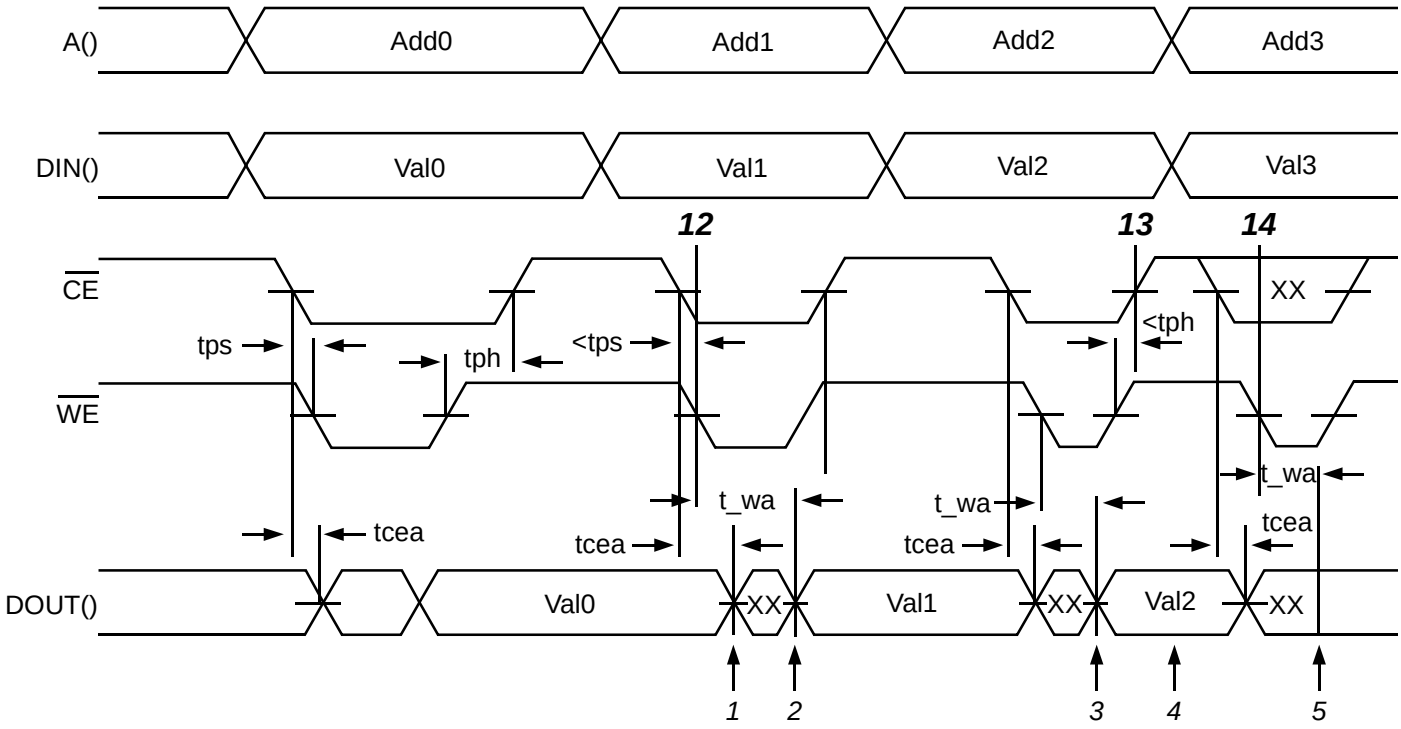
1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If Data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD setup time to $\overline{WE}$ is smaller than Min tps.*
***13**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD hold time to $\overline{WE}$ is smaller than Min tph.*
***14**. Error: Illegal Operation: $\overline{CE}$/PD was "X" at the falling edge of $\overline{WE}$.*

CMOS ASIC Standard Cell Memories

Single Port RAM Write Cycle 5

sram: OE = '0'

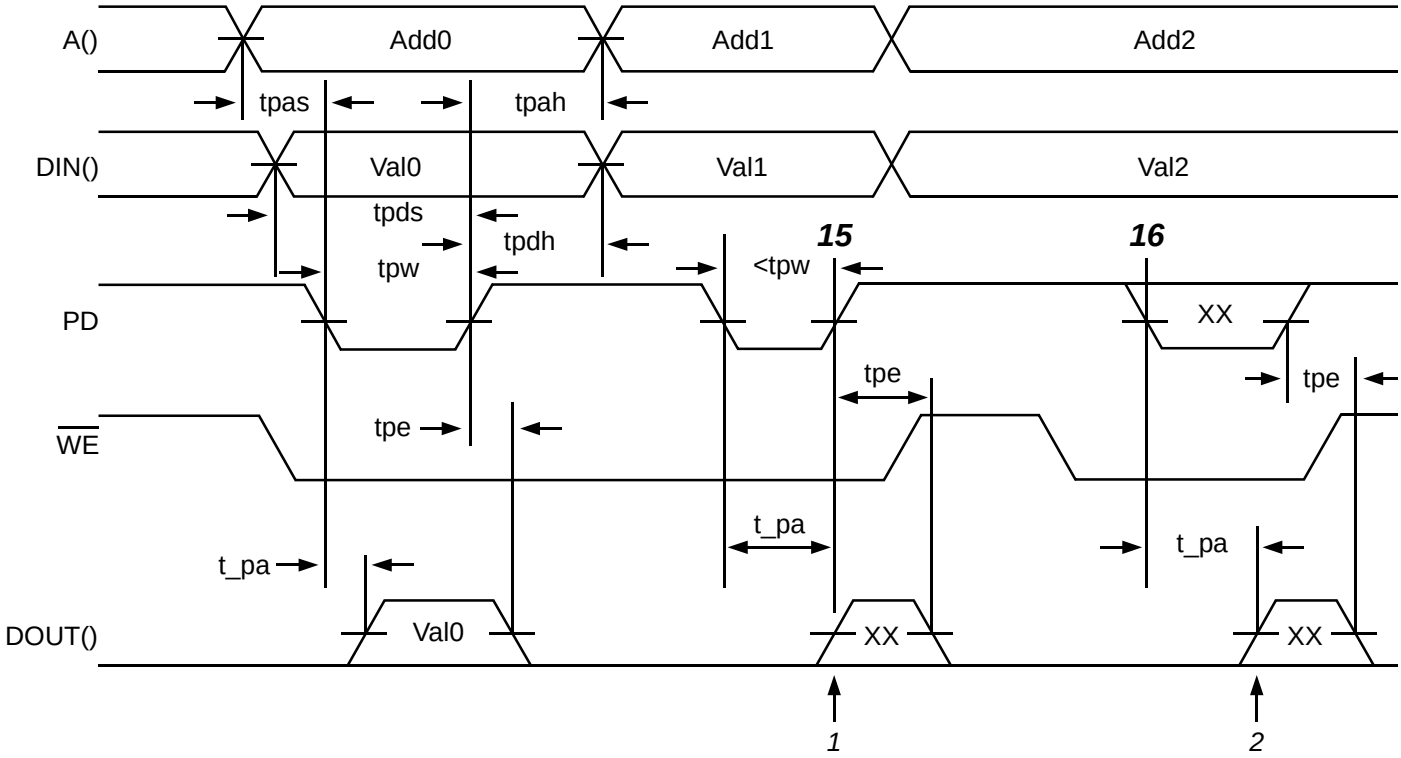


Notes: tps : $\overline{CE}$/PD setup time
tph : $\overline{CE}$/PD hold time
t_wa : Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
tcea : Access time from $\overline{CE}$

1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If Data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD setup time to $\overline{WE}$ is smaller than Min tps.*
***13**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD hold time to $\overline{WE}$ is smaller than Min tph.*
***14**. Error: Illegal Operation: $\overline{CE}$/PD was "X" at the falling edge of $\overline{WE}$.*

Single Port RAM Write Cycle 6 (sram_pd)



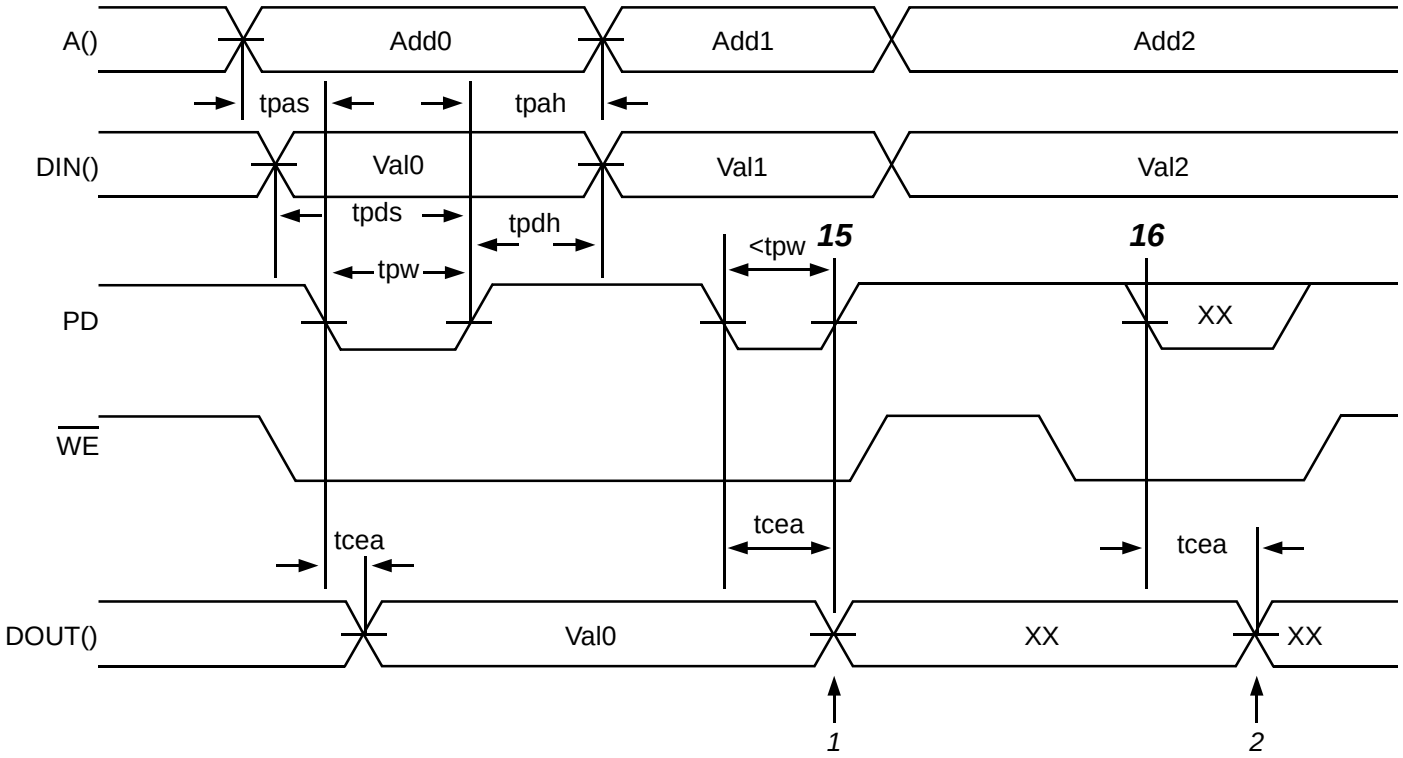
Notes:
- tpas : Address setup time to $\overline{CE}$/PD (PD pin used for zero_out function)
- tpah : Address hold time to $\overline{CE}$/PD (PD pin used for zero_out function)
- tpds : Data setup time to $\overline{CE}$/PD
- tpdh : Data hold time to $\overline{CE}$/PD
- t_pa : Access time from $\overline{CE}$/PD
- tpe : PD shutting off to DOUT() Fall
- tpw : Minimum pulse width for $\overline{CE}$/PD

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{CE}$/PD input: $\overline{CE}$/PD "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{CE}$/PD went "X" while $\overline{WE}$ is "Low".*

CMOS ASIC Standard Cell Memories

Single Port RAM Write Cycle 7 (sram)

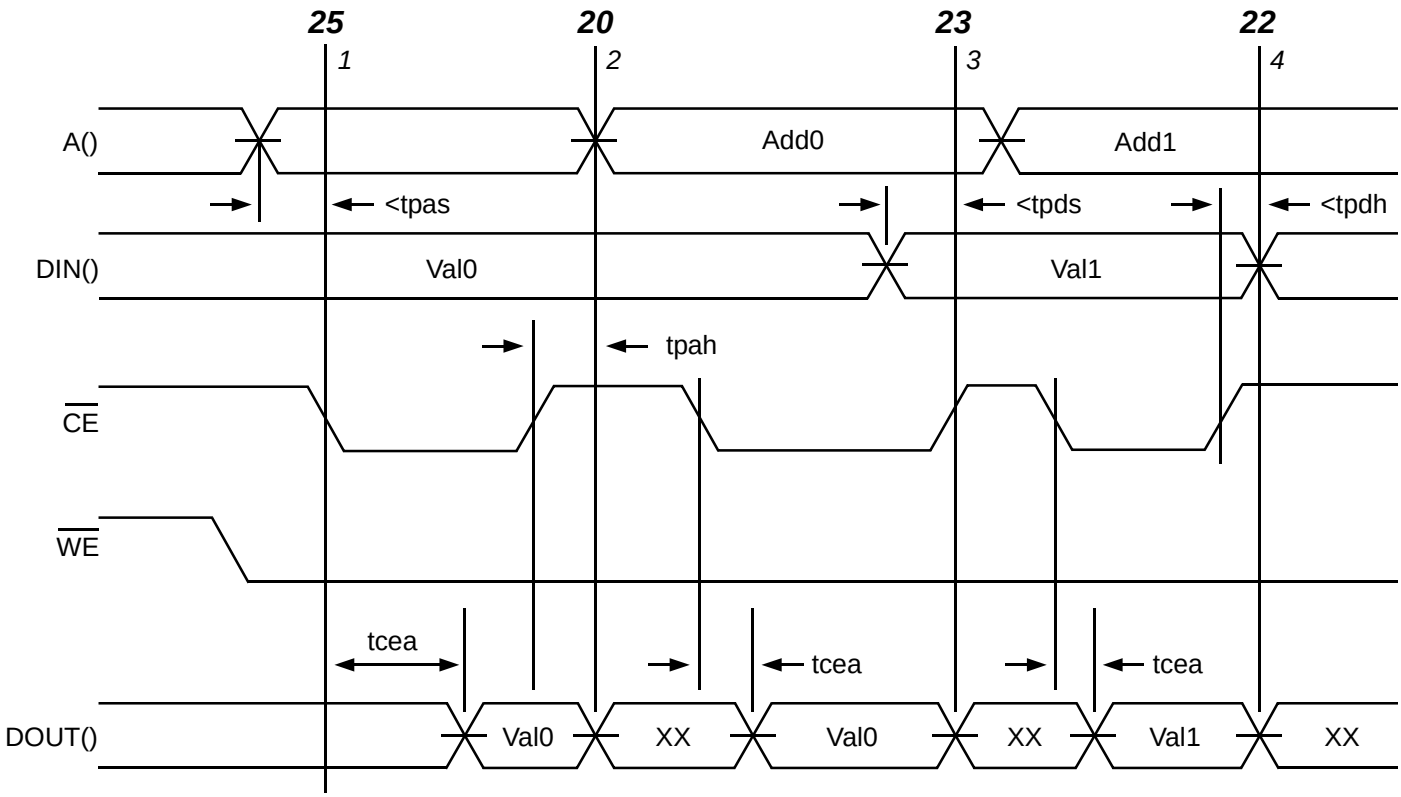


Notes:
- tpas : Address setup time to $\overline{CE}$/PD
- tpah : Address hold time to $\overline{CE}$/PD
- tpds : Data setup time to $\overline{CE}$/PD
- tpdh : Data hold time to $\overline{CE}$/PD
- tcea : Access time from $\overline{CE}$
- tpe : PD shutting off to DOUT() Fall
- tpw : Minimum pulse width from $\overline{CE}$/PD

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X' at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{CE}$/PD input: $\overline{CE}$/PD "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{CE}$/PD went "X" while $\overline{WE}$ is "Low".*

Single Port RAM Write Cycle 8 (sram)

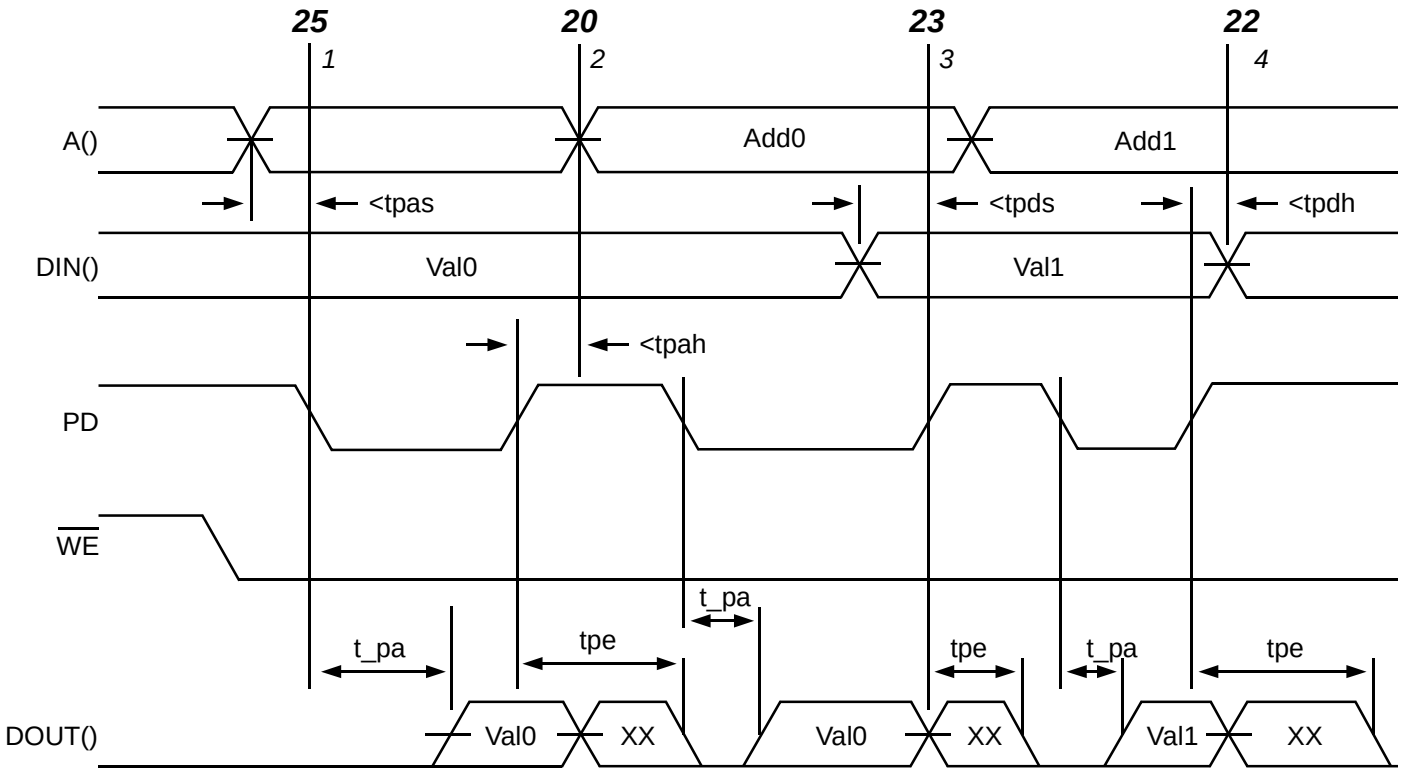


Notes: tpas : Address setup time to $\overline{CE}$/PD
tpah : Address hold time to $\overline{CE}$/PD
tpds : Data setup time to $\overline{CE}$/PD
tpdh : Data setup time to $\overline{CE}$/PD
tcea : Access time from $\overline{CE}$

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

20. Error: Illegal address input: hold time to $\overline{CE}$/PD is smaller than min. tpah.
22. Error: Illegal data input: DIN hold time to $\overline{CE}$/PD is smaller than min. tpdh.
23. Error: Illegal data input: DIN setup time to $\overline{CE}$/PD is smaller than min. tpds.
25. Error: Illegal address input: setup time to $\overline{CE}$/PD is smaller than min. tpas.

Single Port RAM Write Cycle 9 (sram_pd)



Notes: tpas : Address setup time to $\overline{CE}$/PD
tpah : Address hold time to $\overline{CE}$/PD
tpds : Data setup time to $\overline{CE}$/PD
tpdh : Data hold time to $\overline{CE}$/PD
t_pa : Access time from PD
tpe : PD shutting off to DOUT() Fall

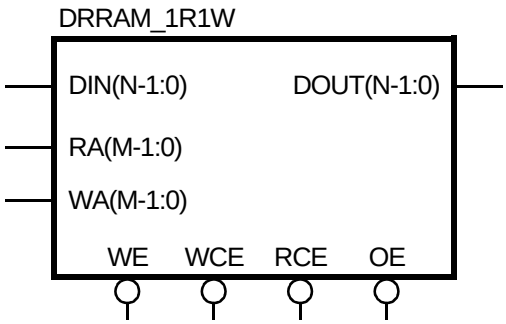
1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

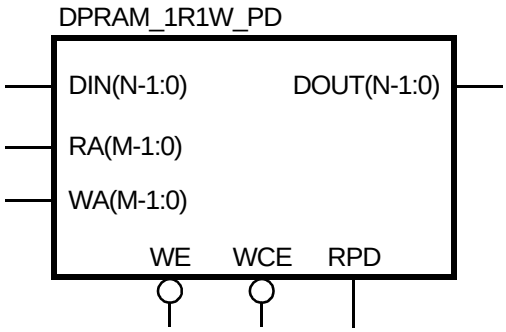
***20**. Error: Illegal address input: hold time to $\overline{CE}$/PD is smaller than min. tpah.*
***22**. Error: Illegal data input: DIN hold time to $\overline{CE}$/PD is smaller than min. tpdh.*
***23**. Error: Illegal data input: DIN setup time to $\overline{CE}$/PD is smaller than min. tpds.*
***25**. Error: Illegal address input: setup time to $\overline{CE}$/PD is smaller than min. tpas.*

Features

- 8-T memory cell design
- Simple combinational logic decoding
- Small bitline differential in read mode eliminates precharge delay
- Fast ATD circuit turns on wordlines and sense amps only as needed to save power while allowing asynchronous operation

Logic Symbol





DPRAM_1R1W
High Speed Low-Power Dual Port RAM

CMOS ASIC Standard Cell Memories

DPRAM_1R1W: High Speed Low-Power Dual Port Description

AMI Semiconductor's high speed, low power CMOS RAM is available in both single and dual port versions. Column select passgates provide a cascode gain stage, followed by a differential voltage sense amp. The memory array columns may be multiplexed to optimize the aspect ratio. Multiplexing of columns, or column folding, shortens the bitline length (reduces the number of rows in the array) while increasing the width of the memory array. No change in the total memory bit count occurs.

The zero_out option sends the outputs all to "zero". This operation is controlled by the PD signal.

The RAM draws current only in response to changing inputs, minimizing power consumption and allowing complete IDDQ testing. Address changes activate the sense amps and one row of memory cells for a period of time longer than access time. The current drawn by each sense amp is comparable to the read current of each memory cell.

DPRAM_1R1W High speed Low-Power dual Port RAM.

Signal Summary

INPUTS		OUTPUTS	
PORT LABLE	FUNCTION	PORT LABEL	FUNCTION
RA	Read Address	DOUT	Output Data
WA	Write Address		
DIN	Input Data		
RCE	Read Chip Enable, active low		
WCE	Write Chip Enable, active low		
WE	Write Enable, active low		
OE	Output Enable, active low		
RPD	Read Power Down, active high, read cycle disabled and output driven to zero (0) when active		

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
WORDS	number of words	Integer	8-16384
N	bits per word	Integer	1-144
M	address size	Integer	3-14
BPC	bits per column	Integer	2, 4, 8, 16, 32
FLOORPLAN	auto floorplan	Integer	0, 1
BUFFER_SIZE	buffer size	String	1-6
FREQUENCY	frequency in MHz	Integer	1-100
VDROP	voltage drop in millivolts	Integer	1-249

Block height range is 4-512; block width range is 4-288; max total bits is 144K (16K x 9).

BPC Options

BPC VALUE	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT	MINIMUM BITS	MAXIMUM BITS
2	8	1024	4	1	144
4	16	2048	8	1	72
8	32	4096	16	1	36
16	64	8192	32	1	18
32	128	16384	64	1	9

DPRAM_1R1W
High Speed Low-Power Dual Port RAM

CMOS ASIC Standard Cell Memories

Parts

PART NAME	PINS
dpram_1r1w	DIN, OE, RA, RCE, WA, WCE, WE, DOUT
dpram_1r1w_pd	DIN, RA, RPD, WA, WCE, WE, DOUT

Truth Tables

zero-out option false

INPUTS					OUTPUTS	COMMENT
RA, WA	WCE, RCE	OE	DIN	WE	DOUT	
0/1	0	0	X	1	Data	Read
X	0	1	X	1	Z	Output Disabled (standard) - RAM Active
X	1	1	X	X	Z	Output Disabled (standard) - RAM Disabled
X	1	0	X	X	Data	Outputs Stable, RAM Disabled
0/1	0	0	0/1	0	Data	Write with Write-Through
0/1	0	1	0/1	0	Z	Write

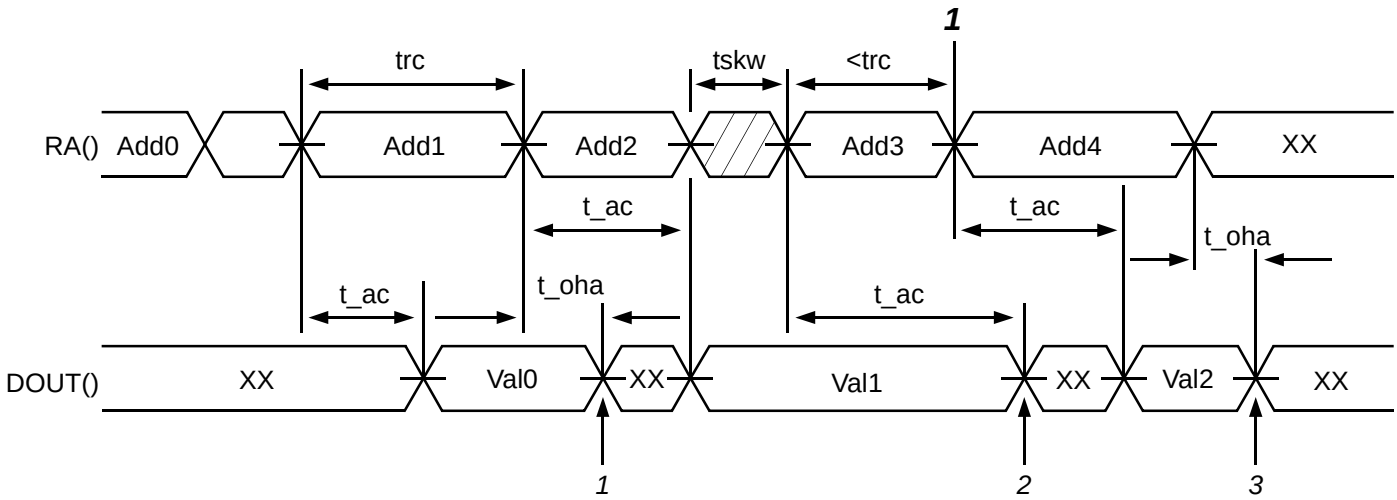
zero-out option true

INPUTS					OUTPUTS	COMMENT
RA, WA	RPD	DIN	WCE	WE	DOUT	
X	1	X	1	X	0	Output Disabled (zero_out), RAM Disabled
0/1	0	X	1	1	Data	Read
0/1	0	0/1	0	0	Data	Write with Write-Through
0/1	1	0/1	0	0	0	Write without Write-Through

SWITCHING TIME WAVEFORMS

Dual Port RAM 1R1W Read Cycle 1

dpram_1r1w : WE = '1', OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WE = '1', WCE = '0', RPD = '0'



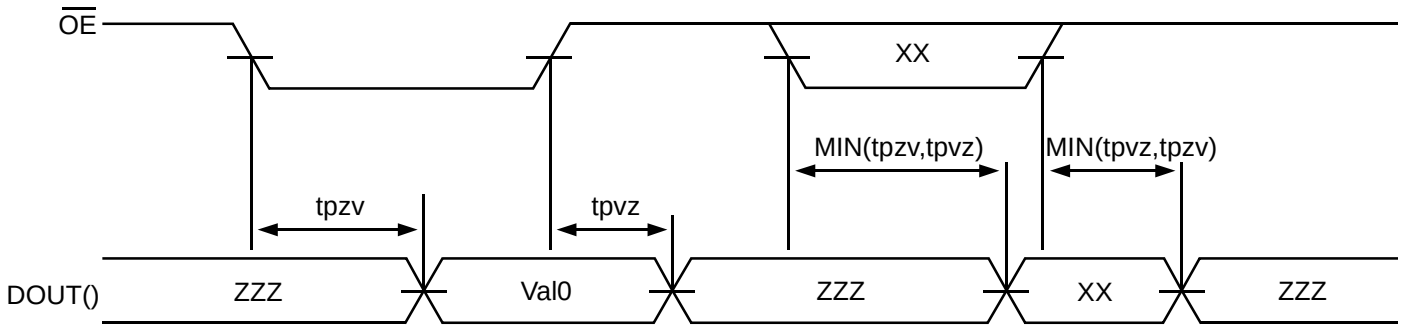
Notes: t_ac : Address Access Time (maximum of Rise/Fall)
trc : Read Cycle Time
t_oha : Output Hold Time from Address Change (minimum of Rise/Fall)
tskw : All addresses must complete transition within this time

1. t_oha delay will only be applied to the last data accessed, otherwise, t_ac will be used for the pin-to-pin delay.
2. trc = t_ac. If Add3 width is less than trc, DOUT() goes to'X'.
3. If A() becomes 'X', DOUT() goes 'X' after time t_oha.

***1**. Error: Illegal Address input: Address cycle time is smaller than minimum trc.*

Dual Port RAM 1R1W Read Cycle 2

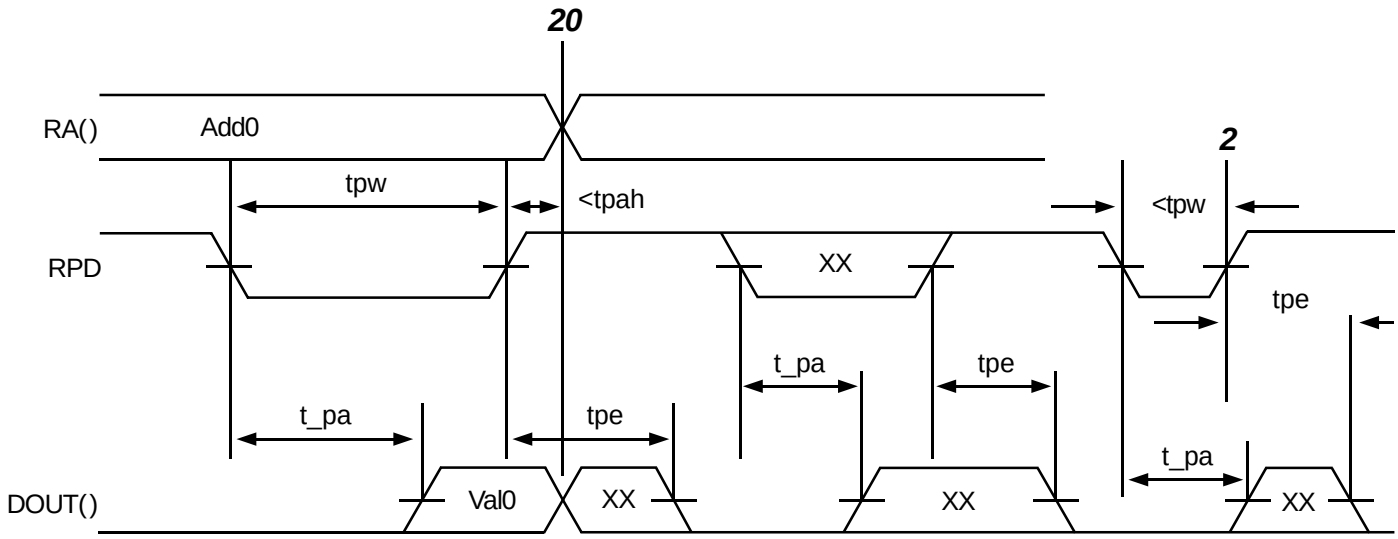
dpram_1r1w: WE = '1', WCE = '0', RCE = '0'



Notes: tpvz : Delay to propagate valid DOUT() to high impedance
tpzv : Delay to propagate high impedance to valid DOUT()

Dual Port RAM 1R1W Read Cycle 3

dpram_1r1w_pd: WE = '1', WCE = '0'

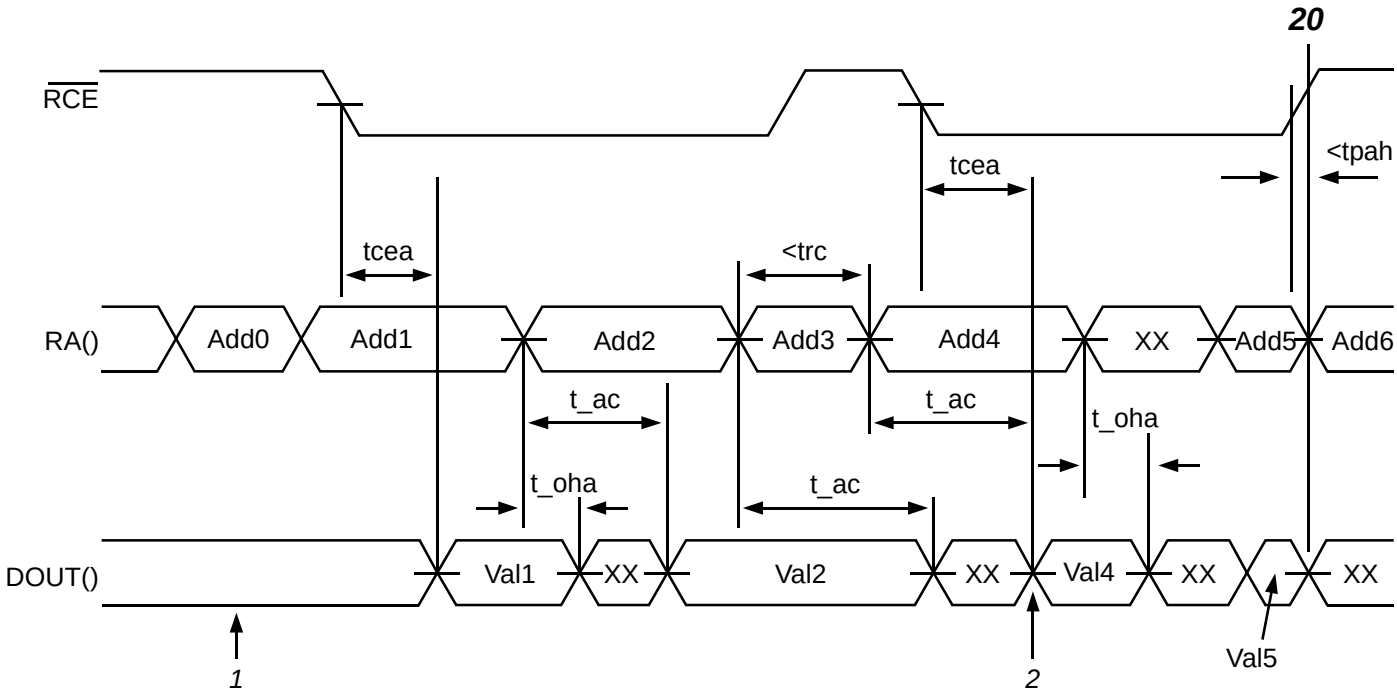


Notes: t_pa : Access time from RPD
tpe : RPD shutting off to DOUT() Fall
tpw : Minimum pulse width for RPD
tpah : Address hold time from RPD rising

2. Error: Illegal RPD input: RPD "Low" width time smaller than Min tpw.
20. Error: Illegal address input: hold time to RPD is smaller than min. tpah.

Dual Port RAM 1R1W Read Cycle 4

dpram_1r1w: WE = '1', WCE = '0', OE = '0'



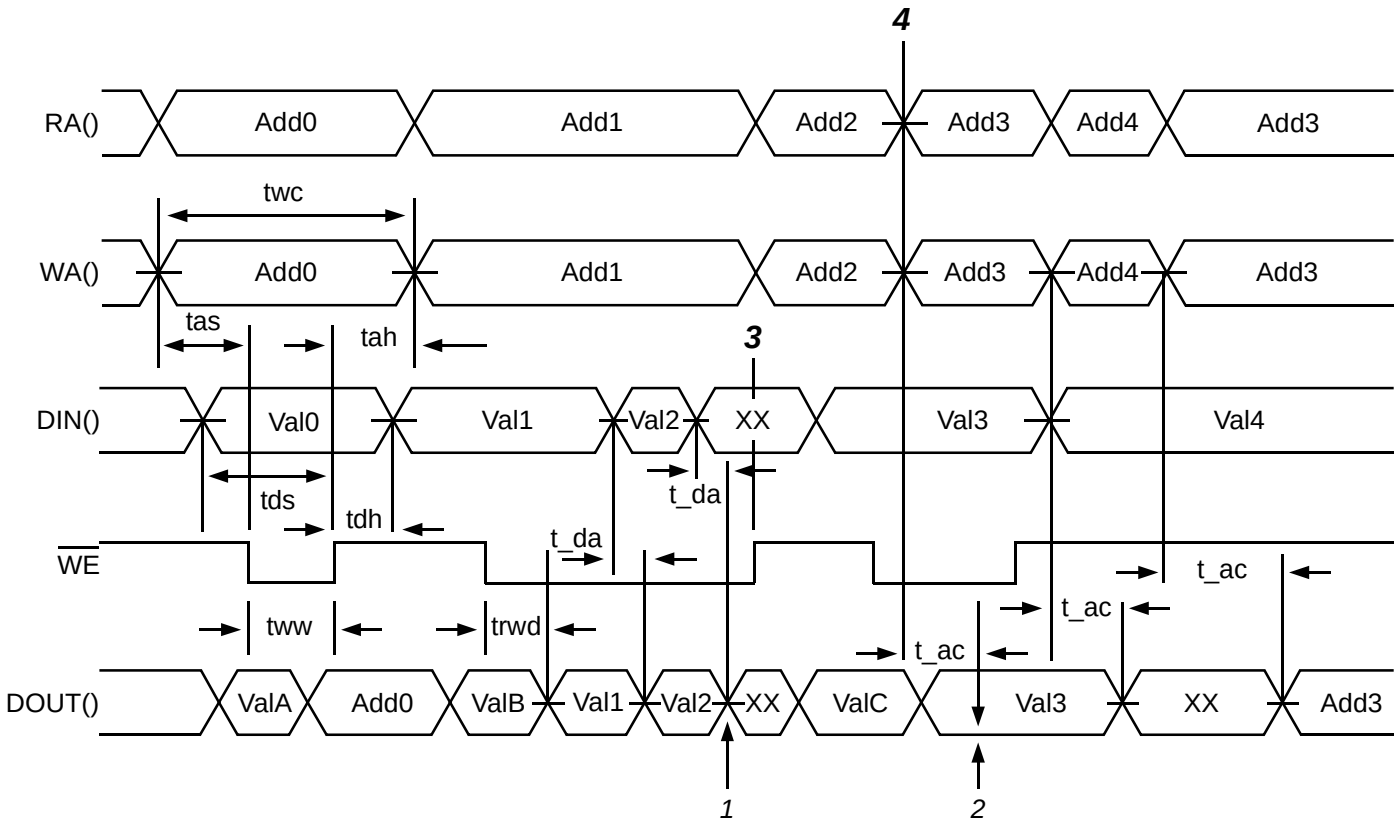
Notes: t_ac : Address access time
tcea : RCE access time (maximum of Rise/Fall)
tpah : Address hold time from RCE rising
trc : Read cycle time
t_oha : Output hold time from address change (minimum of Rise/Fall)

1. Normal DOUT() change due to address change is locked out by RCE pin set to '1'.
2. Output becomes valid after the MAX of t_ac or tcea. Note that the RCE pin rising does not trigger a RAM access.

***20**. Error: Illegal address input: hold time to RCE is smaller than min. tpah.*

Dual Port RAM 1R1W Write Cycle 1

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



Notes:
- t_da : Output delay time from Data (t_da < t_ac) (MAX of Rise/Fall)
- trdw : Data access for a write-through operation
- t_ac : Address access time
- tas : Address setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tww : White pulse width low
- twc : Write cycle time

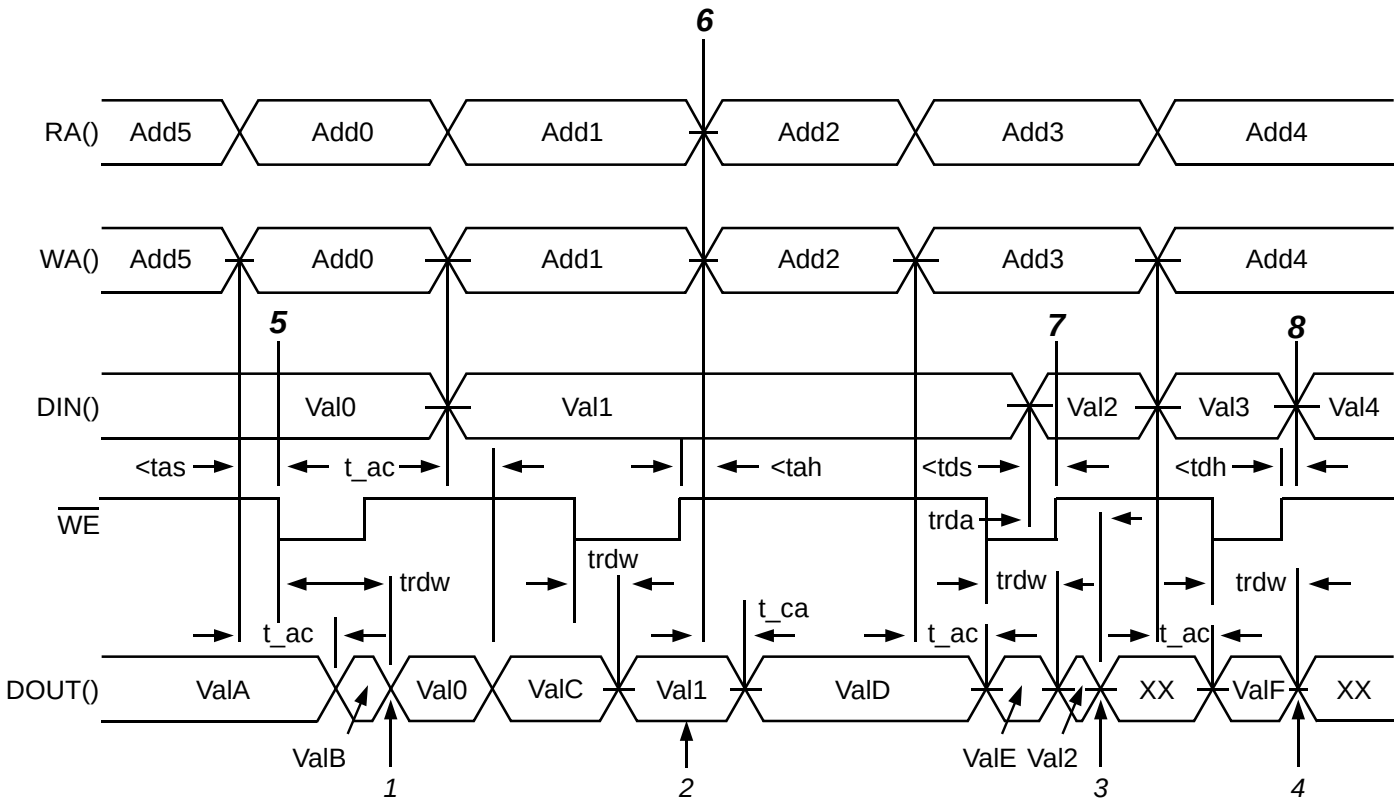
ValA, ValB, and ValC are previously retained in address Add0, Add1, and Add2.

1. Data retained in Add1 is overwritten by 'X' at this time.
2. Data retained in all words is overwritten by 'X' at this time. Writing Val3 into Add3 should be successful.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{WE}$.*
***4**. Error: Illegal Operation: Address was changed while $\overline{WE}$ low.*

Dual Port RAM 1R1W Write Cycle 2

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



Notes: t_ac : Address access time
trda : Output delay time from DIN to DOUT (<t_ac) (MAX of Rise/Fall)
trdw : Data access for a write-through operation
tas : Address setup time
tah : Address hold time
tds : Data setup time
tdh : Data hold time

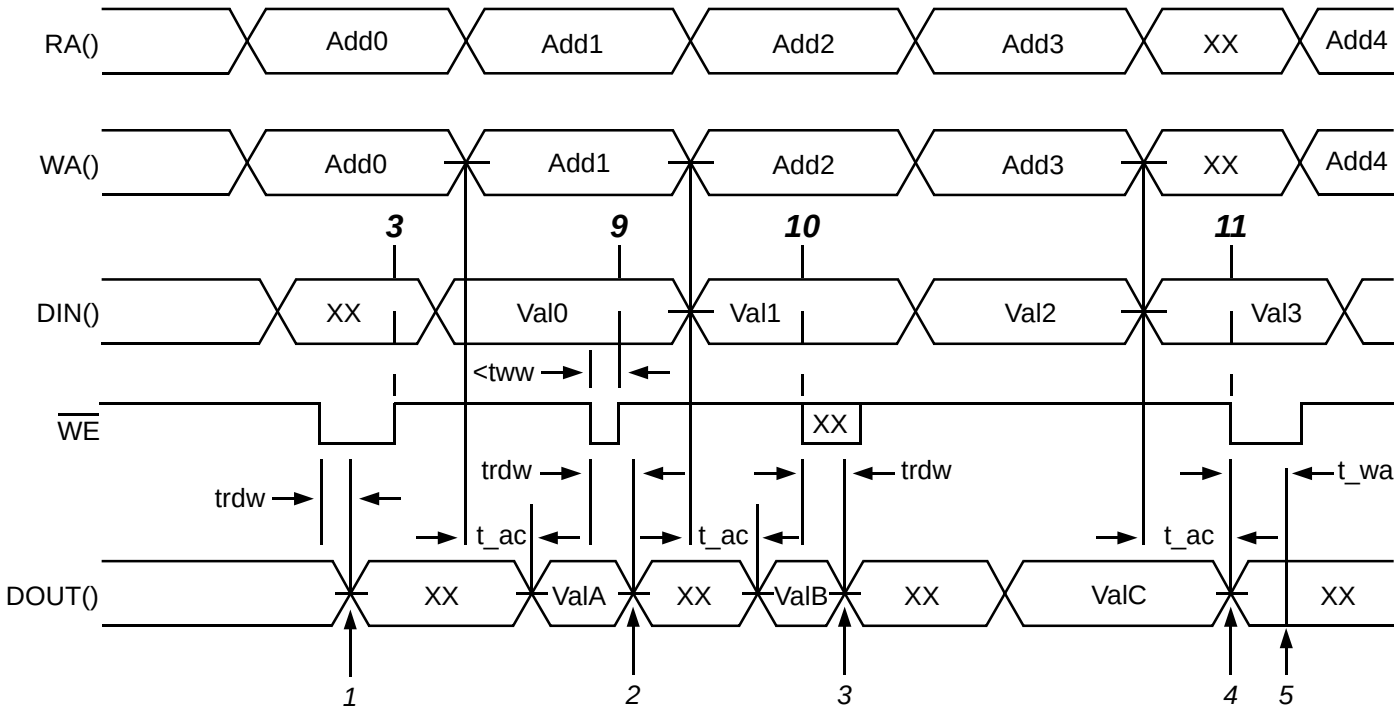
ValA-ValF are previously retained in Add5-Add4.

1. Data retained in all words is overwritten by 'X' at this time. writing Val0 into Add0 should be successful.
2. Data retained by all words is overwritten by 'X' at this time.
3. Data retained in Add3 is overwritten by 'X' at this time.
4. Data retained in Add4 is overwritten by 'X' at this time.

***5**. Error: Illegal Address Input: Address setup time to $\overline{WE}$ is smaller than Min tas.*
***6**. Error: Illegal Address Input: Address hold time to $\overline{WE}$ is smaller than Min tah.*
***7**. Error: Illegal Data Input: DIN setup time to $\overline{WE}$ is smaller than Min tds.*
***8**. Error: Illegal Data Input: DIN hold time to $\overline{WE}$ is smaller than Min tdh.*

Dual Port RAM 1R1W Write Cycle 3

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



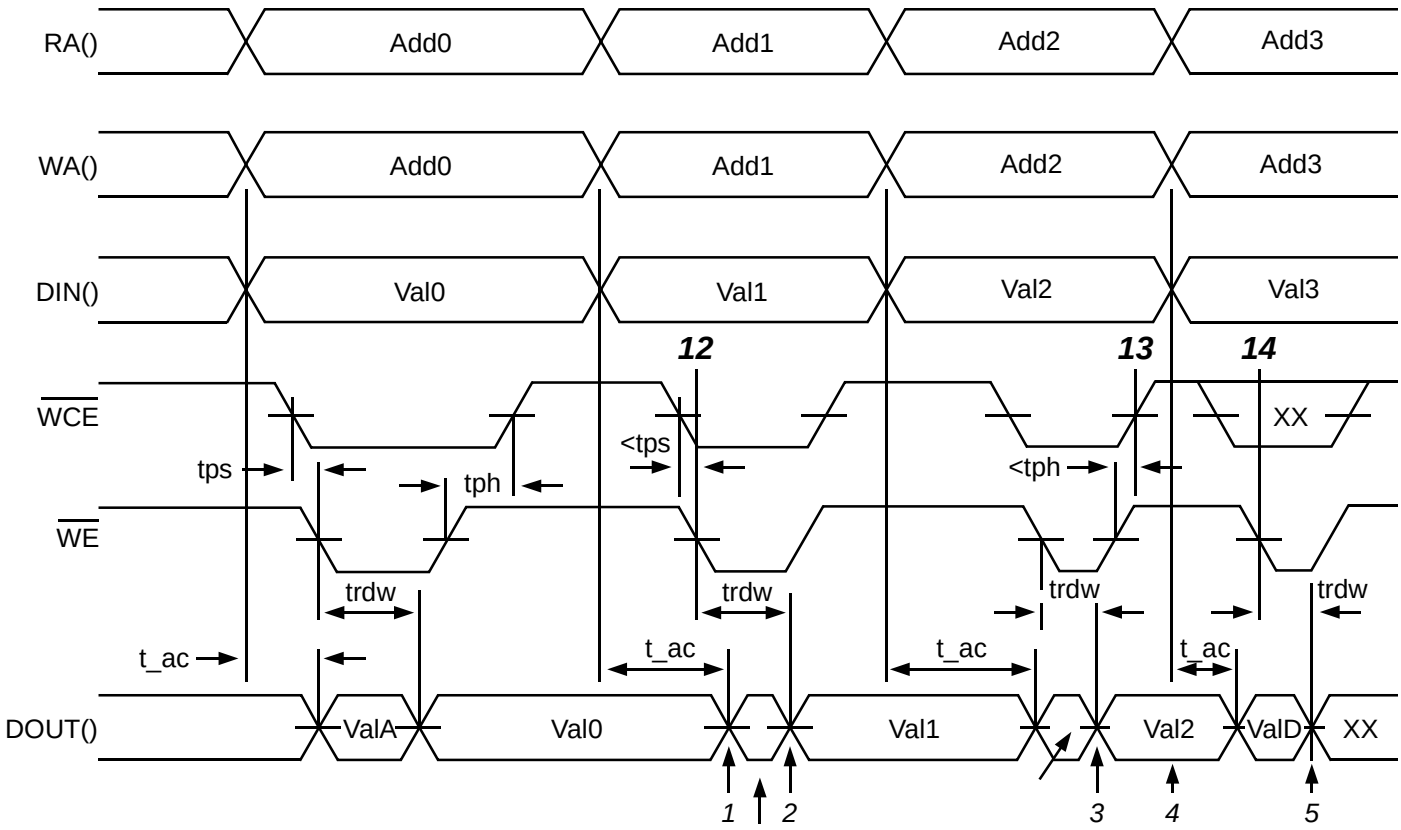
Notes: trdw : Data access for a write-through operation
t_wa : Output delay time from $\overline{WE}$ (Max of Rise/Fall)
t_ac : Address access time
tww : Write pulse width low

1. Data retained in Add0 is overwritten by 'X' at this time.
2. Data retained in Add1 is overwritten by 'X' at this time.
3. Data retained in Add2 is overwritten by 'X' at this time.
4. DOUT() becomes 'X' after t_ac time from leading edge of address 'X'.
5. Data retained in all words is overwritten by 'X' after t_wa time from falling edge of $\overline{WE}$.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{WE}$.*
***9**. Error: Illegal WE input: WE "Low" width time is smaller than Min tww.*
***10**. Error: Illegal Operation: $\overline{WE}$ input went to "X".*
***11**. Error: Illegal Operation: Address was "X" at the falling edge of $\overline{WE}$.*

Dual Port RAM 1R1W Write Cycle 4, and Write Cycle 5

dpram_1r1w_pd : RPD = '0'
dpram_1r1w : RCE = '0', OE = '0'



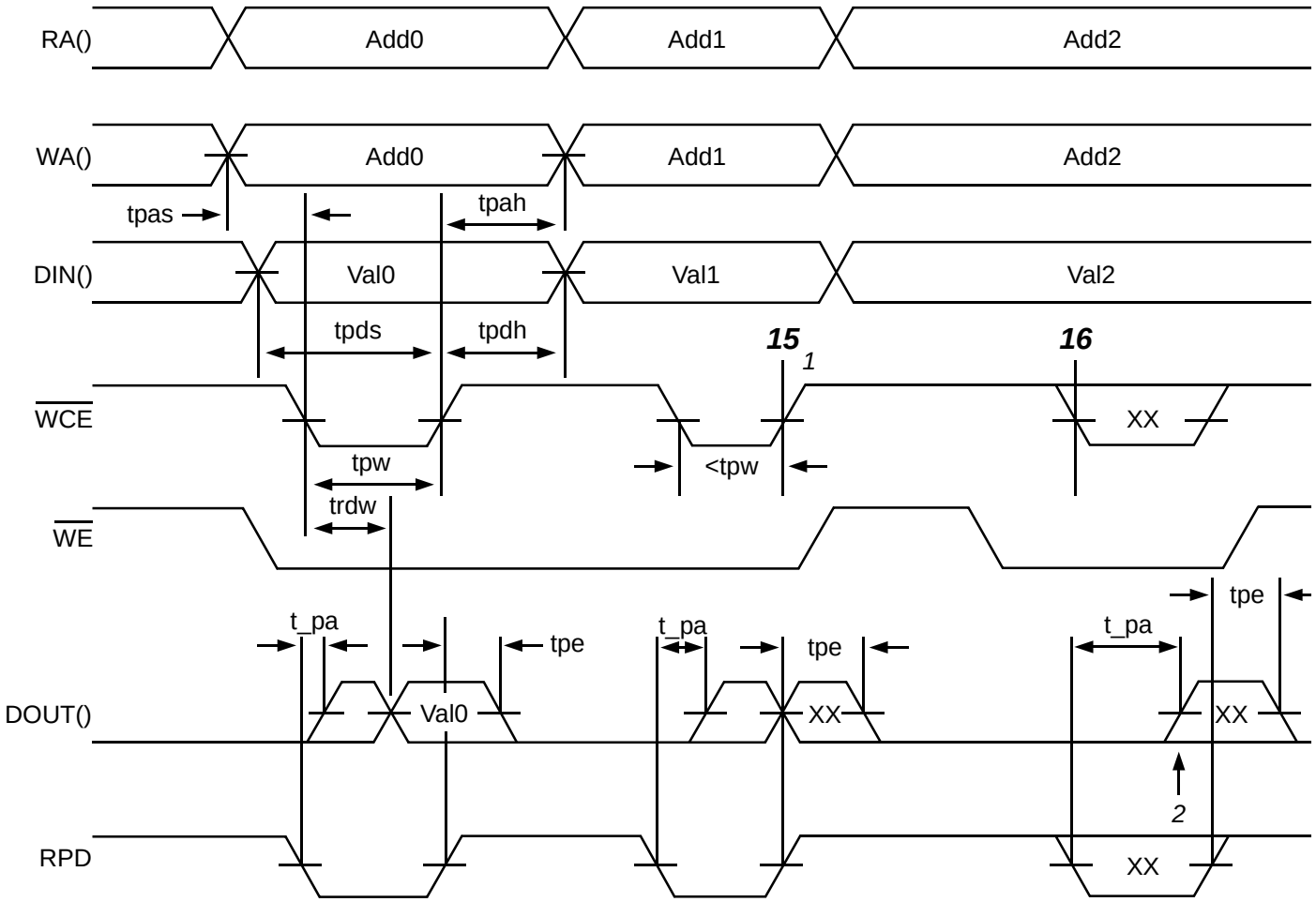
Notes: tps : $\overline{WCE}$/RPD setup time
tph : PD hold time
trdw : Data access for a write-through operation
t_ac : Address access time

ValA-ValD are previously retained in address Add0-Add3.

1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If Data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal RPD Input: RPD setup time to $\overline{WE}$ is smaller than Min tps.*
***13**. Error: Illegal RPD Input: RPD hold time to $\overline{WE}$ is smaller than Min tph.*
***14**. Error: Illegal Operation: RPD was "X" at the falling edge of $\overline{WE}$.*

Dual Port RAM 1R1W Write Cycle 6 (dpram_1r1w_pd)

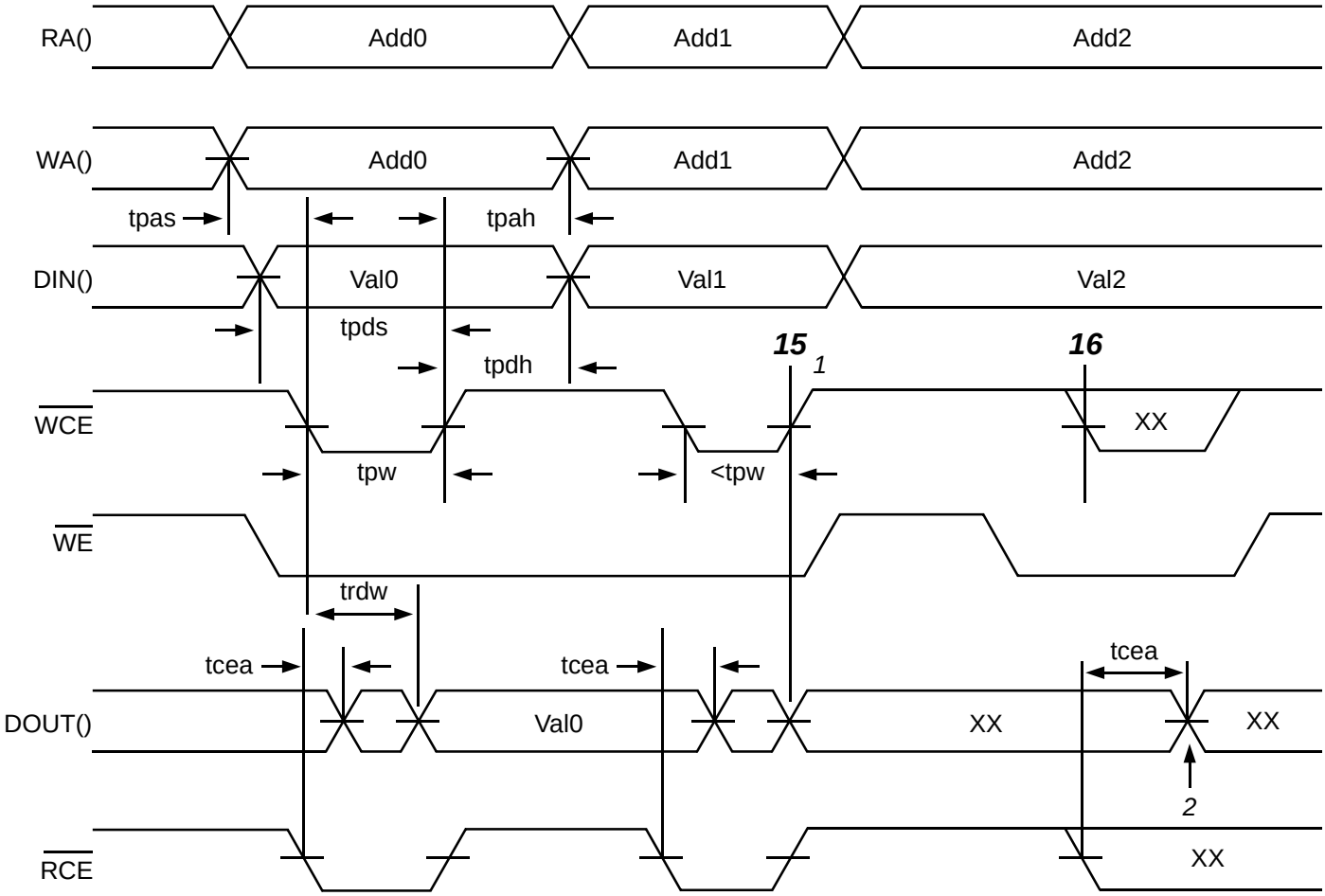


Notes:
- tpas : Address setup time to $\overline{WCE}$
- tpah : Address hold time to $\overline{WCE}$
- tpds : Data setup time to $\overline{WCE}$
- tpdh : Data hold time to $\overline{WCE}$
- t_pa : Access time from RPD
- tpe : RPD shutting off to DOUT() Fall
- tpw : Minimum pulse width for $\overline{WCE}$
- trdw : Data access for a write-through operation

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{WCE}$ input: $\overline{WCE}$ "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{WCE}$ went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 1R1W Write Cycle 7 (dpram_1r1w)



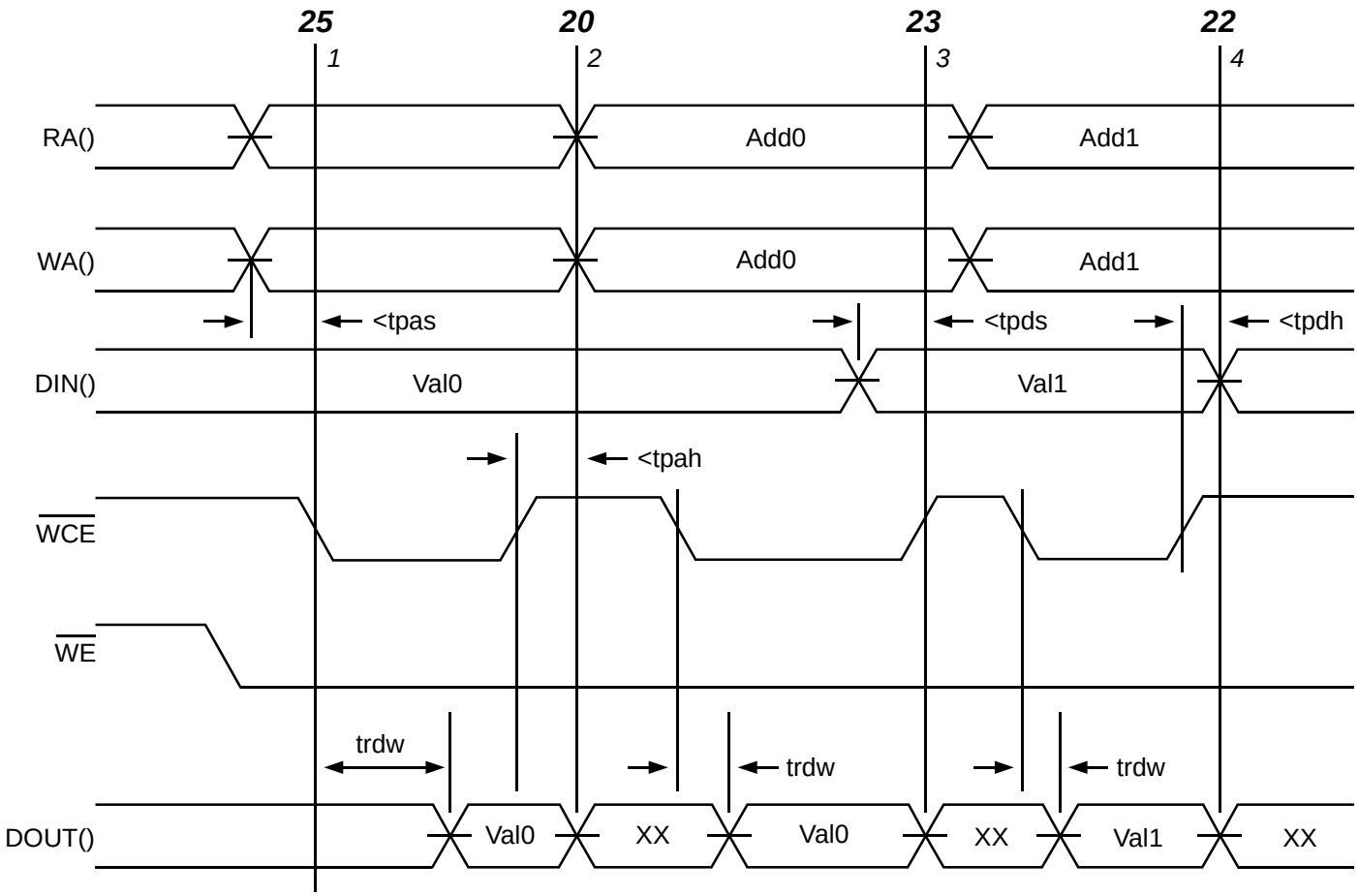
Notes:
- tpas : Address setup time to $\overline{WCE}$
- tpah : Address hold time to $\overline{WCE}$
- tpds : Data setup time to $\overline{WCE}$
- tpdh : Data hold time to $\overline{WCE}$
- tcea : Access time from RCE
- tpw : Minimum pulse width for $\overline{WCE}$
- trdw : Data access for a write-through operation

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{WCE}$ input: $\overline{WCE}$ "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{WCE}$ went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 1R1W Write Cycle 8, Write Cycle 9

dpram_1r1w_pd : RPD = '0'
dpram_1r1w : RCE = '0', OE = '0'



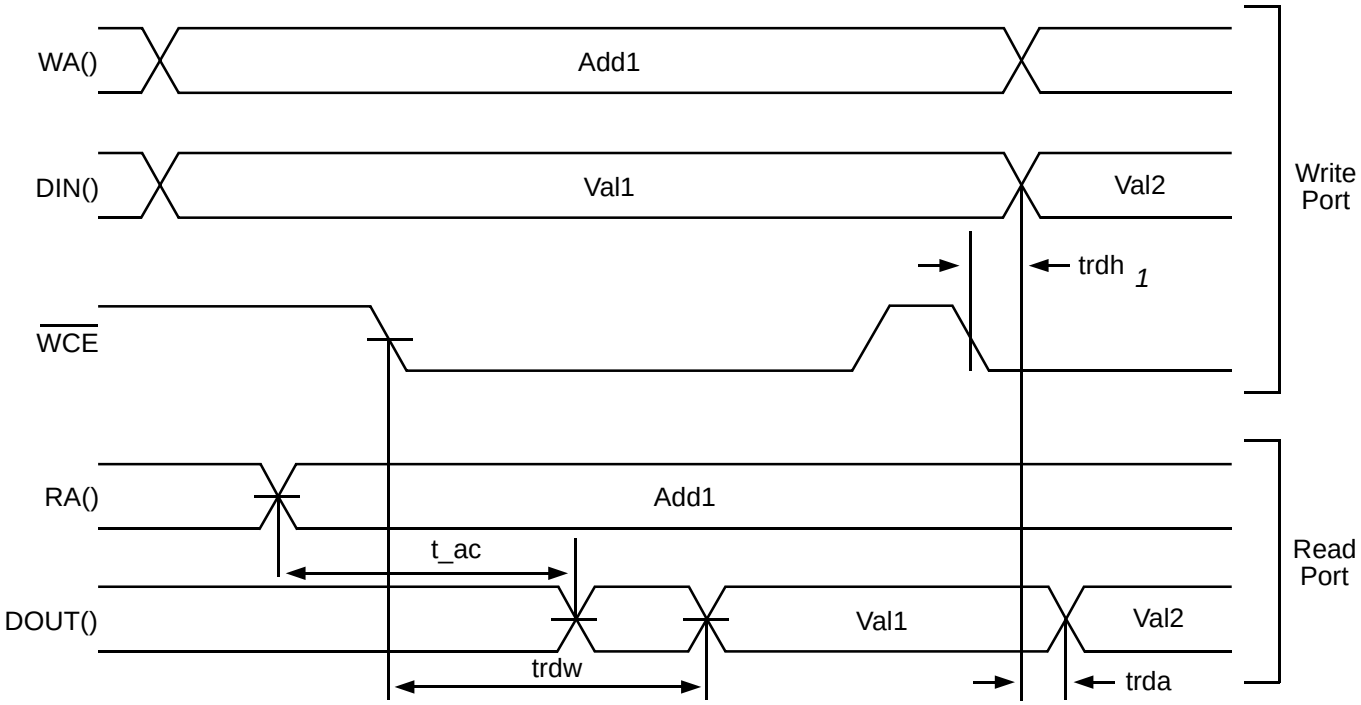
Notes:
- tpas : Address setup time to $\overline{WCE}$
- tpah : Address hold time to $\overline{WCE}$
- tpds : Data setup time to $\overline{WCE}$
- tpdh : Data hold time to $\overline{WCE}$
- trdw : Data access for a write-through operation

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to $\overline{WCE}$ is smaller than min. tpah.*
***22**. Error: Illegal data input: DIN hold time to $\overline{WCE}$ is smaller than min. tpdh.*
***23**. Error: Illegal data input: DIN setup time to $\overline{WCE}$ is smaller than min. tpds.*
***25**. Error: Illegal address input: setup time to $\overline{WCE}$ is smaller than min. tpas.*

Dual Port RAM 1R1W Write Through

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



Notes: t_ac : Address access time
trdw : Data access for a write-through operation from $\overline{WE}$ to data out. This time is always longer than t_wa or t_ac
trdh : Data hold from $\overline{WE}$ rising/falling for write-through
trda : Output delay from DIN

1. If DIN change from $\overline{WE}$ falling edge is greater than trdh, the DIN change will not propagate through to DOUT until the rising edge of $\overline{WE}$.

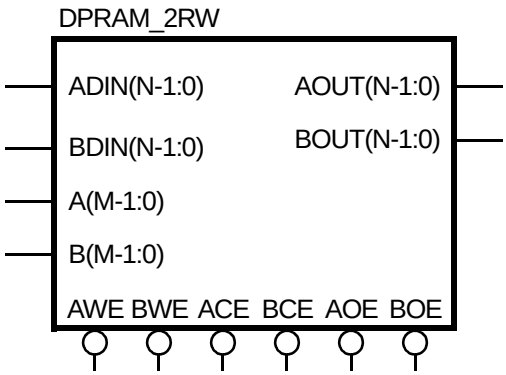
DPRAM_1R1W
High Speed Low-Power Dual Port RAM

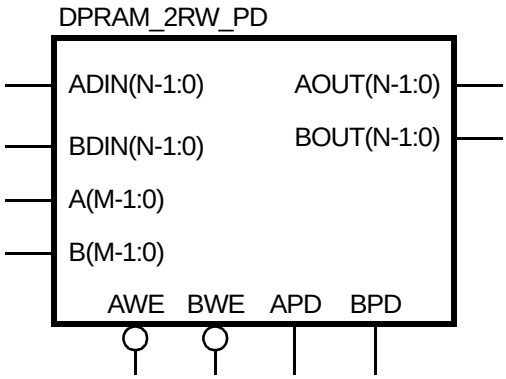
CMOS ASIC Standard Cell Memories

Features

- 8-T memory cell design
- Simple combinational logic decoding
- Small bitline differential in read mode eliminates precharge delay
- Fast ATD circuit turns on wordlines and sense amps only as needed to save power while allowing asynchronous operation

Logic Symbol





DPRAM_2RW: High Speed Low-Power Dual Port Description

AMI Semiconductor's high speed, low power CMOS RAM is available in both single and dual port versions. Column select passgates provide a cascode gain stage, followed by a differential voltage sense amp. The memory array columns may be multiplexed to optimize the aspect ratio. Multiplexing of columns, or column folding, shortens the bitline length (reduces the number of rows in the array) while increasing the width of the memory array. No change in the total memory bit count occurs.

The zero_out option sends the outputs all to "zero". This operation is controlled by the PD signal.

The RAM draws current only in response to changing inputs, minimizing power consumption and allowing complete IDDQ testing. Address changes activate the sense amps and one row of memory cells for a period of time longer than access time. The current drawn by each sense amp is comparable to the read current of each memory cell.

DPRAM_2RW
High Speed Low-Power Dual Port RAM

CMOS ASIC Standard Cell Memories

Signal Summary

INPUTS		OUTPUTS	
PORT LABEL	**FUNCTION**	**PORT LABEL**	**FUNCTION**
A, B	Addresses	ADOUT, BDOUT	Output Data
ADIN, BDIN	Input Data		
ACE, BCE	Chip Enable, active low		
AWE, BWE	Write Enable, active low		
AOE, BOE	Output Enable, active low, tristated output control		
APD, BPD	Power Down, active high, read and write cycles disabled and output driven to zero (0) when active		

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
N	bits per word	Integer	1 - 144
WORDS	number of words	Integer	8 - 16384
M	address size	Integer	3-14
BPC	bits per column	Integer	2, 4, 8, 16, 32
FLOORPLAN	auto floorplan	Integer	0, 1
BUFFER_SIZE	buffer size	String	1-6
FREQUENCY	frequency in MHz	Integer	1-100
VDROP	voltage drop in millivolts	Integer	1-249

Core Size

MEASUREMENT	DATA TYPE	VALUE
Block Height	Integer	4 to 512
Block Width	Integer	4 to 288
Maximum Total Bits	Integer	144K (16K by 9)

Bits Per Column (BPC) Options

BPC VALUE	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT	MINIMUM BITS	MAXIMUM BITS
2	8	1024	4	1	144
4	16	2048	8	1	72
8	32	4096	16	1	36
16	64	8192	32	1	18
32	128	16384	64	1	9

Parts

PART NAME	PINS
dpram_2rw	A, ACE, ADIN, AOE, AWE, B, BCE, BDIN, BOE, BWE, ADOUT, BDOUT
dpram_2rw_pd	A, ADIN, APD, AWE, B, BDIN, BPD, BWE, ADOUT, BDOUT

Truth Tables

zero-out option false

INPUTS					OUTPUTS	COMMENT
A, B	ACE, BCE	AOE, BOE	ADIN, BDIN	AWE, BWE	ADOUT, BDOUT	
0/1	0	0	X	1	Data	Read
X	0	1	X	1	Z	Output Disabled (standard) - RAM Active
X	1	1	X	X	Z	Output Disabled (standard) - RAM Disabled
X	1	0	X	X	Data	Outputs Stable, RAM disabled
0/1	0	0	0/1	0	Data	Write with Write-Through
0/1	0	1	0/1	0	Z	Write

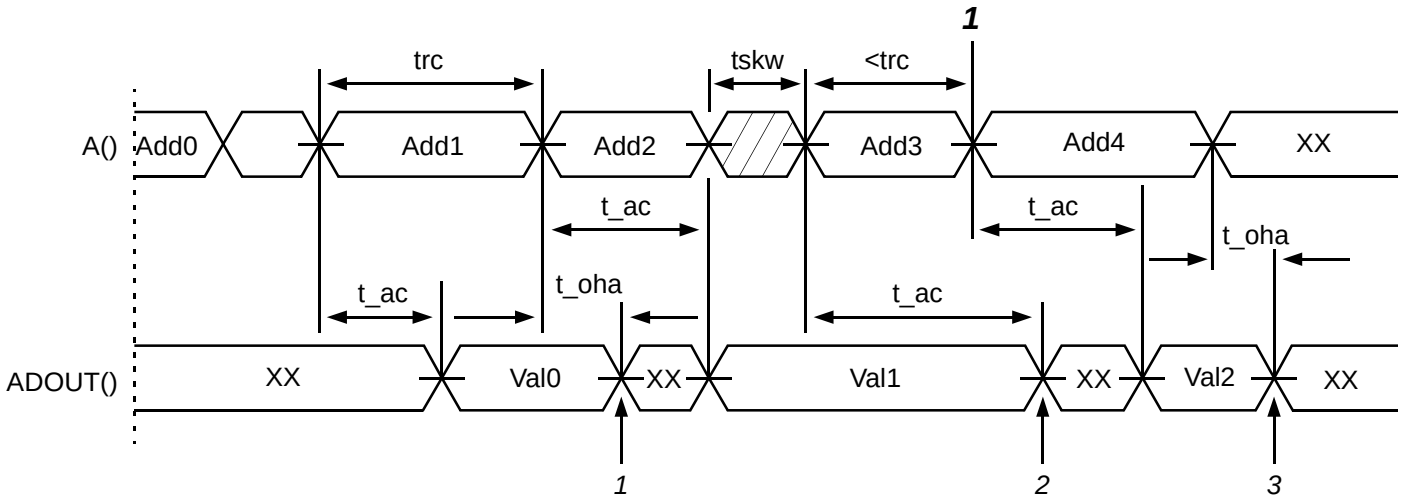
zero-out option true

INPUTS				OUTPUTS	COMMENT
A, B	APD, BPD	ADIN, BDIN	AWE, BWE	ADOUT, BDOUT	
X	1	X	X	0	Output Disabled (zero_out), RAM disabled
0/1	0	X	1	Data	Read
0/1	0	0/1	0	Data	Write with Write-Through

SWITCHING TIME WAVEFORMS

Dual Port RAM 2RW Read Cycle 1

dpram_2rw :AWE = '1', BWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd :AWE = '1', BWE = '1', APD = '0', BPD = '0'

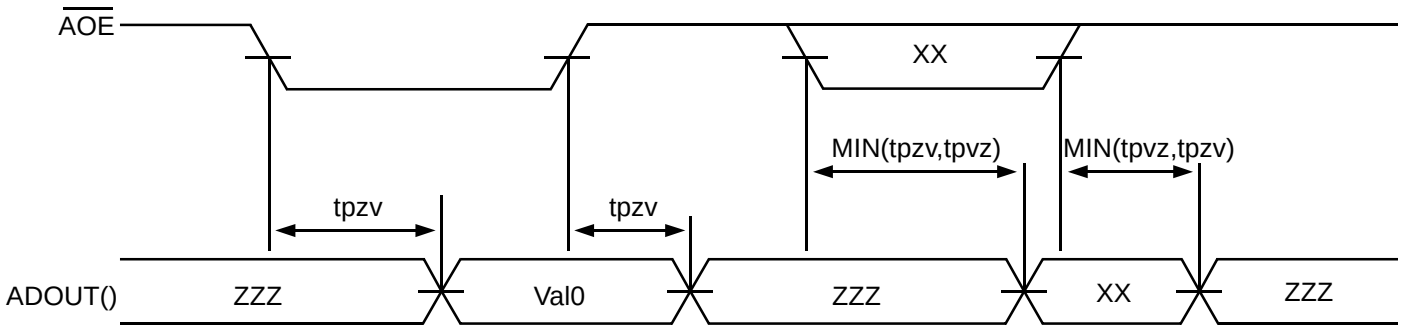


Notes: t_ac : Address Access Time (maximum of Rise/Fall)
trc : Read Cycle Time
t_oha : Output Hold Time from Address Change (minimum of Rise/Fall)
tskw : All addresses must complete transition within this time

1. t_oha delay will only be applied to the last data accessed, otherwise, t_ac will be used for the pin-to-pin delay.
2. trc = t_ac. If Add3 width is less than trc, DOUT() goes to 'X'.
3. If A() becomes 'X', DOUT() goes 'X' after time t_oha.
***1**. Error: Illegal Address input: Address cycle time is smaller than minimum trc.*

Dual Port RAM 2RW Read Cycle 2

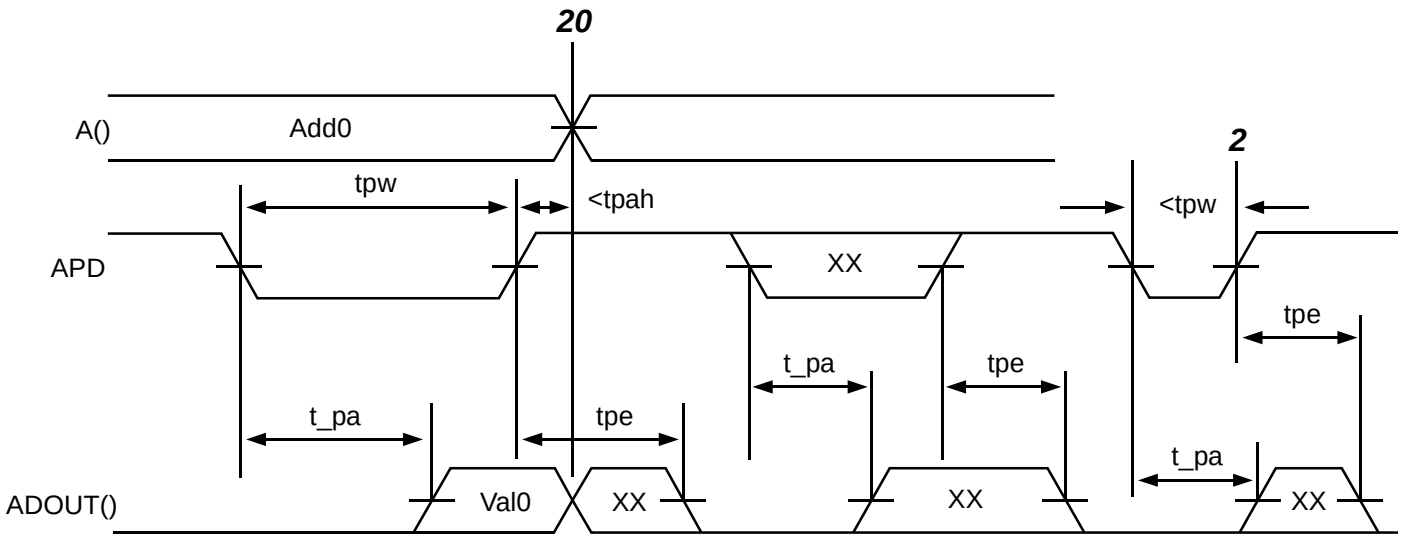
dpram_2rw: AWE = '1', BWE = '1', ACE = '0', BCE = '0'



Notes: tpvz : Delay to propagate valid DOUT() to high impedance.
tpzv : Delay to propagate high impedance to valid DOUT().

Dual Port RAM 2RW Read Cycle 3

dpram_2rw_pd: AWE = '1', BWE = '1'

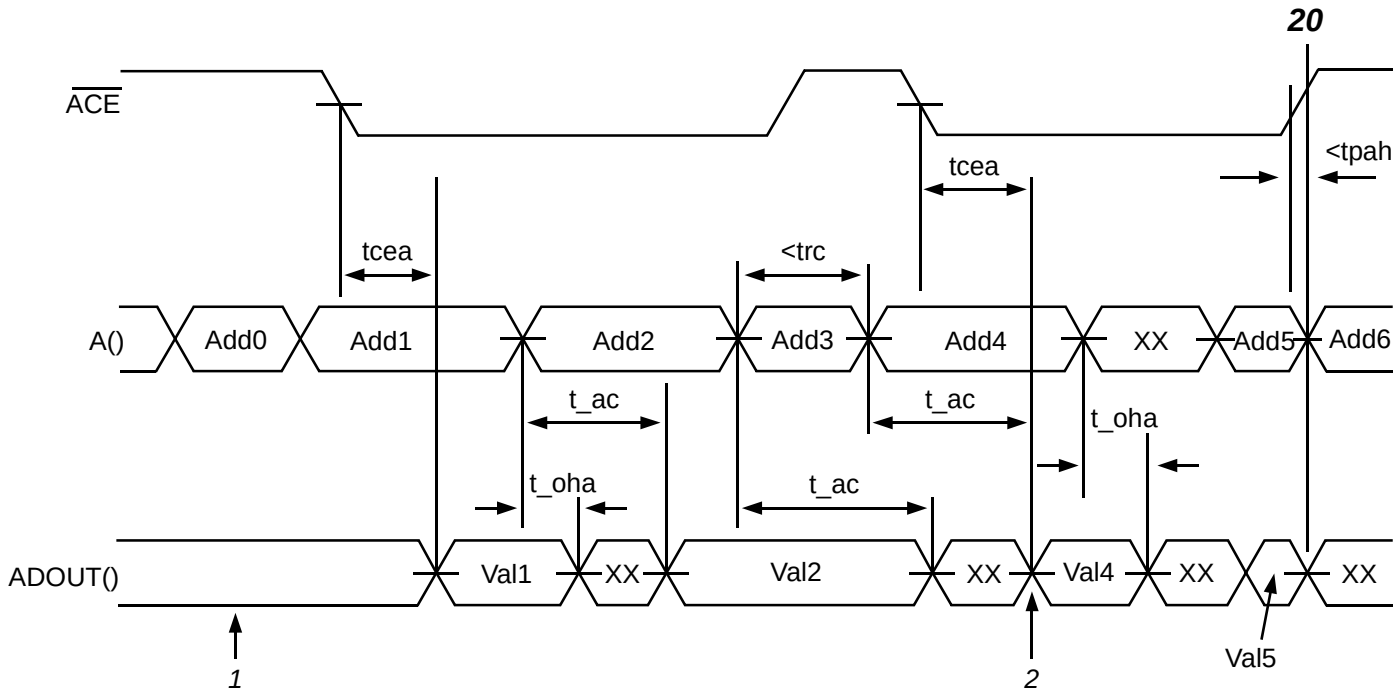


Notes: t_pa : Access time from PD
tpe : PD shutting off to DOUT() Fall
tpw : Minimum pulse width for PD
tpah : Address hold time from APD rising

***2**. Error: Illegal ADP input: ADP "Low" width time smaller than min. tpw.*
***20**. Error: Illegal address input: hold time to ADP is smaller than min. tpah.*

Dual Port RAM 2RW Read Cycle 4

dpram_2rw: AWE = '1', BWE = '1', AOE = '0', BOE = '0'



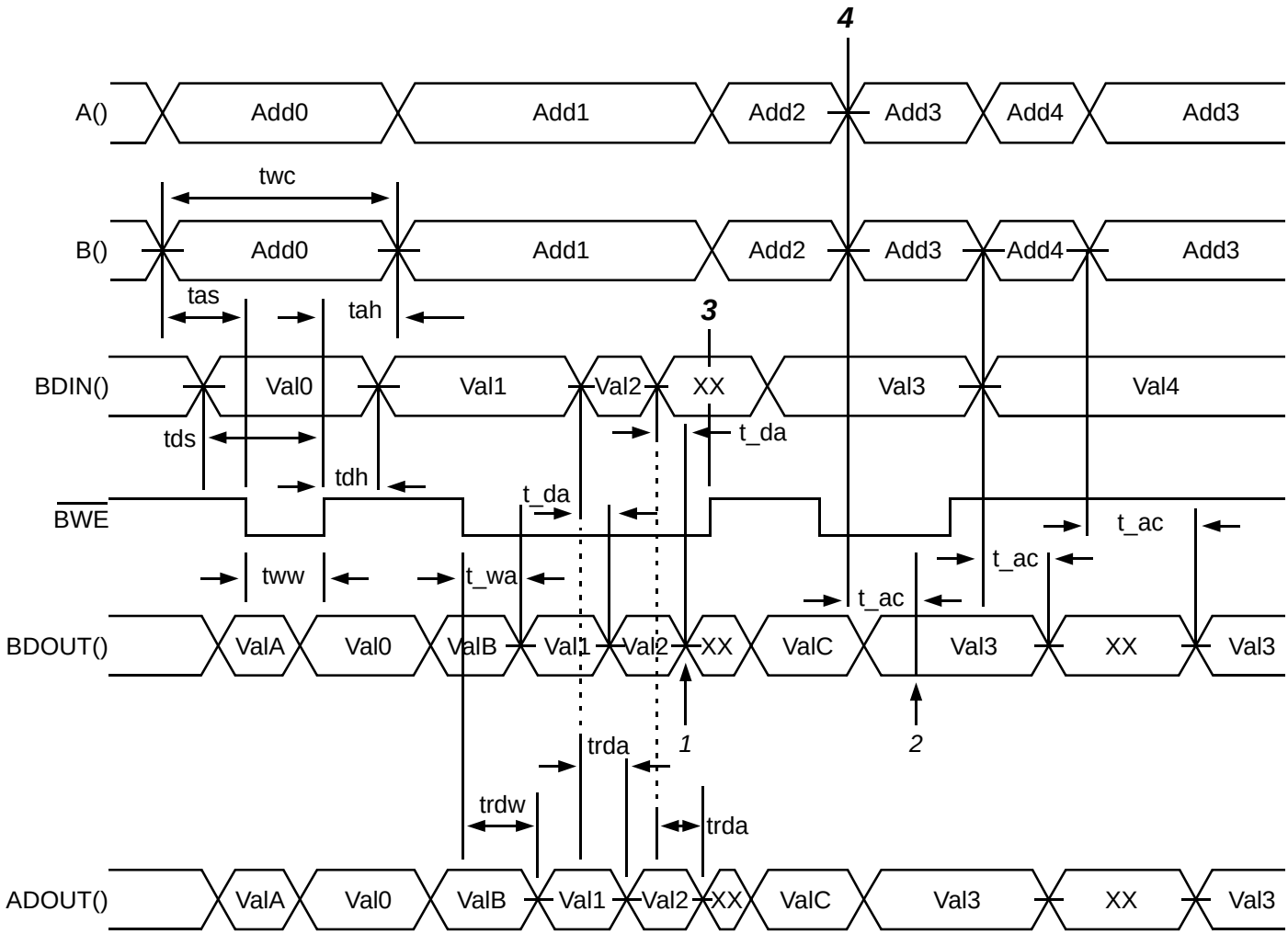
Notes:
- t_ac : Address access time
- tcea : $\overline{ACE}$ Access Time (maximum Rise/Fall)
- tpah : Address hold time from $\overline{ACE}$ rising
- trc : Read Cycle Time
- t_oha : Output hold time from address change (minimum of Rise/Fall)

1. Normal DOUT() change due to address change is locked out by '$\overline{ACE}$' pin set to '1'.
2. Output becomes valid after the MAX of t_ac or tcea.
Note that the '$\overline{ACE}$' pin rising does not trigger a RAM access.

***20**. Error: Illegal address input: hold time to $\overline{ACE}$ is smaller than min. tpah.*

Dual Port RAM 2RW Write Cycle 1

dpram_2rw : AWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: AWE = '1', APD = '0', BPD = '0'



Notes:
- t_da : Output delay time from Data (t_da<t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from BWE (MAX of Rise/Fall)
- t_ac : Address Access Time (maximum of Rise/Fall)
- trdw : Data access for write-through operation from BWE to ADOUT. This time is always longer than t_wa or t_ac
- trda : Output delay from BDIN
- tas : Access setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tww : Write pulse width low

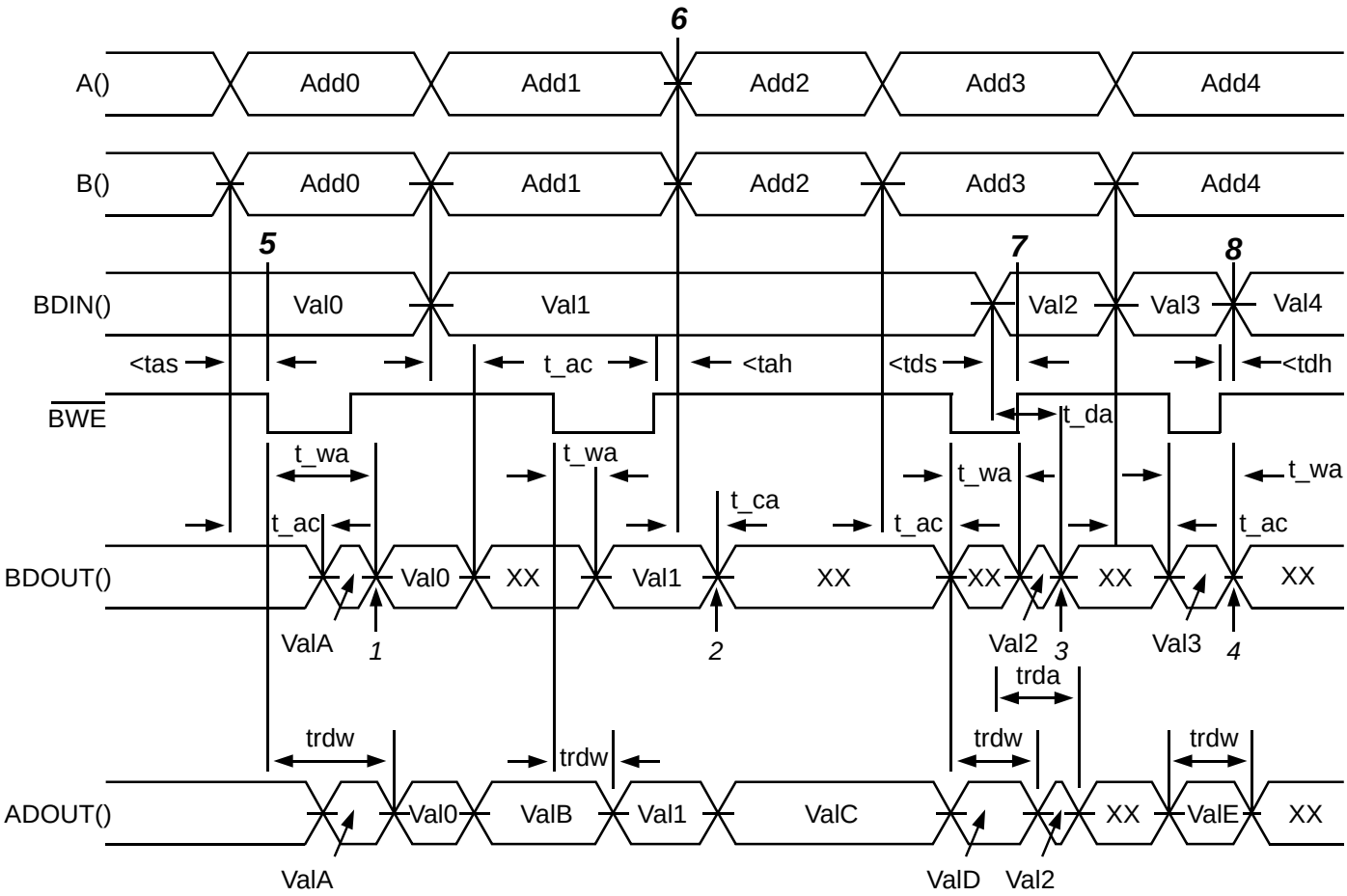
ValA, ValB, and ValC are previously retained in address Add0, Add1, and Add2.

1. Data retained in Add1 is overwritten by 'X' at this time.
2. Data retained in all words is overwritten by 'X' at this time. Writing Val3 into Add3 should be successful.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of BWE.*
***4**. Error: Illegal Operation: Address was changed while BWE low.*

Dual Port RAM 2RW Write Cycle 2

dpram_2rw : AWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: AWE = '1', APD = '0', BPD = '0'



Notes:
- t_da : Output delay time from Data (t_da<t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from BWE (MAX of Rise/Fall)
- t_ac : Address Access Time (maximum of Rise/Fall)
- trdw : Data access for write-through operation from BWE to ADOUT. This time is always longer than t_wa or t_ac
- trda : Output delay from BDIN to ADOUT
- tas : Access setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time

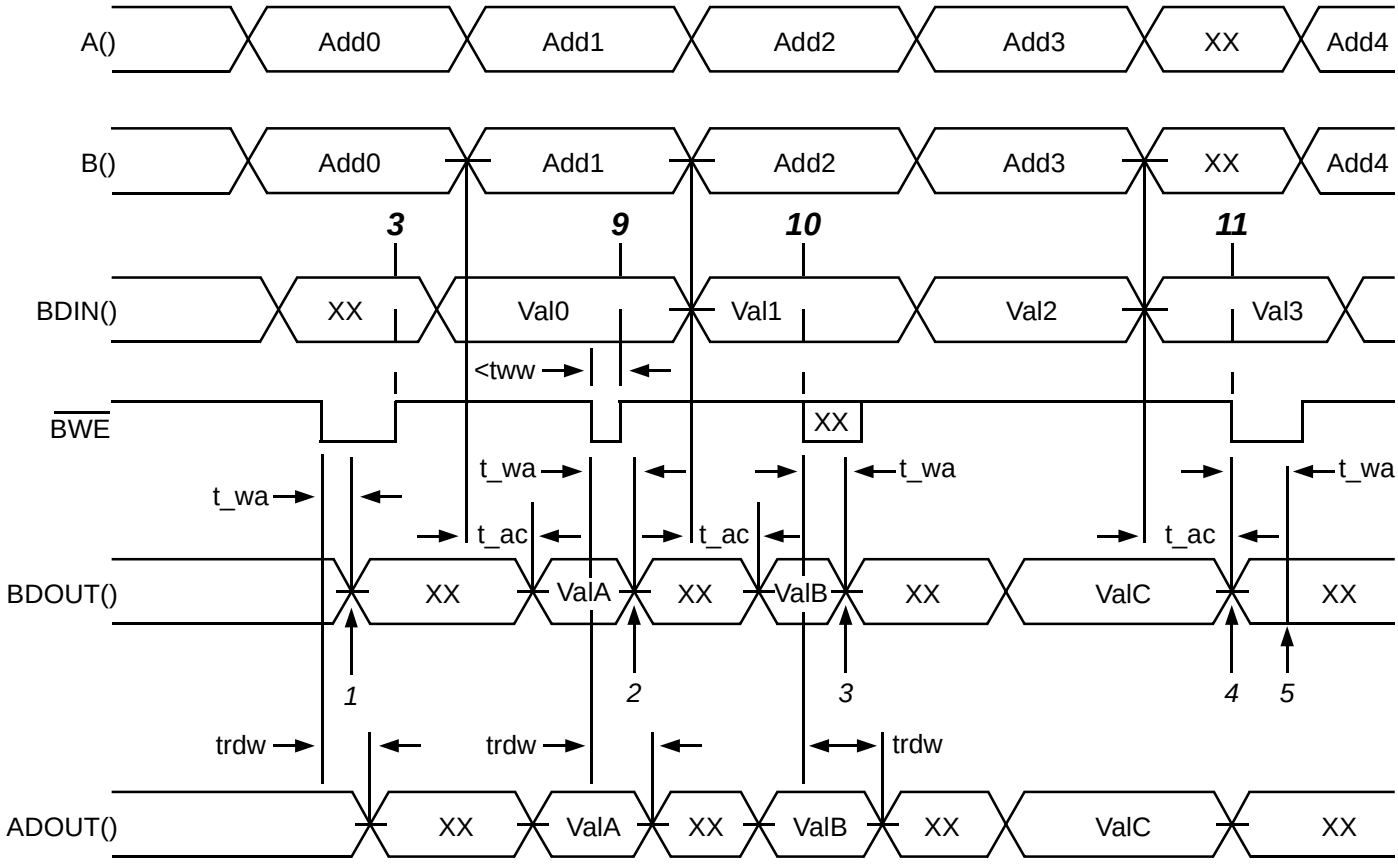
ValA - ValE are previously retained in Add0 - Add4.

1. Data retained in all words is overwritten by 'X' at this time. Writing Val0 into Add0 should be successful.
2. Data retained by all words is overwritten by 'X' at this time.
3. Data retained in Add3 is overwritten by 'X' at this time.
4. Data retained in Add4 is overwritten by 'X' at this time.

***5**. Error: Illegal Address Input: Address Setup time to $\overline{BWE}$ is smaller than Min tas.*
***6**. Error: Illegal Address Input: Address hold time to $\overline{BWE}$ is smaller than Min tah.*
***7**. Error: Illegal Data Input: DIN setup time to $\overline{BWE}$ is smaller than Min tds.*
***8**. Error: Illegal Data Input: DIN hold time to $\overline{BWE}$ is smaller than Min tdh.*

Dual Port RAM 2RW Write Cycle 3

dpram_2rw : AWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: AWE = '1', APD = '0', BPD = '0'



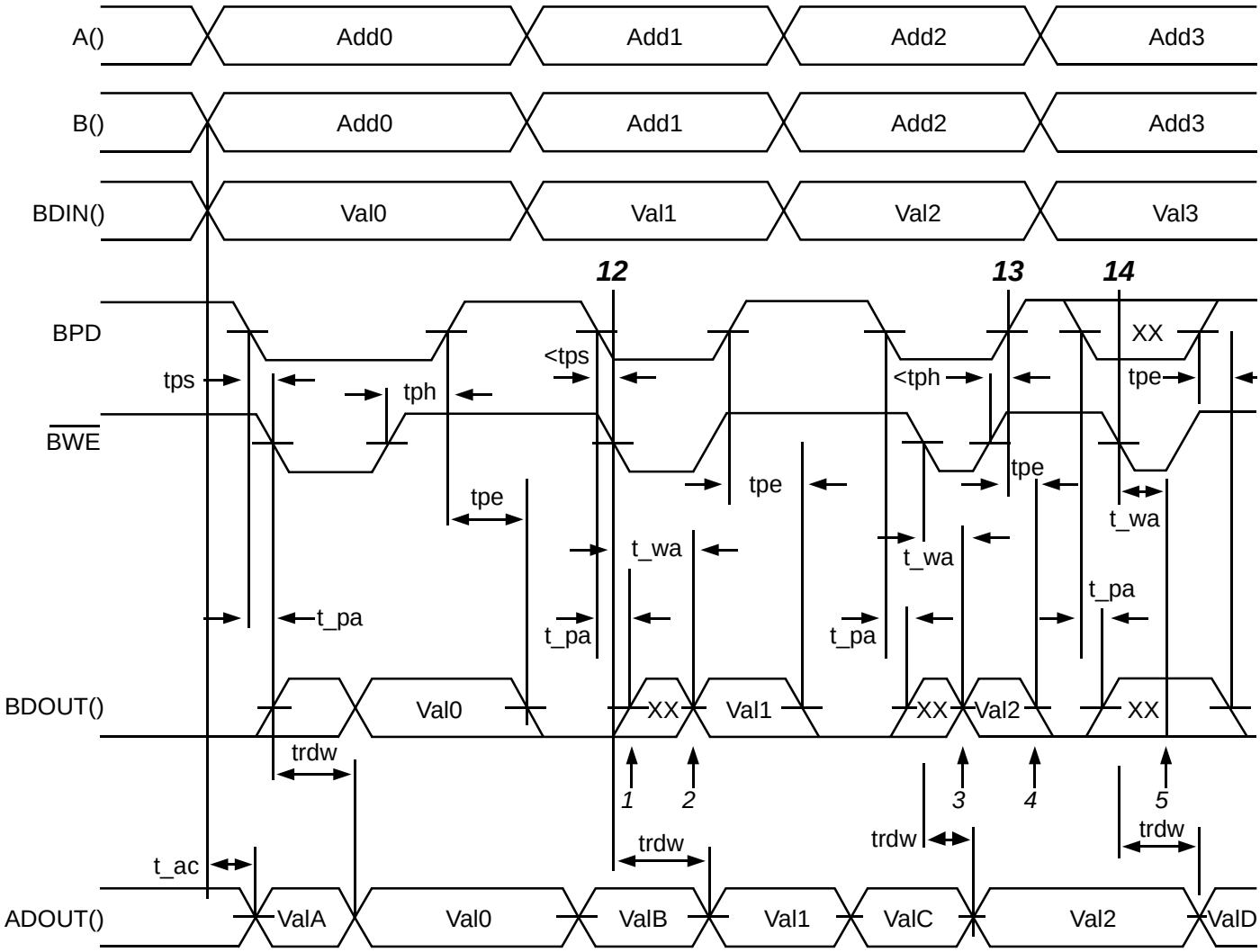
Notes: t_wa: Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
t_ac: Address Access Time (maximum of Rise/Fall)
trdw: Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_wa or t_ac
tww: Write pulse width low

1. Data retained in Add0 is overwritten by 'X' at this time.
2. Data retained in Add1 is overwritten by 'X' at this time.
3. Data retained in Add2 is overwritten by 'X' at this time.
4. BDOUT() becomes 'X' after t_ac time from leading edge of address 'X'.
5. Data retained in all words is overwritten by 'X' after t_wa time from falling edge of $\overline{BWE}$.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{BWE}$.*
***9**. Error: Illegal $\overline{BWE}$ Input: $\overline{BWE}$ "Low" width time is smaller than Min. tww.*
***10**. Error: Illegal Operation: $\overline{BWE}$ input went to "X".*
***11**. Error: Illegal Operation: Address was "X" at the falling edge of $\overline{BWE}$.*

Dual Port RAM 2RW Write Cycle 4

dpram_2rw_pd: AWE = '1', APD = '0'



Notes:
- t_ac : Address Access Time (maximum of Rise/Fall)
- tps : BCE/BPD setup time (BPD pin used for zero_out function)
- tph : BCE/BPD hold time (BPD pin used for zero_out function)
- t_wa : Output delay time from WE (MAX of Rise/Fall)
- trdw : Data access for write-through operation from BWE to ADOUT. This time is always longer than t_wa or t_ac
- t_pa : Access time from BPD
- tpe : BPD shutting off to BDOUT() Fall

ValA - ValD are previously retained in Add0 - Add3.

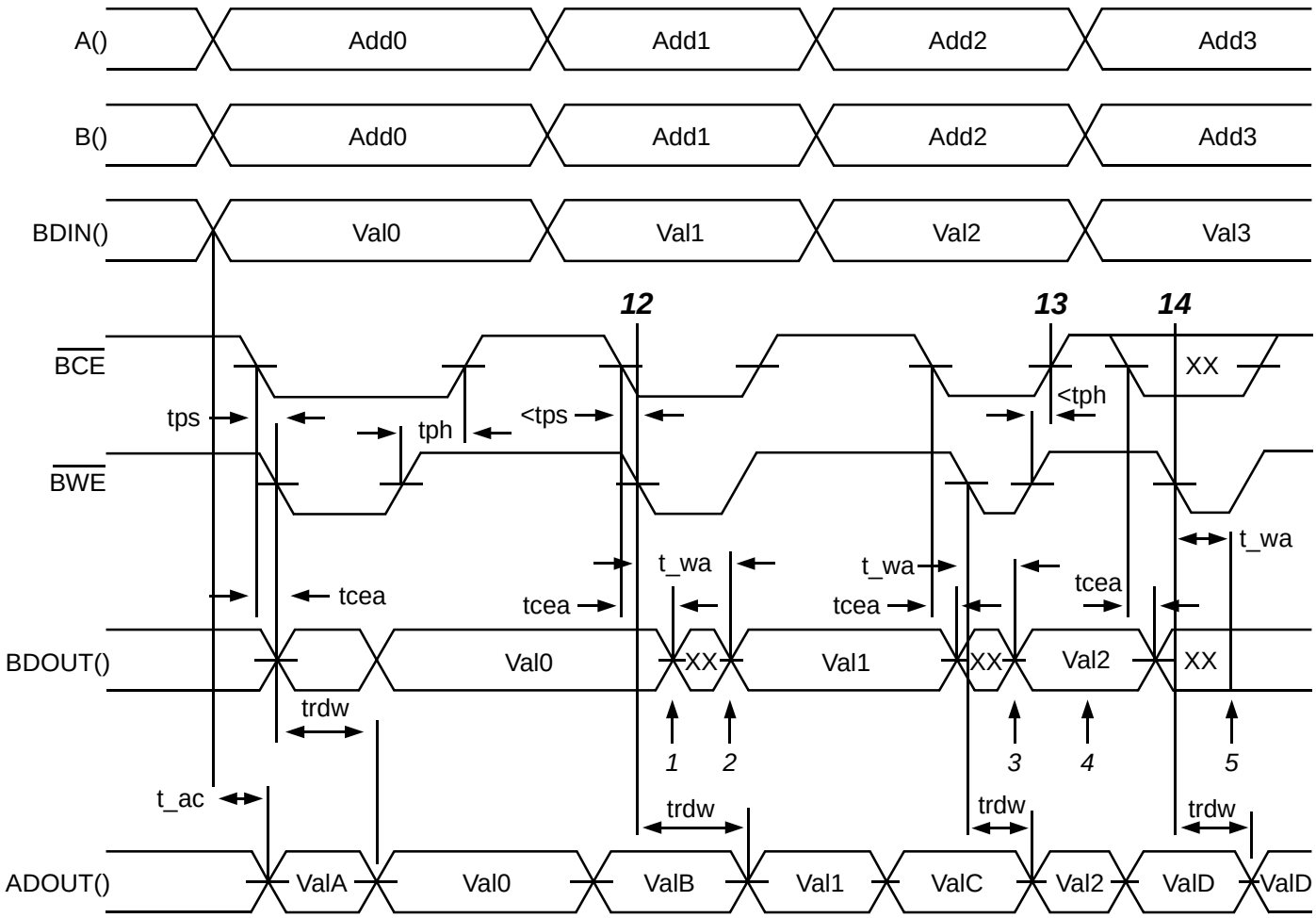
1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal BCE/BPD Input: BCE/BPD Setup time to BWE is smaller than Min. tps*

***13**. Error: Illegal $\overline{BCE}$/BPD Input: $\overline{BCE}$/BPD hold time to $\overline{BWE}$ is smaller than Min. tph.*
***14**. Error: Illegal Operation: BCE/BPD was "X" at the falling edge of $\overline{BWE}$.*

Dual Port RAM 2RW Write Cycle 5

dpram_2rw: AWE = '1', ACE = '0', AOE = '0', BOE = '0'



Notes: t_ac : Address access time (maximum of Rise/Fall)
tps : $\overline{BCE}$/BPD setup time
tph : $\overline{BCE}$/BPD hold time
t_wa : Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
trdw : Data access for a write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_wa or t_ac
tcea : Access time from $\overline{BCE}$

ValA - ValD are previously retained in Add0 - Add3.

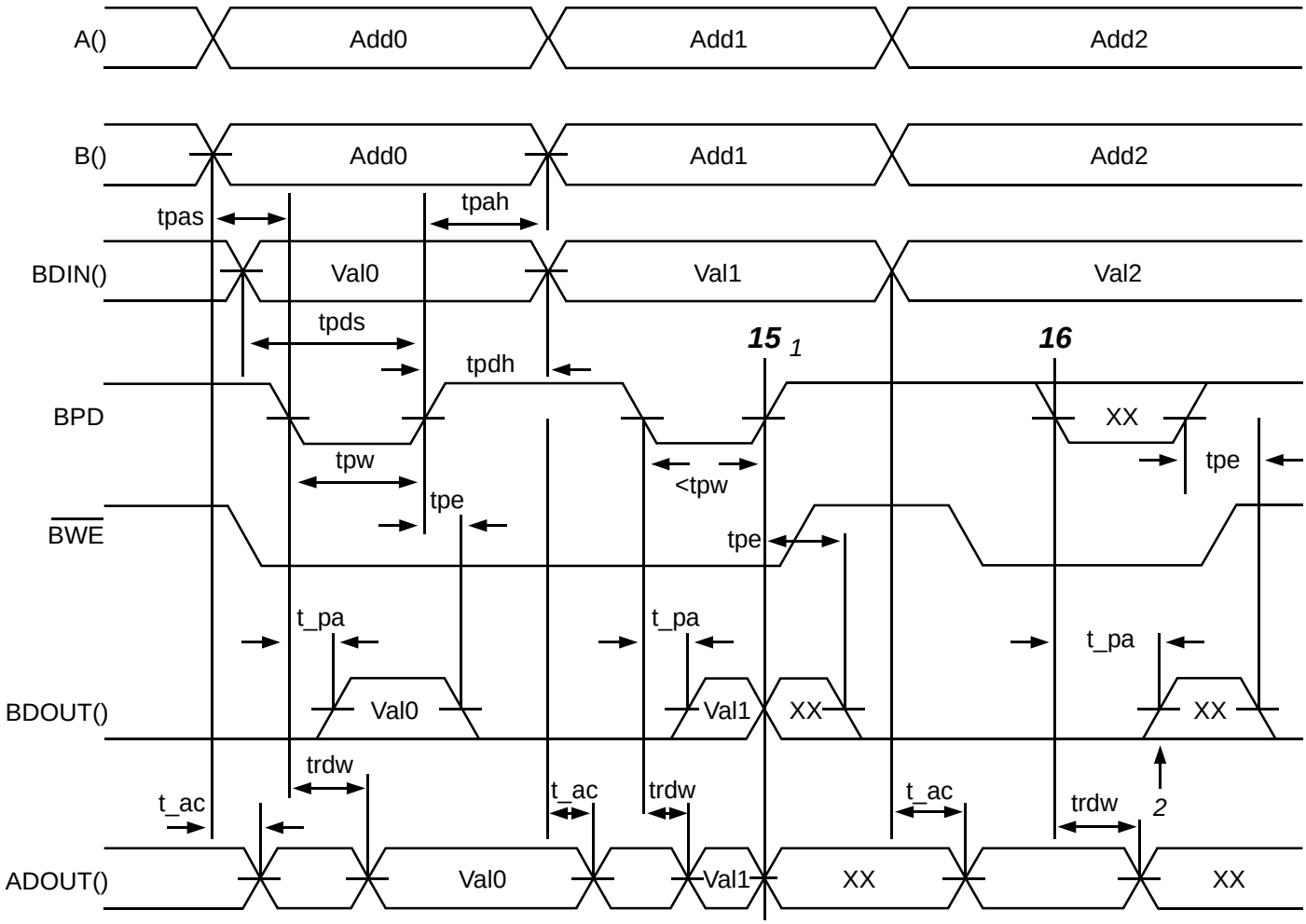
1., 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten By Val2 at this time.
5. If data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal $\overline{BCE}$/BPD Input: $\overline{BCE}$/BPD setup time to $\overline{BWE}$ is smaller than Min. tps.*

***13**. Error: Illegal $\overline{BCE}$/BPD Input: $\overline{BCE}$/BPD hold time to $\overline{BWE}$ is smaller than Min. tph.*
***14**. Error: Illegal Operation: BCE/BPD was "X" at the falling edge of $\overline{BWE}$.*

Dual Port RAM 2RW Write Cycle 6

dpram_2rw_pd: AWE = '1', APD = '0'



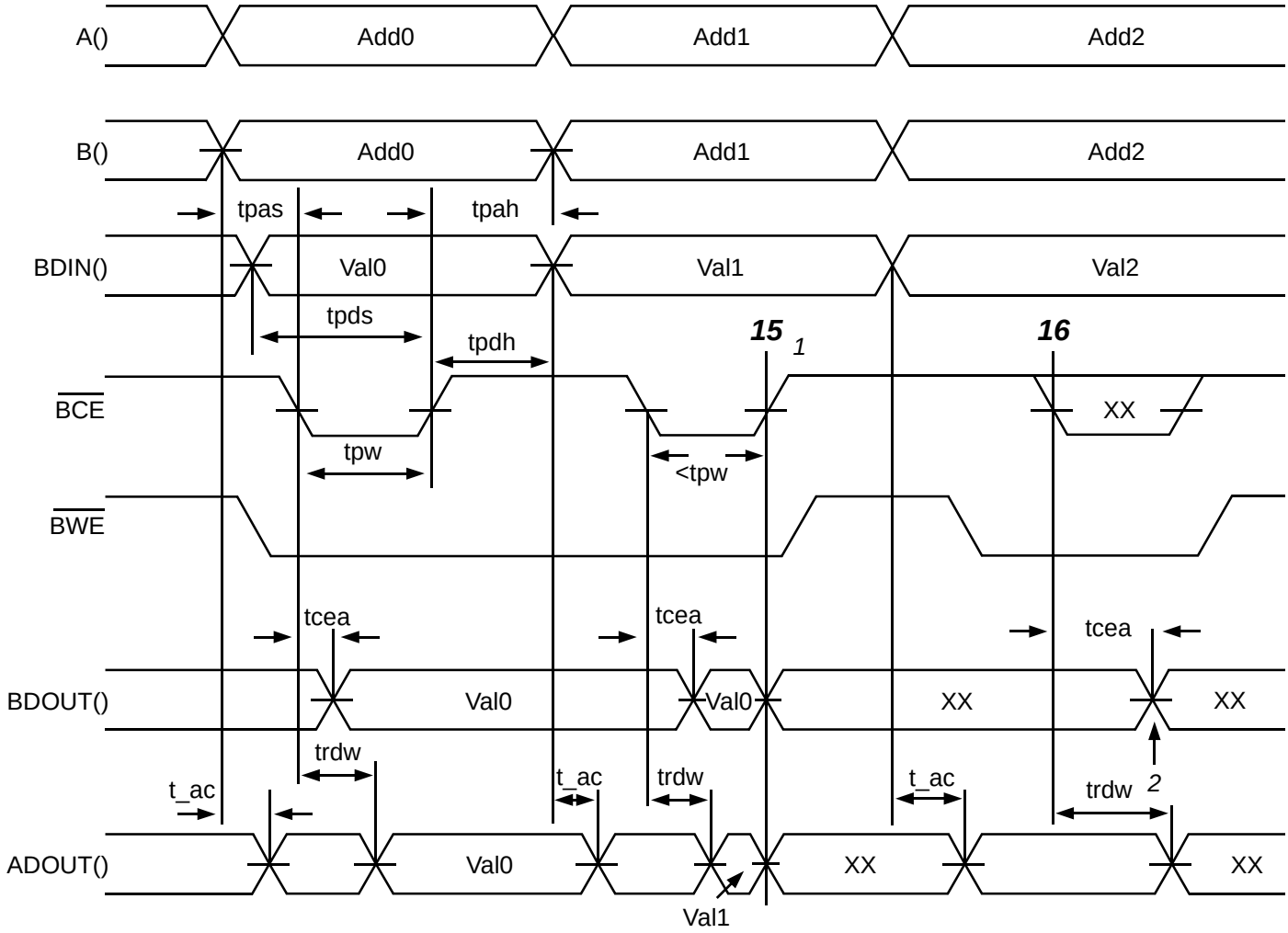
Notes:
- tpas : Address setup time to BPD (BPD pin used for zero_out function)
- tpah : Address hold time to BPD (BPD pin used for zero_out function)
- tpds : Data setup time to BPD
- tpdh : Data hold time to BPD
- t_ac : Address access time
- t_pa : Access time from BPD
- trdw : Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_ac
- tpw : Minimum pulse width for BPD
- tpe : PD shutting off to BDOUT() Fall

1. If data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal BPD Input: BPD "Low" width time smaller than Min. tpw.*
***16**. Error: Illegal Operation: BPD went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 2RW Write Cycle 7

dpram_2rw: AWE = '1', ACE = '0', AOE = '0', BOE = '0'



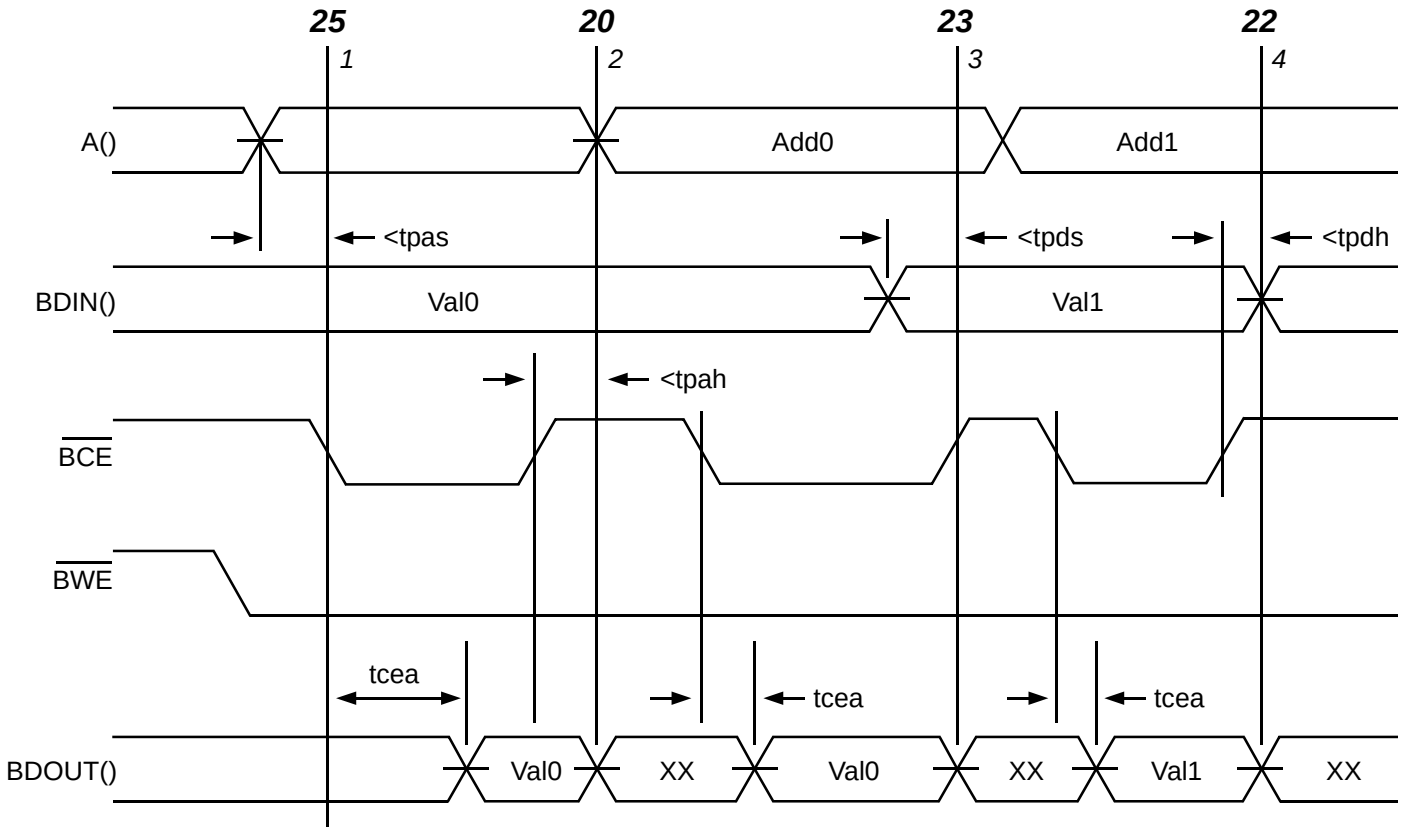
Notes:
- tpas : Address setup time to $\overline{BCE}$
- tpah : Address hold time to $\overline{BCE}$
- tpds : Data setup time to $\overline{BCE}$
- tpdh : Data hold time to $\overline{BCE}$
- t_ac : Address access time
- tcea : Address time from $\overline{BCE}$
- trdw : Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_ac
- tpw : Minimum pulse width for $\overline{BCE}$

1. If data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{BCE}$ Input: $\overline{BCE}$ "Low" width time smaller than Min. tpw.*
***16**. Error: Illegal Operation: $\overline{BCE}$ went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 2RW Write Cycle 8

dpram_2rw: ACE = '0', AOE = '0', BOE = '0', AWE = '1'



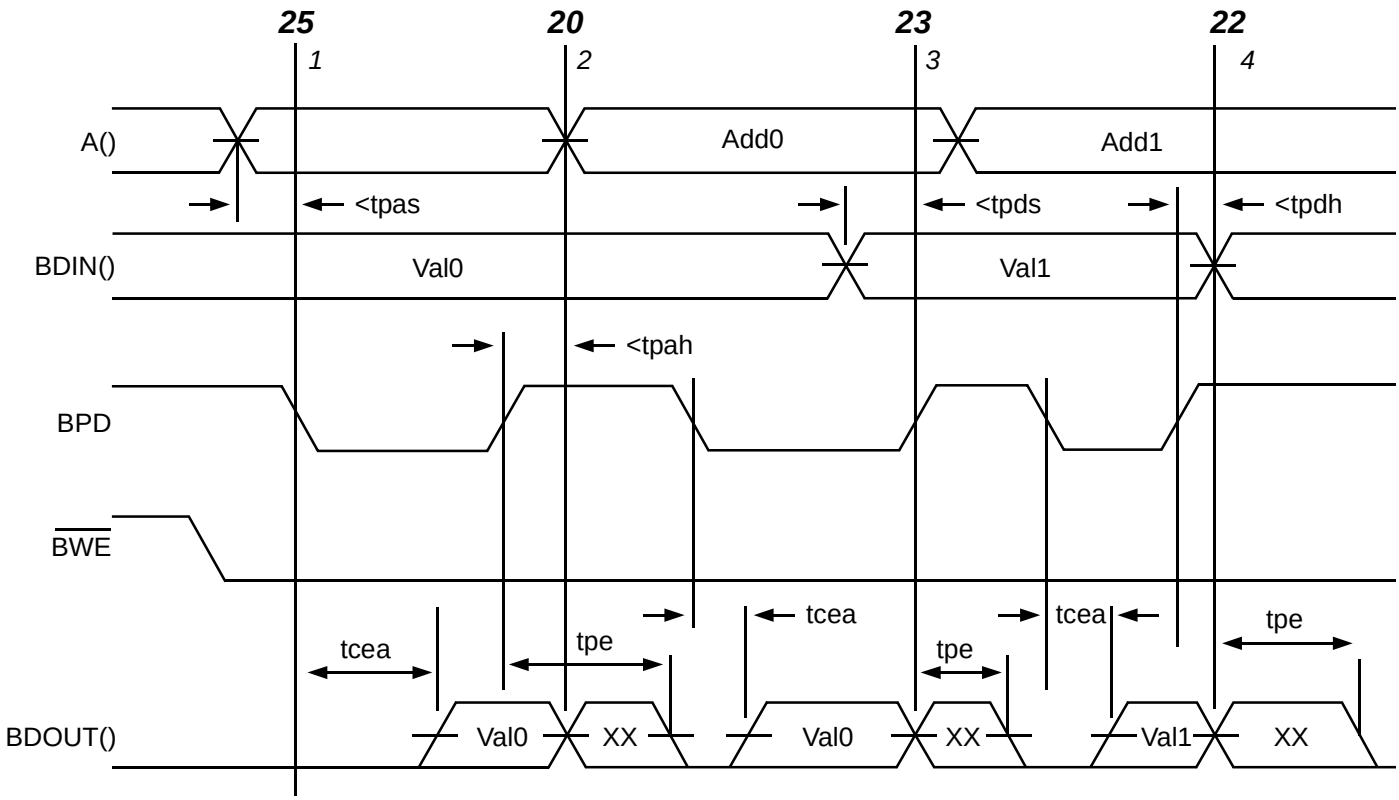
Notes: tpas : Address setup time to $\overline{BCE}$
tpah : Address hold time to $\overline{BCE}$
tpds : Data setup time to $\overline{BCE}$
tcea : BCE access time

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to $\overline{BCE}$ is smaller than Min. tpah.*
***22**. Error: Illegal data input: DIN hold time to $\overline{BCE}$ is smaller than Min. tpdh.*
***23**. Error: Illegal data input: DIN setup time to $\overline{BCE}$ is smaller than Min. tpds.*
***25**. Error: Illegal address input: setup time to BCE is smaller than MIn. tpas.*

Dual Port RAM 2RW Write Cycle 9

dpram_2rw_pd: APD = '0', AWE = '1'



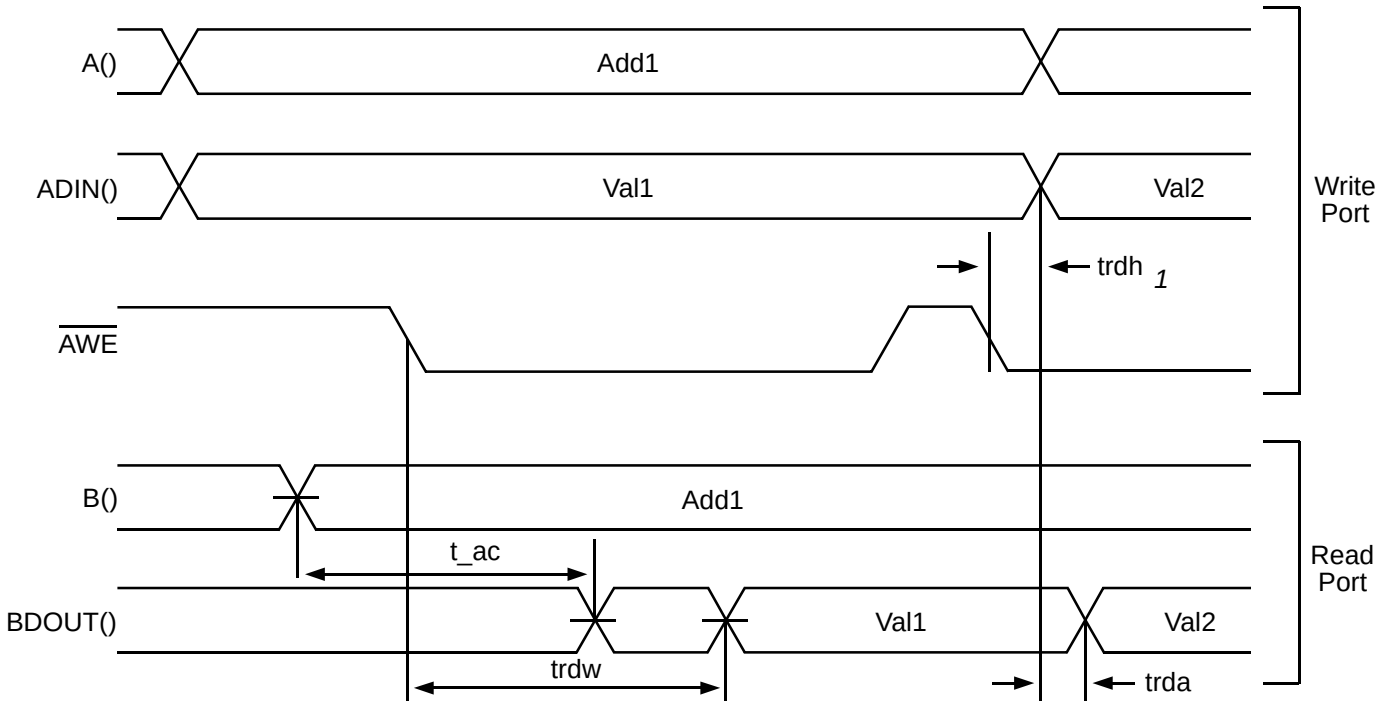
Notes:
- tpe : BPD shutting off to BDOUT() Fall
- tpas : Address setup time to BPD
- tpah : Address hold time to BPD
- tpds : Data setup time to BPD
- tcea : BPD access time

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to BPD is smaller than Min. tpah.*
***22**. Error: Illegal data input: BDIN hold time to BPD is smaller than Min. tpdh.*
***23**. Error: Illegal data input: BDIN setup time to BPD is smaller than Min. tpds.*
***25**. Error: Illegal address input: setup time to BPD is smaller than MIn. tpas.*

Dual Port RAM 2RW Write Through

dpram_2rw : BWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: BWE = '1', APD = '0', BPD = '0'



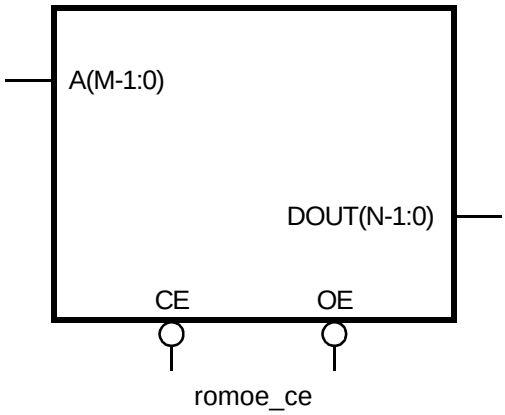
Notes: t_ac : Address access time
trdw : Data access for a write-through operation from $\overline{AWE}$ to data out. This time is always longer than t_ac
trdh : Data hold from $\overline{AWE}$ rising/falling for write-through
trda : Output delay from ADIN

1. If ADIN change from $\overline{AWE}$ falling edge is greater than trdh, the ADIN change will not propagate through to BDOUT until the rising edge of $\overline{AWE}$.

Features

- Maximum of 32K words; 2 MBits
- Word length selectable from 2 to 64 bits per word
- Setup and hold timing constraints on address lines eliminated using combinational address decoding
- Powerdown option minimizes power consumption

Logic Symbol



N = Number of bits per memory word
M = Number of address lines

CMOS ASIC Standard Cell Memories

ROM: High Speed ROM Description

AMI Semiconductor's high speed ROM is built to customer specified parameters including number of bits per word, number of address lines, number of words per module, number of bits per column, tristate output, and power down.

The powerdown option adds a chip enable input (CE), that allows the output to be disabled, minimizing power consumption. CE is independent of output enable (OE). While the ROM is disabled with CE, outputs either go to 1, or are tristated with the optional OE pin.

AMI Semiconductor's ROM has an output enable port when tristate output is selected. When output enable is held high, the output is tristated.

Bits Per Column Options

BITS PER COLUMN	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT
4	64	4096	32
8	64	8192	64
16	512	16384	128
32	512	32768	256

Signal Summary

PORT LABEL	FUNCTION
A(i)	Address input, bit i
OE	Output enable (tristate output buffer)
CE	Chip enable (powerdown)
DOUT(i)	Data output, bit i

CMOS ASIC Standard Cell Memories

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
N	Bits per word	Integer	2-64
WORDS	Number of words	Integer	64-32768
M	Number of address lines	Integer	6-15
CODEFILE	Name of codefile	String	<codefile_name>
BUFFER_SIZE	Buffer size	String	1-4
FREQUENCY	Frequency in MHz	Integer	1-100
VDROP	Voltage drop in millivolts	Integer	1-249

Parts

PART NAME	PINS	OPTIONS	
		TRISTATE	PWR_DOWN
rom	A, DOUT		
romce	A, CE, DOUT		X
romoe	A, OE, DOUT	X	
romoe_ce	A, CE, OE, DOUT	X	X

Truth Tables

With Tristate

A	OE	MODE	DOUT
Addr	0	Read	Data[a]
X	1	High impedance	z

With Powerdown

A	CE	MODE	DOUT
Addr	0	Read	Data[a]
X	1	Pwerdown	All 1’s

With Tristate and Powerdown

A	CE	OE	DOUT
X	1	1	z
X	1	0	1
X	0	1	z

SECTION 7
SALES INFORMATION

On-Line Sales Office information

AMIS maintains a strong global presense through design and sales operations in North America, Europe and the Asia Pacific region. Please visit our website at http://www.amis.com/sales for the most current sales contacts.