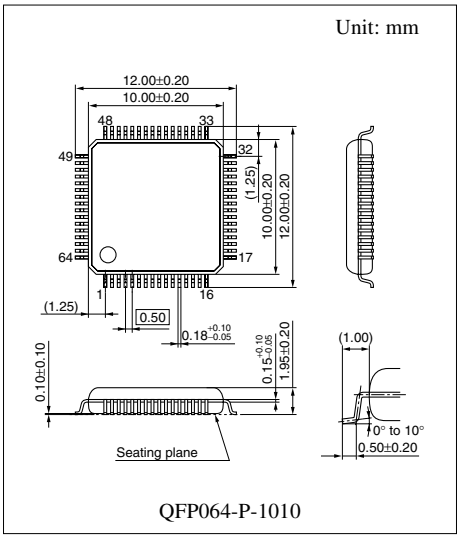
AN2526NFH

Automotive LCD TV signal processor IC

■ Overview

The AN2526NFH is a video signal processing IC built-in a 5-volt power-supply source driver for TFT color LCD (normally white type), and it supports NTSC and PAL systems. The main circuitry of this IC includes video-signal processing circuit, chrominance signal processing circuit, interface circuit, synchronizing circuit and many color quality adjusting circuits. This IC converts the composite video signal or separated Y/C signal or RGB signals into RGB signals available for TFT color LCD.



Note) The package of this product will be changed to lead-free type (QFP064-P-1010A). See the new package dimensions section later of this datasheet.

■ Features

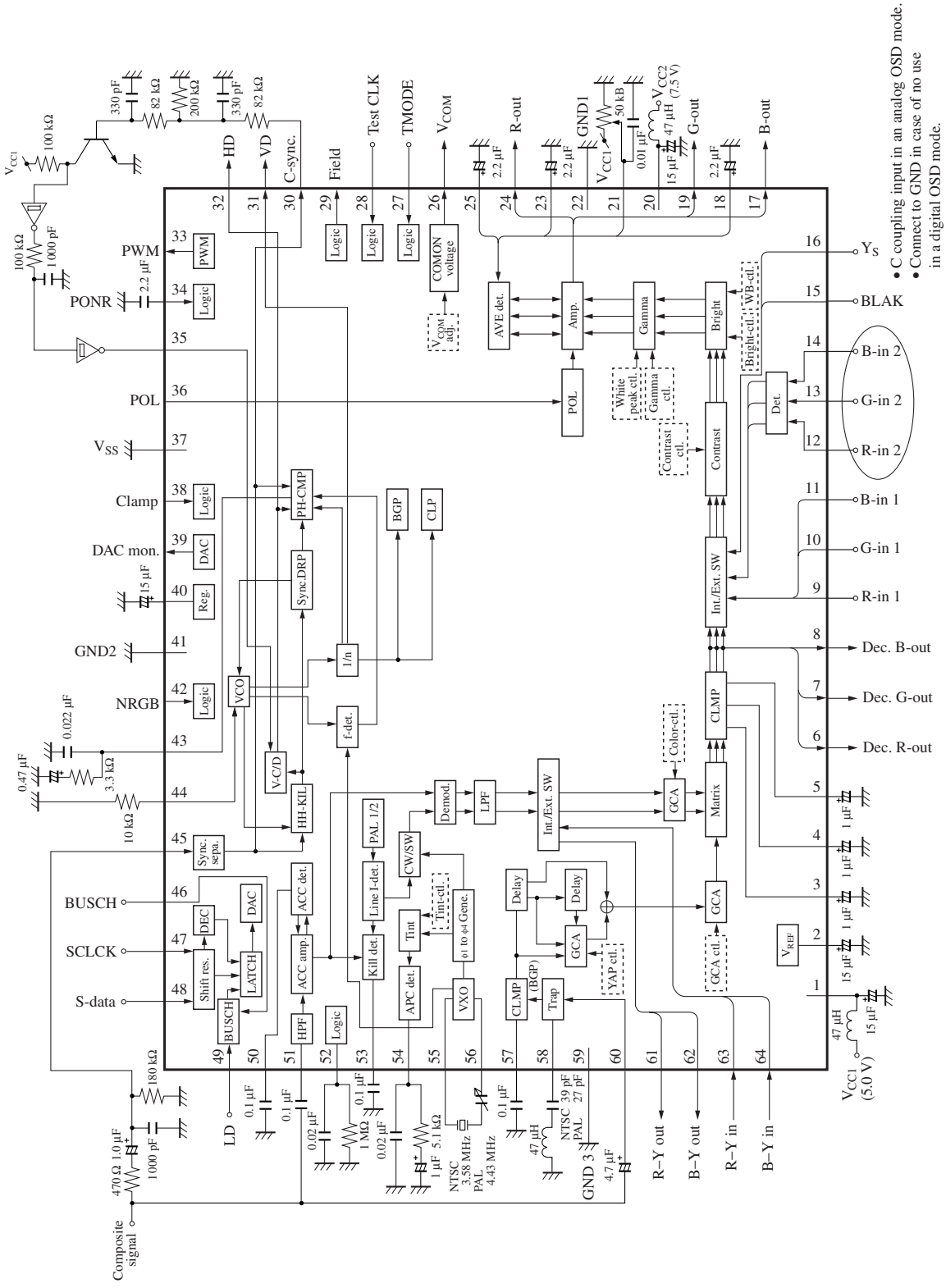
- Supply voltage: 5 V/7.5 V
- Built-in a 5-volt power-supply source driver for TFT type LCD
- Low consumption power (typ. 260 mW)
- Supporting NTSC and PAL
- Supporting composite, component and color difference signal input
- Video signal, analog RGB (2 systems)
  One is for OSD (analog/digital).
- Each mode setting is possible with 3-line or I^2C bus control.
- Electronic volume (D/A converter) built in
- Contrast/Brightness/γ correction circuit built in
- Horizontal and vertical display position adjustment are possible by serial control.
- Difference from the AN2526FH
  Compared to the AN2526FH, the sync. system gain is increased in no signal input. This may cause the picture on the screen to be swaying horizontally. So we cannot recommend this IC to be used in the set with no-signal input mode.

■ Applications

- 4 inches to 7 inches middle size TFT LCD equipment of normally white, of such as an in-car TV and an LCD monitor for car navigation system.

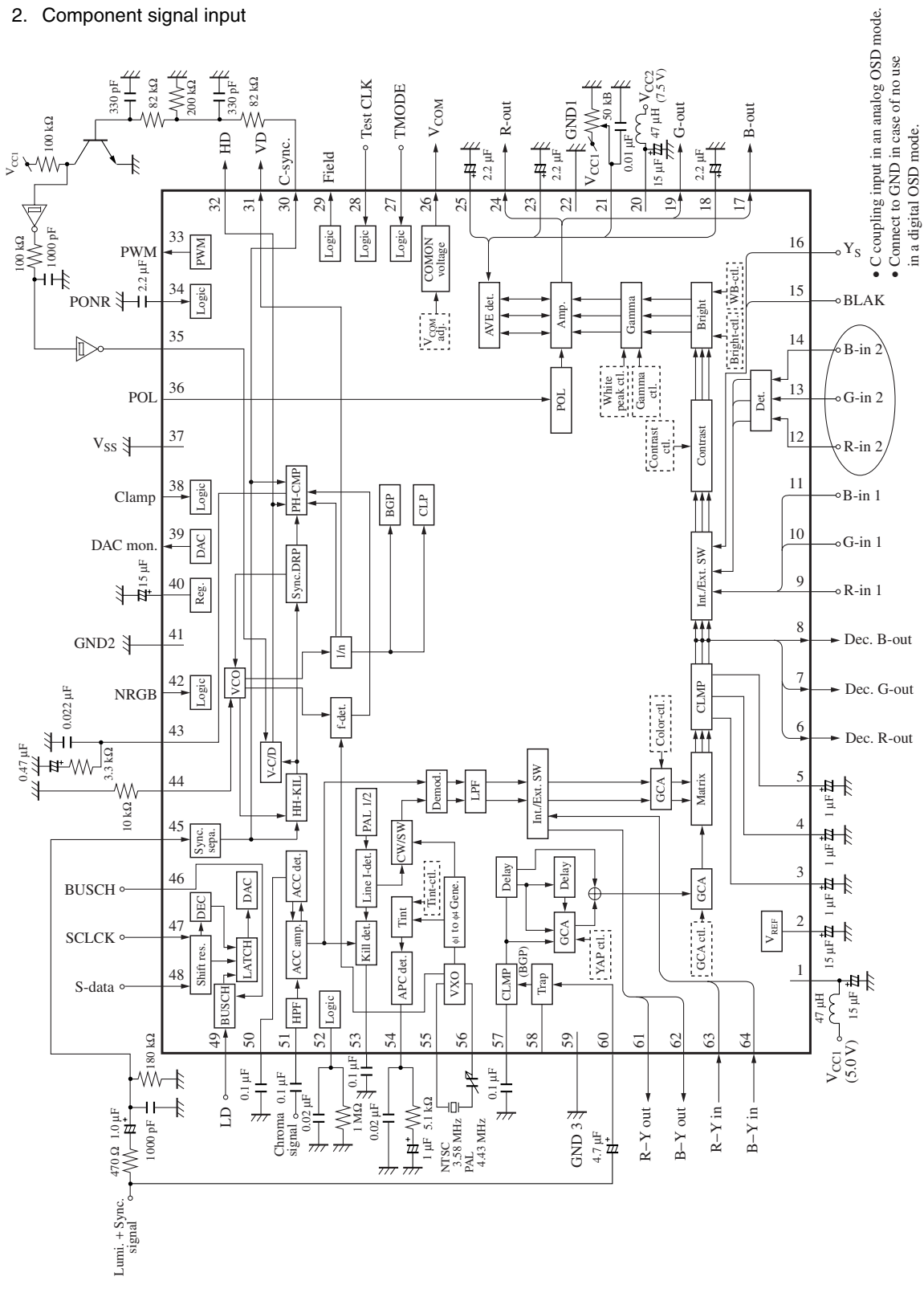
■ Application Circuit Examples

1. Composite signal input



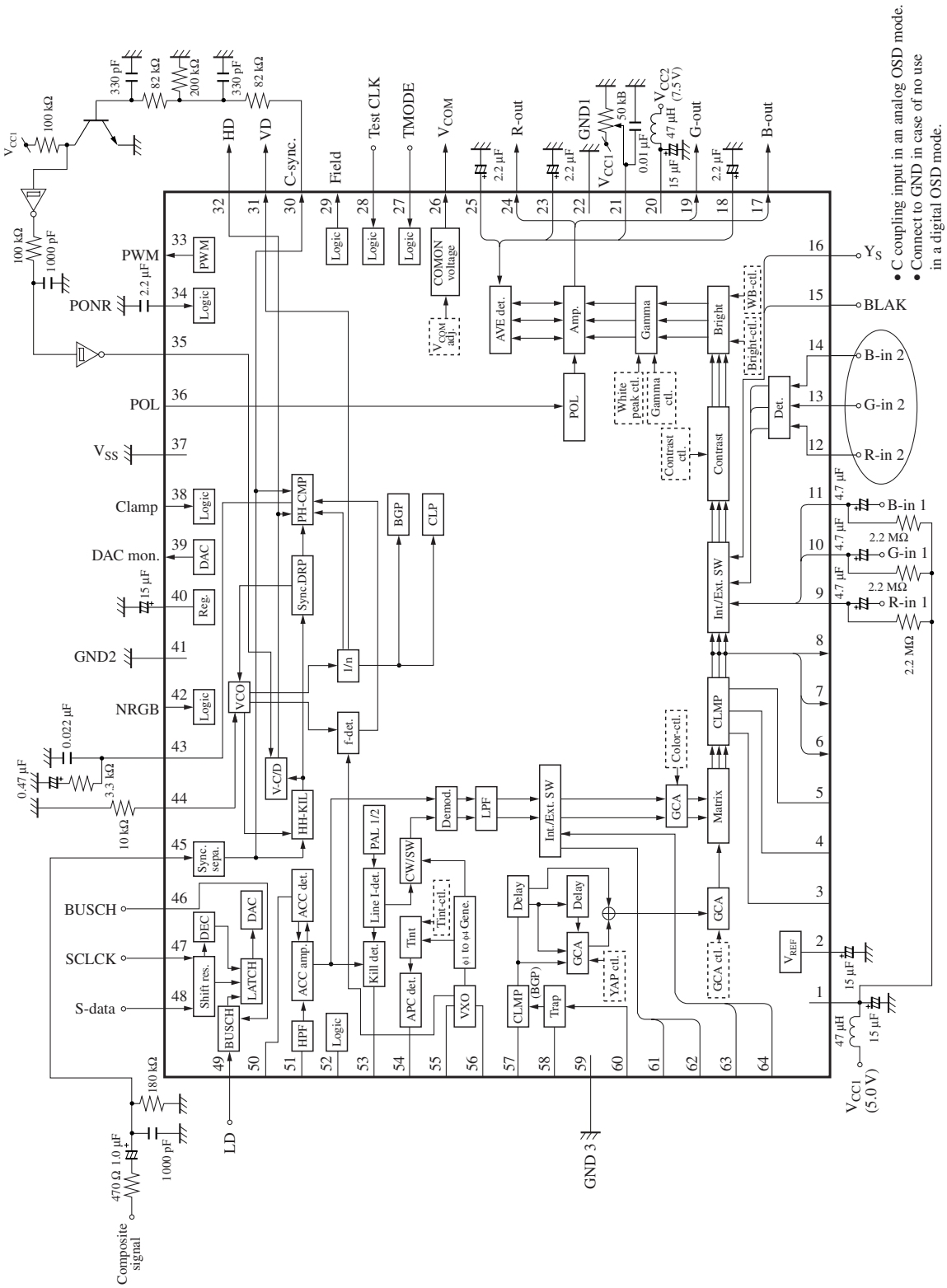
■ Application Circuit Examples (continued)

2. Component signal input



■ Application Circuit Examples (continued)

3. Analog RGB signal input



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	V_{CC1} (5.0 V)	33	PWM output pin
2	Reference voltage pin	34	Power-on reset detection pin
3	R-ch. clamp detection pin	35	Vertical synchronizing signal input pin
4	G-ch. clamp detection pin	36	1H reverse signal input pin
5	B-ch. clamp detection pin	37	Clock-system GND (V_{SS})
6	R-ch. decoder output pin	38	Clamp pulse input pin
7	G-ch. decoder output pin	39	DAC monitor pin
8	B-ch. decoder output pin	40	Clock-system power supply (3.0 V)
9	R-ch. analog signal input pin	41	GND 2
10	G-ch. analog signal input pin	42	Analog imposing control signal input pin
11	B-ch. analog signal input pin	43	AFC loop filter connecting pin
12	R-ch. analog/character signal input pin	44	VCO frequency adjustment pin
13	G-ch. analog/character signal input pin	45	Synchronizing signal input pin
14	B-ch. analog/character signal input pin	46	Serial/I^2C bus switching pin
15	Black level indication control signal input pin	47	Serial data shift clock input pin
16	Character picking up pulse input pin	48	Serial data input pin
17	B-ch. output pin	49	Serial data write pulse input pin
18	B-ch. output DC feedback detection pin	50	ACC detection pin
19	G-ch. output pin	51	ACC input pin
20	V_{CC2} (7.5 V)	52	Horizontal clock detection pin
21	Drive output reference potential input pin	53	Chrominance killer detection pin
22	GND 1	54	APC detection pin
23	G-ch. output DC feedback detection pin	55	VXO input pin
24	R-ch. output pin	56	VXO output pin
25	R-ch. output DC feedback detection pin	57	Y-system clamp detection pin
26	Common reverse signal output pin	58	Chrominance signal trap filter connection pin
27	Testing pulse input pin	59	GND 3
28	Testing clock input pin	60	Luminance signal input pin
29	Field identification signal output pin	61	R-Y output pin
30	Composite synchronizing signal output pin	62	B-Y output pin
31	Vertical synchronizing signal output pin	63	R-Y input pin
32	Horizontal synchronizing signal output pin	64	B-Y input pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1}	5.5	V
	V_{CC2}	8.5	
Supply current	I_{CC}	—	mA
Power dissipation *2	P_D	423	mW
Operating ambient temperature *1	T_{opr}	−30 to +85	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
∗2: The power dissipation shown is the value in free air for T_{opr} = 85°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	4.7 to 5.3	V
	V_{CC2}	7.0 to 8.0	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC						
V_{CC1}-system current consumption	I_{TOTAL1}	—	29	—	43	mA
V_{CC2}-system current consumption	I_{TOTAL2}	—	6.0	—	14.0	mA
Pin 2 voltage	V_2	—	1.8	—	2.2	V
Pin 40 voltage	V_{40}	—	2.7	—	3.3	V
Chrominance system						
R-Y standard gain	G_{RY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	9.5	—	14.5	dB
R-Y/G-Y relative gain	G_{RYGY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	−8.0	—	−4.0	dB
B-Y standard gain	G_{BY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	9.5	—	14.5	dB
B-Y/G-Y relative gain	G_{BYGY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	−20.5	—	−12.5	dB
High-level APC pull-in	AP_H	SG5 (4.43 MHz + 520 Hz, PAL)	500	—	540	Hz
Low-level APC pull-in	AP_L	SG5 (4.43 MHz − 520 Hz, PAL)	−540	—	−500	Hz
ACC output characteristic 1	G_{ACC1}	SG5 (0 dB, 6 dB, NTSC), ch.1 = "80"	−1.0	—	1.0	dB
ACC output characteristic 2	G_{ACC2}	SG5 (0 dB, 6 dB, NTSC), ch.1 = "80"	−1.0	—	1.0	dB
Chrominance killer characteristic 1	V_{KILL1}	SG5 (−30 dB, NTSC) ch.1 = "80", ch.2 = "80", ch.5 = "FF"	400	—	—	mV[p-p]
Chrominance killer characteristic 2	V_{KILL2}	SG5 (−50 dB, NTSC) ch.1 = "80", ch.2 = "80", ch.5 = "FF"	—	—	600	mV[p-p]

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system						
Sharpness control characteristic	G_{SH}	SG1 (2 MHz, NTSC) ch.1 = "80", ch.9 = "80"/"FF"	1.0	—	—	dB
Sharpness frequency characteristic 1	f_{SH1}	SG1 (100 kHz/2 MHz, NTSC) ch.1 = "80"	3.5	—	—	dB
R-ch. contrast adjustment range 1	CTR_{R1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"FF"	1.5	—	—	dB
G-ch. contrast adjustment range 1	CTR_{G1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"FF"	1.5	—	—	dB
B-ch. contrast adjustment range 1	CTR_{B1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"FF"	1.5	—	—	dB
R-ch. contrast adjustment range 2	CTR_{R2}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"80"	—	—	–5.2	dB
G-ch. contrast adjustment range 2	CTR_{G2}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"80"	—	—	–5.2	dB
B-ch. contrast adjustment range 2	CTR_{B2}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"80"	—	—	–5.2	dB
R-ch. pedestal amplitude minimum	$V_{PEDRmin}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "FF" ch.15 = "C0"	—	—	2.0	V[p-p]
G-ch. pedestal amplitude minimum	$V_{PEDGmin}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "FF" ch.15 = "C0"	—	—	2.0	V[p-p]
B-ch. pedestal amplitude minimum	$V_{PEDBmin}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "FF" ch.15 = "C0"	—	—	2.0	V[p-p]

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
R-ch. pedestal amplitude maximum	$V_{PEDRmax}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "00" ch.15 = "C0"	3.0	—	—	V[p-p]
G-ch. pedestal amplitude maximum	$V_{PEDGmax}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "00" ch.15 = "C0"	3.0	—	—	V[p-p]
B-ch. pedestal amplitude maximum	$V_{PEDBmax}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "00" ch.15 = "C0"	3.0	—	—	V[p-p]
G-ch. output DC voltage	V_{GDC}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11 adjustment, ch.15 = "C0"	2.2	—	2.5	V[p-p]
R-ch. gamma characteristic 1	G_{GAMR1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment	−8.5	—	−3.5	dB
G-ch. gamma characteristic 1	G_{GAMG1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment	−8.5	—	−3.5	dB
B-ch. gamma characteristic 1	G_{GAMB1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment	−8.5	—	−3.5	dB
R-ch. gamma characteristic 2	G_{GAMR2}	SG3 (NTSC), ch.1 = "E0", ch.4 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"FF"	−8.2	—	—	dB
G-ch. gamma characteristic 2	G_{GAMG2}	SG3 (NTSC), ch.1 = "E0", ch.4 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"FF"	−8.2	—	—	dB
B-ch. gamma characteristic 2	G_{GAMB2}	SG3 (NTSC), ch.1 = "E0", ch.4 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"FF"	−8.2	—	—	dB
R-ch. gamma characteristic 3	G_{GAMR3}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"60"	−3.5	—	0.5	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
G-ch. gamma characteristic 3	G_{GAMG3}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"60"	−3.5	—	0.5	dB
B-ch. gamma characteristic 3	G_{GAMB3}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"60"	−3.5	—	0.5	dB
R-ch. white limiter low-level	V_{WRRL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "00", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	—	—	3.0	V[p-p]
G-ch. white limiter low-level	V_{WRGL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "00", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	—	—	3.0	V[p-p]
B-ch. white limiter low-level	V_{WRBL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "00", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	—	—	3.0	V[p-p]
R-ch. white limiter high-level	V_{WRRH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	3.2	—	—	V[p-p]
G-ch. white limiter high-level	V_{WRGH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	3.2	—	—	V[p-p]
B-ch. white limiter high-level	V_{WRBH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	3.2	—	—	V[p-p]
R-ch. black limiter low-level	V_{BRRL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.7 = "80", ch.12 = "FF" ch.14 = "40", ch.8/10/11/15 adjustment ch.8 = "00"	3.0	—	—	V
G-ch. black limiter low-level	V_{BRGL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.7 = "80", ch.12 = "FF" ch.14 = "40", ch.8/10/11/15 adjustment ch.8 = "00"	3.0	—	—	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
B-ch. black limiter low-level	V_{BRBL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.7 = "80", ch.12 = "FF" ch.14 = "40", ch.8/10/11/15 adjustment ch.8 = "00"	3.0	—	—	V
R-ch. black limiter high-level	V_{BRRH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF" ch.8/10/11/15 adjustment, ch.7 = "FF" ch.8 = "00", ch.14 = "40"	—	—	1.2	V
G-ch. black limiter high-level	V_{BRGH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF" ch.8/10/11/15 adjustment, ch.7 = "FF" ch.8 = "00", ch.14 = "40"	—	—	1.2	V
B-ch. black limiter high-level	V_{BRBH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF" ch.8/10/11/15 adjustment, ch.7 = "FF" ch.8 = "00", ch.14 = "40"	—	—	1.2	V
R-ch. Y_S threshold 1	V_{tYSR1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = 1 V	0.8	—	—	V[p-p]
G-ch. Y_S threshold 1	V_{tYSG1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = 1 V	0.8	—	—	V[p-p]
B-ch. Y_S threshold 1	V_{tYSB1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = 1 V	0.8	—	—	V[p-p]
R-ch. Y_S threshold 2	V_{tYSR2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = 2.2 V	—	—	0.5	V[p-p]
G-ch. Y_S threshold 2	V_{tYSG2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = 2.2 V	—	—	0.5	V[p-p]
B-ch. Y_S threshold 2	V_{tYSB2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = 2.2 V	—	—	0.5	V[p-p]
R-ch. black level	CHR_{RB}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = SG7	− 0.6	—	0.6	V
G-ch. black level	CHR_{GB}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = SG7	− 0.6	—	0.6	V
B-ch. black level	CHR_{BB}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = SG7	− 0.6	—	0.6	V

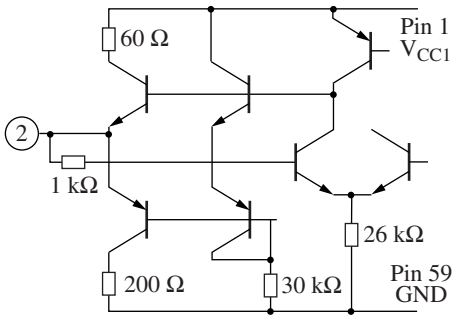
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
R-ch. black level width	$WCHR_{RB}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = SG7	2.25	—	3.75	µs
G-ch. black level width	$WCHR_{GB}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = SG7	2.25	—	3.75	µs
B-ch. black level width	$WCHR_{BB}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 16 = SG7	2.25	—	3.75	µs
R-ch. CHR threshold 1	V_{tCHR1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 12 = 1 V	1.5	—	—	V[p-p]
G-ch. CHR threshold 1	V_{tCHG1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 13 = 1 V	1.5	—	—	V[p-p]
B-ch. CHR threshold 1	V_{tCHB1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 14 = 1 V	1.5	—	—	V[p-p]
R-ch. CHR threshold 2	V_{tCHR2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 12 = 2.2 V	3.0	—	—	V[p-p]
G-ch. CHR threshold 2	V_{tCHG2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 13 = 2.2 V	3.0	—	—	V[p-p]
B-ch. CHR threshold 2	V_{tCHB2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 14 = 2.2 V	3.0	—	—	V[p-p]
R-ch. white level	CHR_{RW}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 12 = SG7	2.0	—	—	V[p-p]
G-ch. white level	CHR_{GW}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 13 = SG7	2.0	—	—	V[p-p]
B-ch. white level	CHR_{BW}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 14 = SG7	2.0	—	—	V[p-p]
R-ch. white level width	$WCHR_{RW}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 12 = SG7	2.25	—	3.75	µs
G-ch. white level width	$WCHR_{GW}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 13 = SG7	2.25	—	3.75	µs

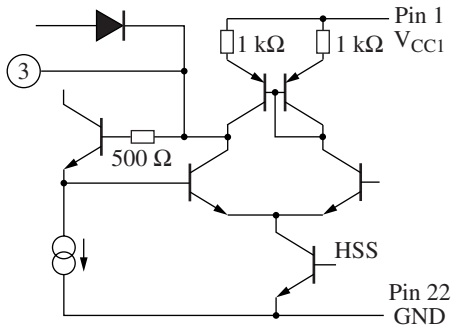
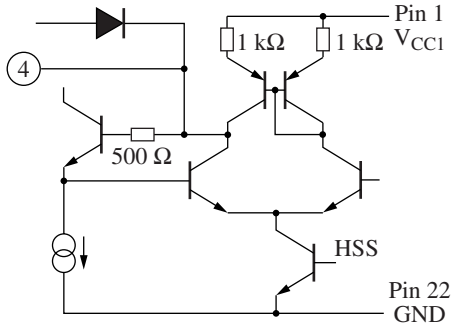
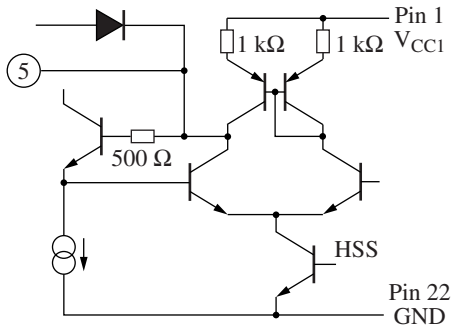
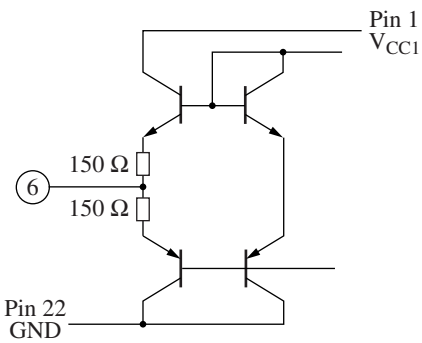
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
B-ch. white level width	$WCHR_{BW}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, pin 14 = SG7	2.25	—	3.75	µs
R-ch. RGB2 relative amplitude	V_{RGB2R}	SG2 (NTSC), ch.1 = "A0" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, ch.3 = "40" ch.6 = "40", pin 42 = 2.2 V	– 0.45	—	0.45	V[p-p]
B-ch. RGB2 relative amplitude	V_{RGB2B}	SG2 (NTSC), ch.1 = "A0" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, ch.3 = "40" ch.6 = "40", pin 42 = 2.2 V	– 0.45	—	0.45	V[p-p]
Synchronizing system						
Horizontal sync. pulse low-level	V_{HDL}	—	—	—	0.4	V
Horizontal sync. pulse amplitude	V_{HD}	—	4.0	—	—	V[p-p]
Horizontal sync. pulse width	t_{HD}	—	4.86	—	6.86	µs
Vertical sync. pulse low-level	V_{VDL}	—	—	—	0.4	V
Vertical sync. pulse amplitude	V_{VD}	—	4.0	—	—	V[p-p]
Horizontal sync. separation pulse high-level	V_{HSSH}	SG2 (NTSC)	4.0	—	—	V
Horizontal sync. separation pulse amplitude	V_{HSS}	SG2 (NTSC)	4.0	—	—	V[p-p]
Horizontal sync. separation pulse width	t_{HSS}	SG2 (NTSC)	3.8	—	5.8	µs
Horizontal sync. pulse free-run frequency	f_{HD}		15.434	—	16.034	kHz

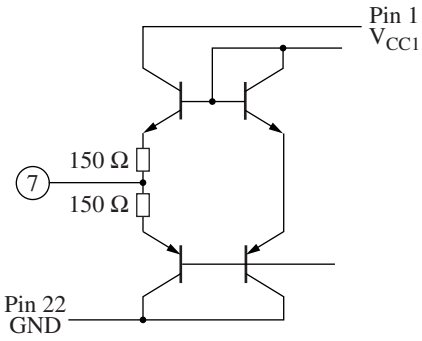
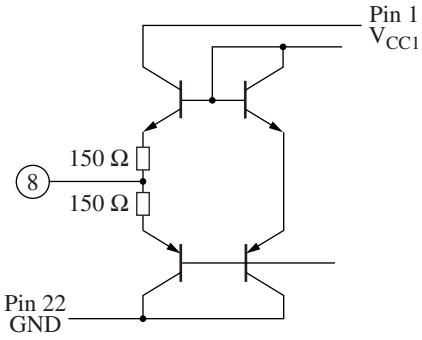
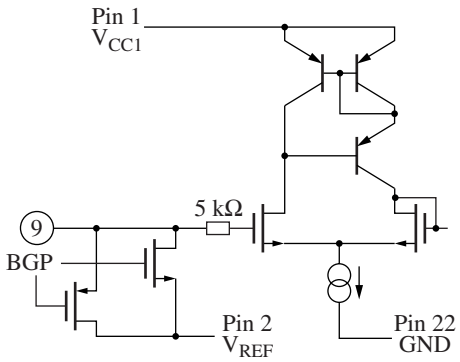
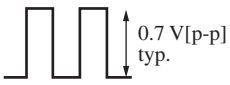
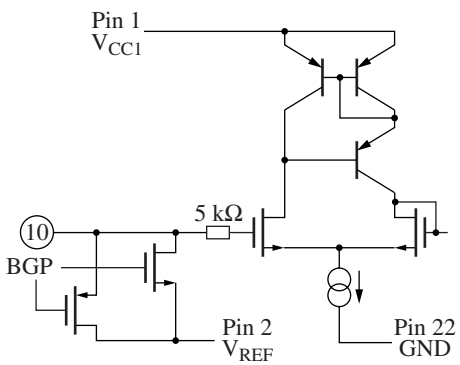
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage · Waveform
1	—	V_{CC1}: 5.0 V-system power supply pin Supply current 40 mA typ.	—
2		V_{REF}: Reference voltage output pin 2.0 V typ.	—

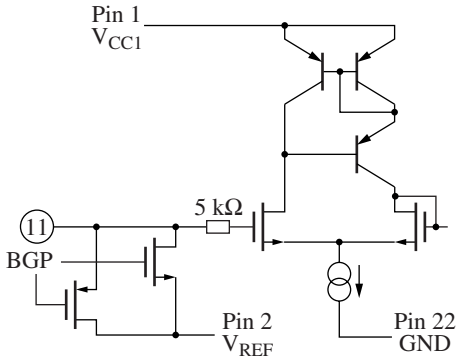
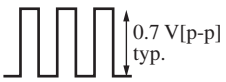
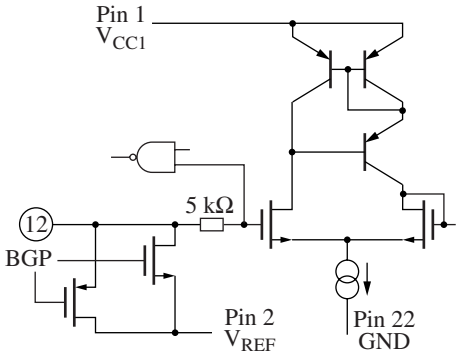
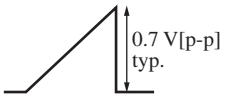
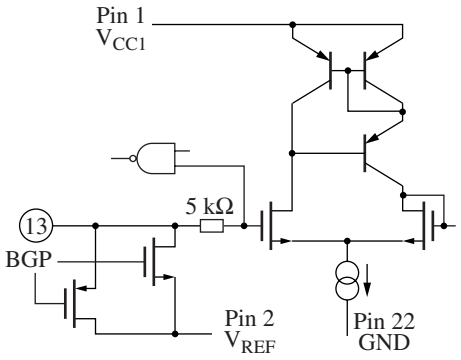
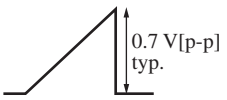
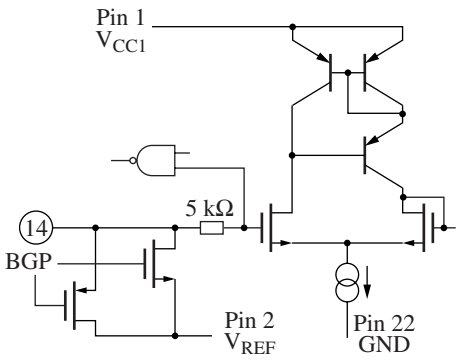
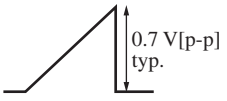
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
3		R-ch. det.: R-ch. clamping capacitor coupling pin	—
4		G-ch. det.: G-ch. clamping capacitor coupling pin	—
5		B-ch. det.: B-ch. clamping capacitor coupling pin	—
6		Dec.R-out: Output pin of R signal demodulated from video signal	

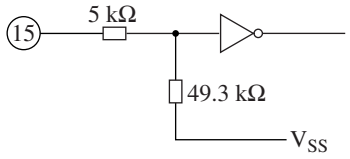
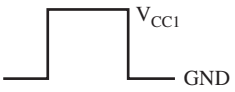
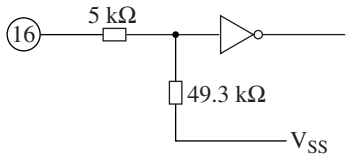
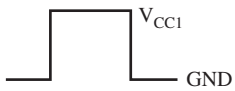
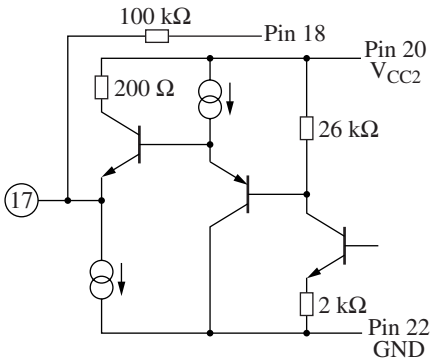
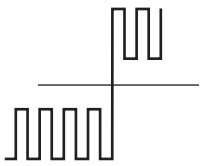
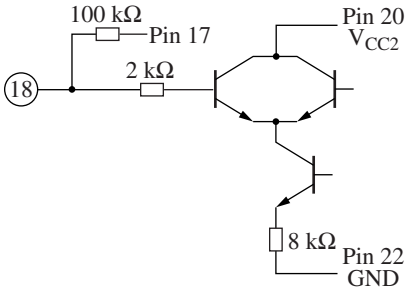
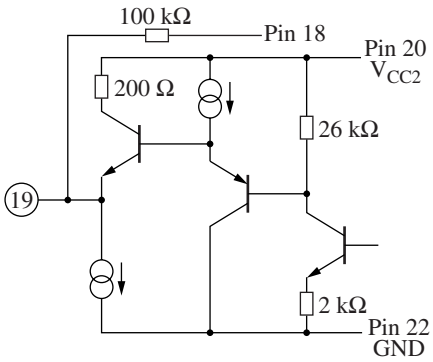
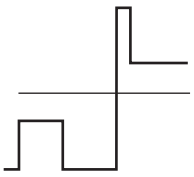
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
7		Dec.G-out: Output pin of G signal demodulated from video signal	
8		Dec.B-out: Output pin of B signal demodulated from video signal	
9		R-in 1: Analog R signal input	Analog R signal 
10		G-in 1: Analog G signal input	Analog G signal 

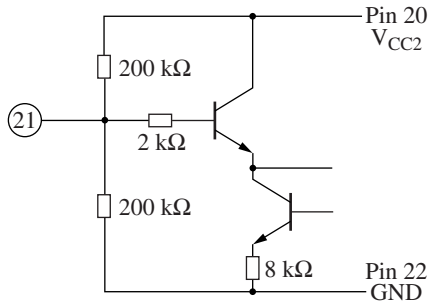
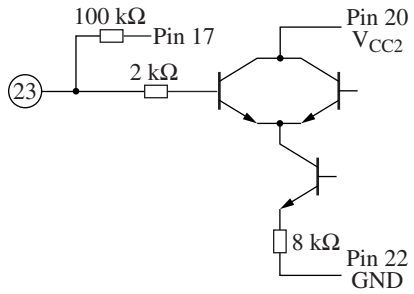
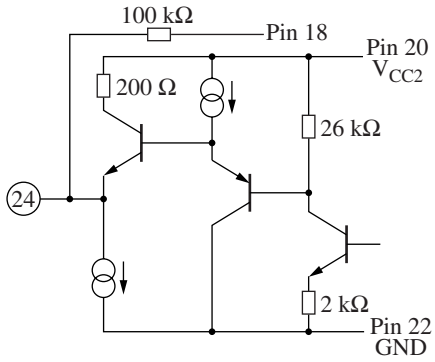
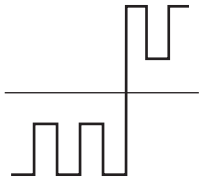
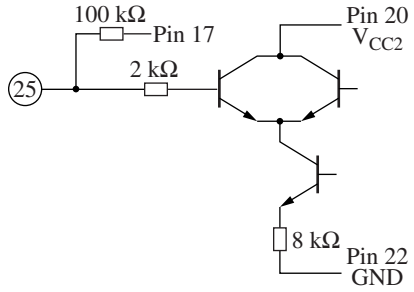
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
11		B-in 1: Analog B signal input	Analog B signal 
12		R-in 2: Character insertion signal input for R-ch., supporting analog and digital OSD.	Analog OSD  Digital OSD 
13		G-in 2: Character insertion signal input for G-ch., supporting analog and digital OSD.	Analog OSD  Digital OSD 
14		B-in 2: Character insertion signal input for B-ch., supporting analog and digital OSD.	Analog OSD  Digital OSD 

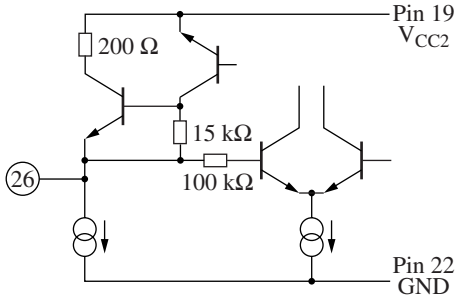
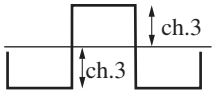
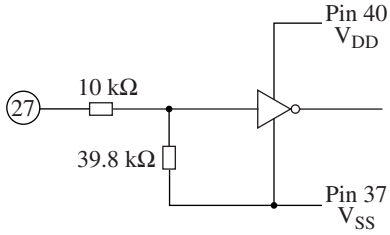
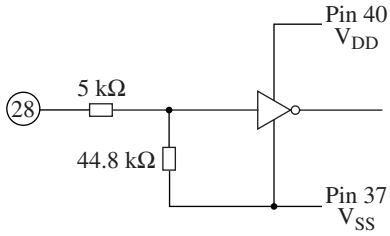
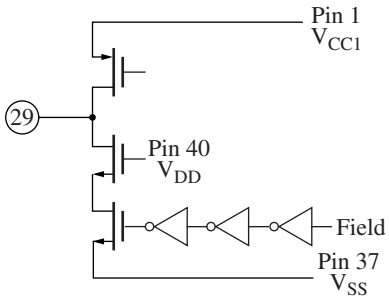
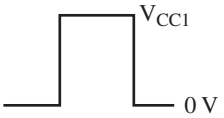
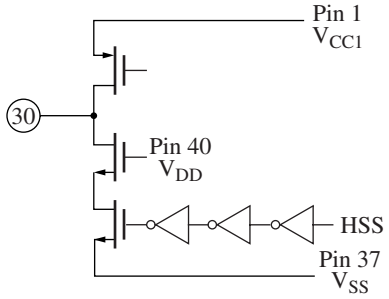
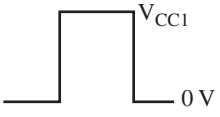
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
15		BLAK: Black level indication control signal input pin	
16		Y_S: Character picking up signal input	
17		B-out: B signal output pin	
18		B-ch.AVE det.: B-ch. output DC feedback detection pin	—
19		G-out: G signal output pin	
20	—	V_{CC2}: 7.5 V system power supply Supply current 12 mA typ.	—

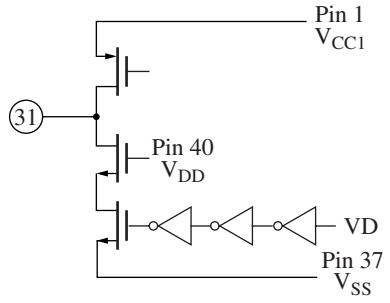
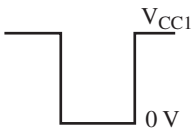
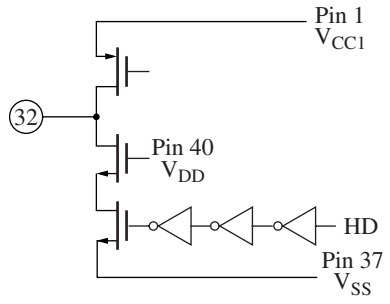
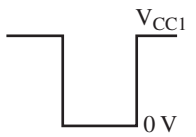
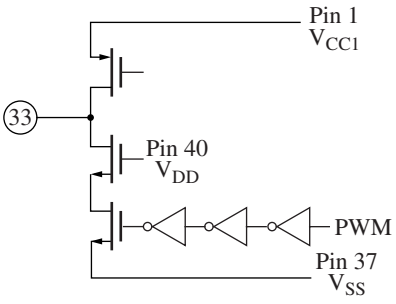
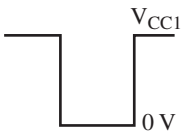
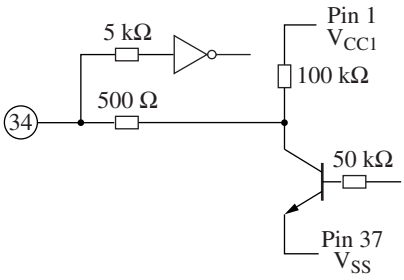
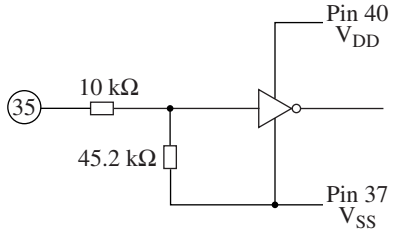
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
21		AVE: R,G,B output DC reference voltage pin	—
22	—	GND 2: Drive circuit system GND	—
23		G-ch.AVE det.: G-ch. output DC feedback detection pin	—
24		R-out: R signal output pin	
25		R-ch.AVE det.: R-ch. output DC feedback detection pin	—

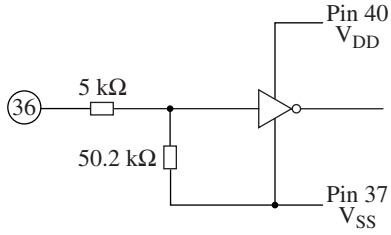
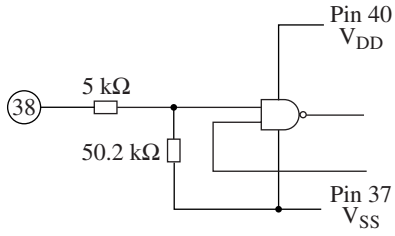
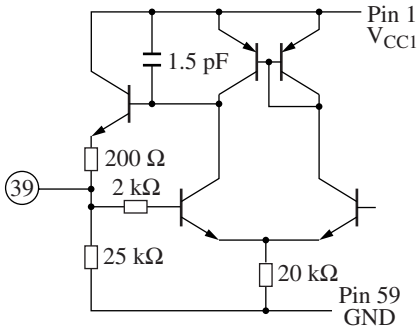
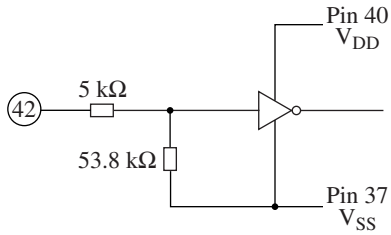
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
26		Common out: Opposed voltage output pin for common. Output impedance; Approx. 150 Ω	
27		Test mode: Logic test mode start signal input pin; "Open" or "GND" normally	High or Low
28		Test CLK: Logic test pulse input pin; "Open" or "GND" normally	High or Low
29		Field: Field identifying signal output pin	Output waveform 
30		HSS: Composite synchronizing signal output pin	Output waveform 

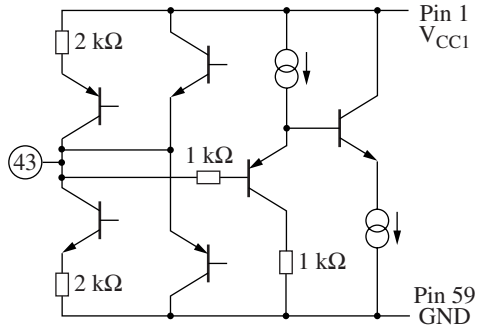
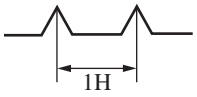
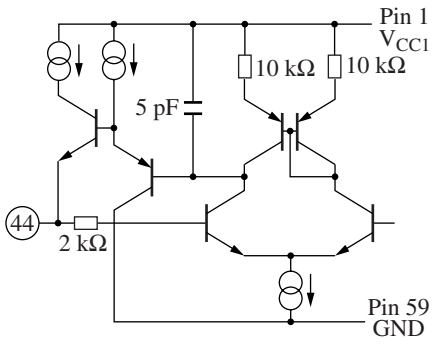
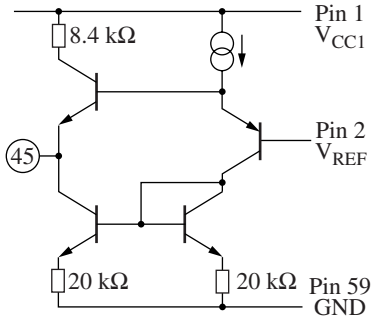
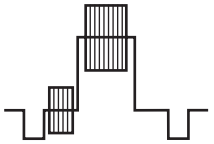
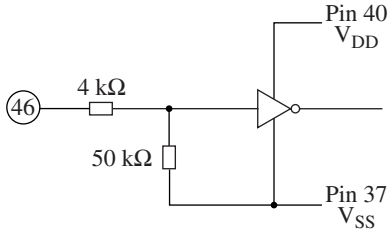
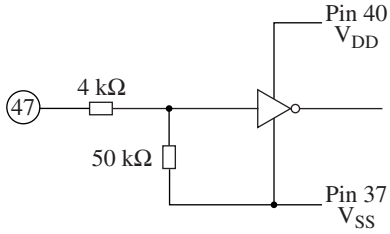
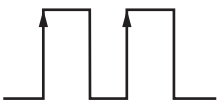
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
31		VD: Vertical synchronizing signal output pin	Output waveform 
32		HD: Horizontal synchronizing signal output pin	Output waveform 
33		PWM: PWM signal output pin	Output waveform 
34		RST: Capacitor coupling pin for power-on reset	—
35		VDB in: Vertical synchronizing pulse input pin	High or Low

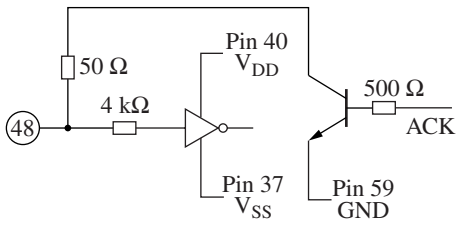
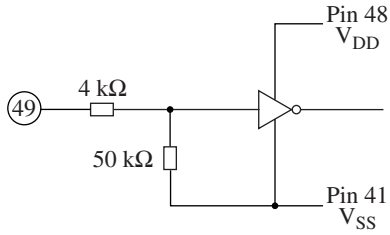
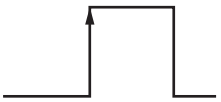
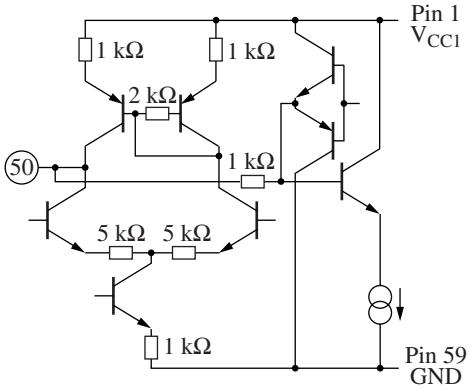
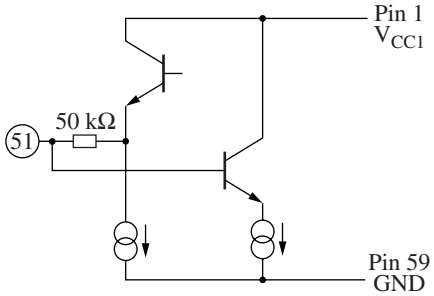
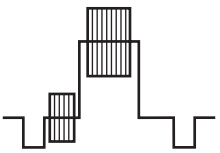
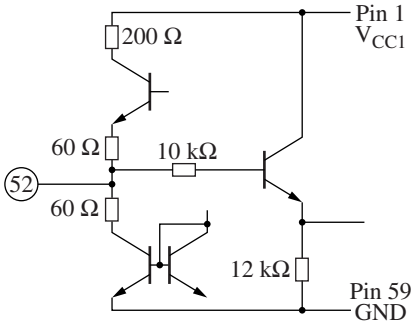
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
36		Ext. pol.: 1H reverse signal input pin	High or Low
37	—	V_{SS}: MOS system GND	—
38		Clamp in: Clamp pulse input pin Valid only in the external clamp mode. Positive polarity input.	High or Low
39		DAC mon.: DAC DC voltage output pin	DC
40	—	V_{DD}: Capacitor connection pin for MOS part power supply. 3.0 V typ.	—
41	—	GND 3: Pulse system GND	—
42		PRGB: Analog OSD signal input Mode start-up signal input pin Valid only in the analog OSD mode High = analog OSD start up	High or Low

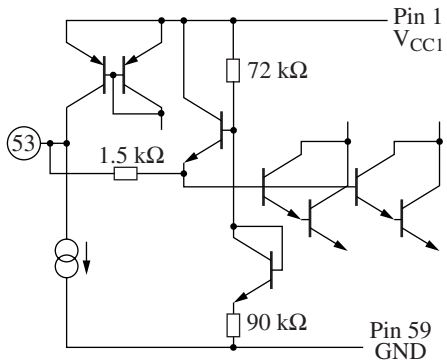
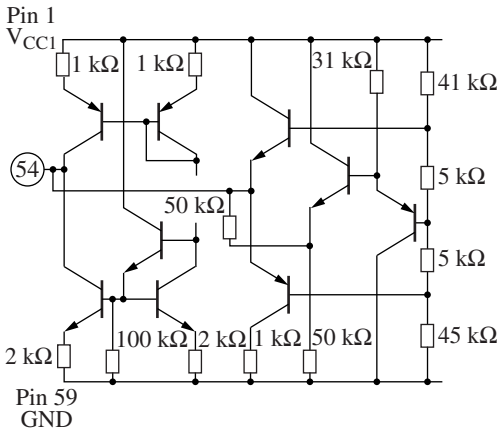
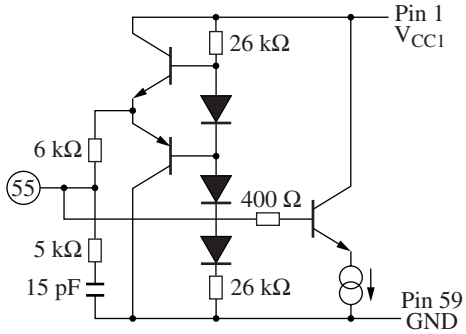
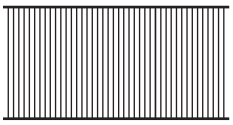
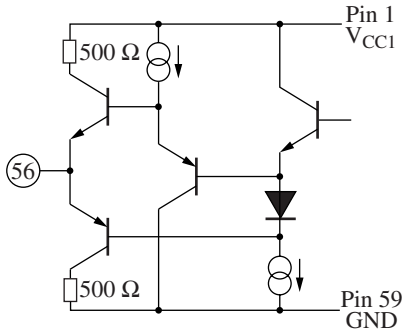
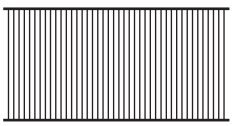
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
43		AFC det.: AFC filter connection pin Input impedance; 100 kΩ or more	
44		H f_O: VCO oscillation frequency adjusting resistor connection pin	—
45		HSS in: H-sync. input pin Separates a sync. signal from luminance signal (video signal)	Input signal example: Video signal 
46		Bus-ch: Switching pin for 3-line serial control/I^2C bus control High = I^2C bus Open or Low = 3-line serial control	High or Low
47		DAC: Serial clock input pin	

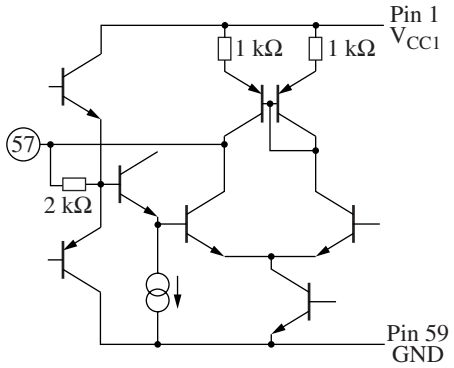
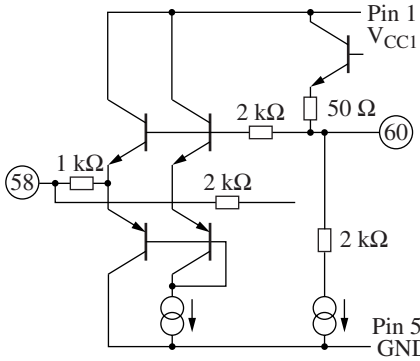
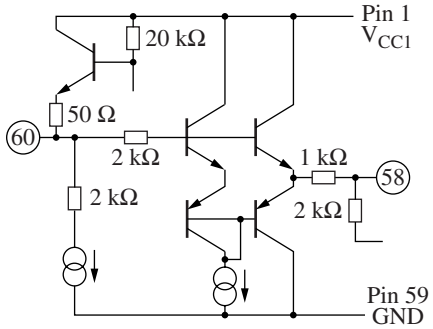
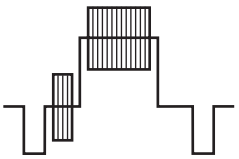
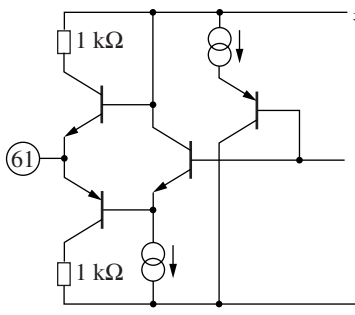
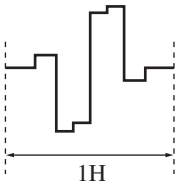
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
48		DAT: Serial data input pin	
49		LEN: Load pulse input pin, also works as the slave address conversion pin in the I^2C mode. High = "88" Low = "8A"	High or Low 
50		ACC det.: ACC capacitor connecting pin, adjusting the amplitude of a burst signal automatically	—
51		C in: Chrominance signal input pin Input chrominance signal (video signal)	Input signal example: Video signal 
52		L.det.: Capacitor coupling pin for the horizontal unlock detecting circuit	—

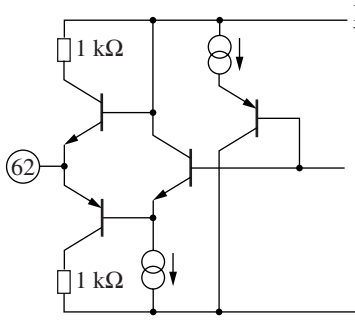
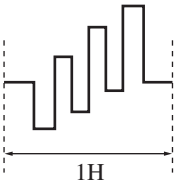
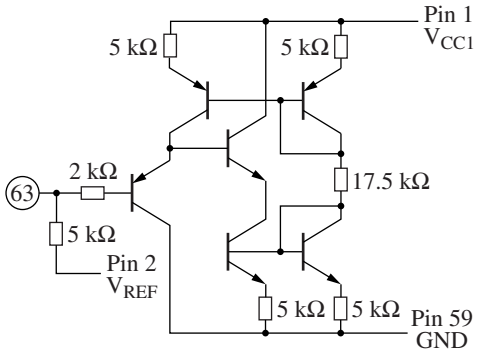
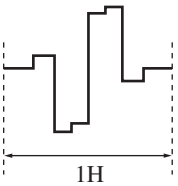
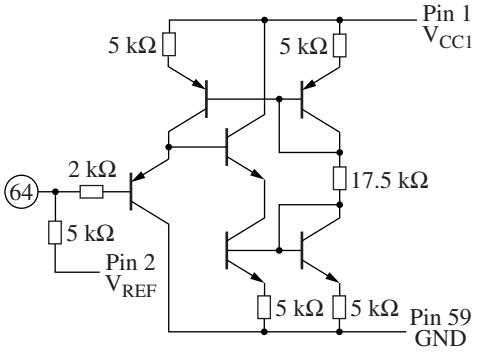
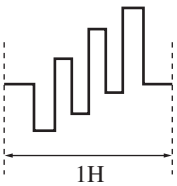
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
53		Kill det.: Killer capacitor coupling pin. To prevent degradation of image in a small amplitude of a burst signal, this pin stops a chroma signal and the mode changes to black and white mode.	—
54		APC det.: APC capacitor coupling pin. Matching the phase of a crystal oscillation to that of burst signal.	—
55		VXOI: Crystal oscillator connecting pin The pair with pin 56	NTSC 3.58 MHz PAL 4.43 MHz 
56		VXOO: Crystal oscillator connecting pin. The pair with pin 55 Output impedance; Approximately 100 Ω	NTSC 3.58 MHz PAL 4.43 MHz 

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
57		Y-det.: Capacitor coupling pin for luminance signal clamping	—
58		Trap: Trap connecting pin Trapping a chrominance signal by connecting external inductor and capacitor. Not necessary in case that an input signal is a component.	—
59	—	GND 3: GND for chrominance and luminance signal process blocks	—
60		Y-in: Luminance signal input pin Input luminance signal (video signal)	Input signal example: Video signal 
61		R-Y out: R-Y signal output pin, demodulated from a video signal	R-Y signal 

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
62		B-Y out: B-Y signal output pin, demodulated from a video signal	B-Y signal 
63		R-Y in: R-Y signal input pin in a color difference mode and in standard PAL.	R-Y signal 
64		B-Y in: B-Y signal input pin in a color difference mode and in standard PAL.	B-Y signal 

■ Usage Notes

- Evaluated throughly on the application of this device in PAL.
- If the duty of PWM output is set to other than 0% or 100%, the jitter of the HD output increases. So, confirm the horizontal jitter amount by all means on the screen of the application product in which the PWM function is used.

■ Technical Data

1. Serial interface description

1) Serial data control

In addition to its serial control by the conventional 3-line method, the AN2526NFH can be controlled by the I^2C bus. The communication method is selected by the voltage to be applied to pin 46.

3-line control mode: pin 46 = low (connect to GND)

I^2C Bus mode: pin 46 = high (pin 41: connect to V_{DD})

It is recommended that the serial data is transferred during a vertical blanking period.

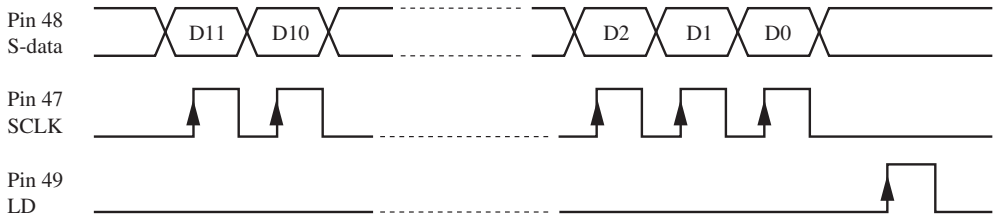
2) 3-line control mode

A serial data is of 3-line system transmitting three kinds of signals of data, shift clock and load pulse independently. The data communicated is made up by 12 bits in total of address (4 bits) and data (8 bits). The DAC is composed of four blocks of serial-parallel conversion, address decoder, data latch and ladder resistors, enabling to control 16 channels in total. Further, the mode setting such as the input signal switching is done by a serial data to reduce the pin count.

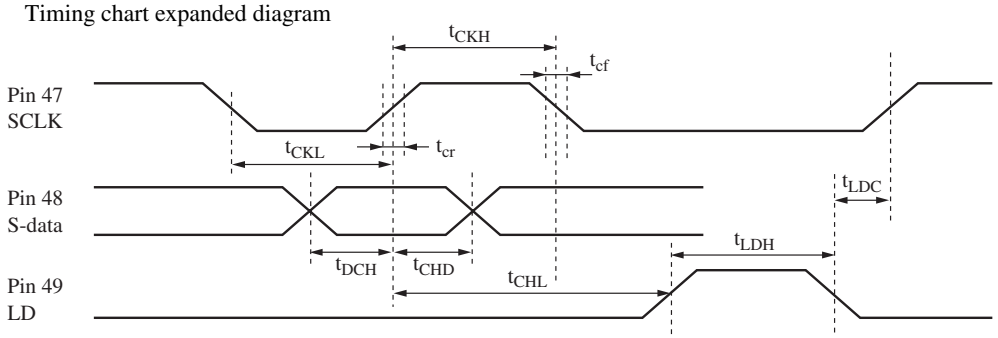
(1) Serial data format

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address block				Data block							

(2) Serial data input timing chart



Timing chart expanded diagram



■ Technical Data (continued)

1. Serial interface description (continued)

2) 3-line control mode (continued)

(2) Serial data input timing chart (continued)

Parameter	Symbol	Min	Max	Unit
Clock low-level pulse width	t_{CKL}	500	—	ns
Clock high-level pulse width	t_{CKH}	500	—	ns
Clock rise time	t_{cr}	—	20	ns
Clock fall time	t_{cf}	—	20	ns
Data setup time	t_{DCH}	30	—	ns
Data hold time	t_{CHD}	60	—	ns
Load setup time	t_{CHL}	200	—	ns
Load hold time	t_{LDC}	100	—	ns
Load high-level pulse width	t_{LDH}	500	—	ns

(3) Mode setting channel bits table

D11	D10	D9	D8	Selection-ch.	EVR control function	Number of bits
0	0	0	0	0	Vertical sync. signal output position	3
1	0	0	0	1	Horizontal sync. signal output position	5
0	1	0	0	2	PWM duty	6
1	1	0	0	3	Common pulse amplitude	7
0	0	1	0	4	Y-gain	8
1	0	1	0	5	Color gain	7
0	1	1	0	6	Hue	7
1	1	1	0	7	Black-limiter level	8
0	0	0	1	8	Brightness	8
1	0	0	1	9	Y-aperture gain	8
0	1	0	1	10	R-ch. sub-brightness	8
1	1	0	1	11	B-ch. sub-brightness	8
0	0	1	1	12	White peak limiter level	8
1	0	1	1	13	Gamma-1 Knee level	8
0	1	1	1	14	Gamma-2 Knee level	8
1	1	1	1	15	RGB contrast	7

The mode setting of the each channel that the data bits number is less than 8 is made by using the data of the data block.
The contents of each mode setting are shown next.

■ Technical Data (continued)

1. Serial interface description (continued)

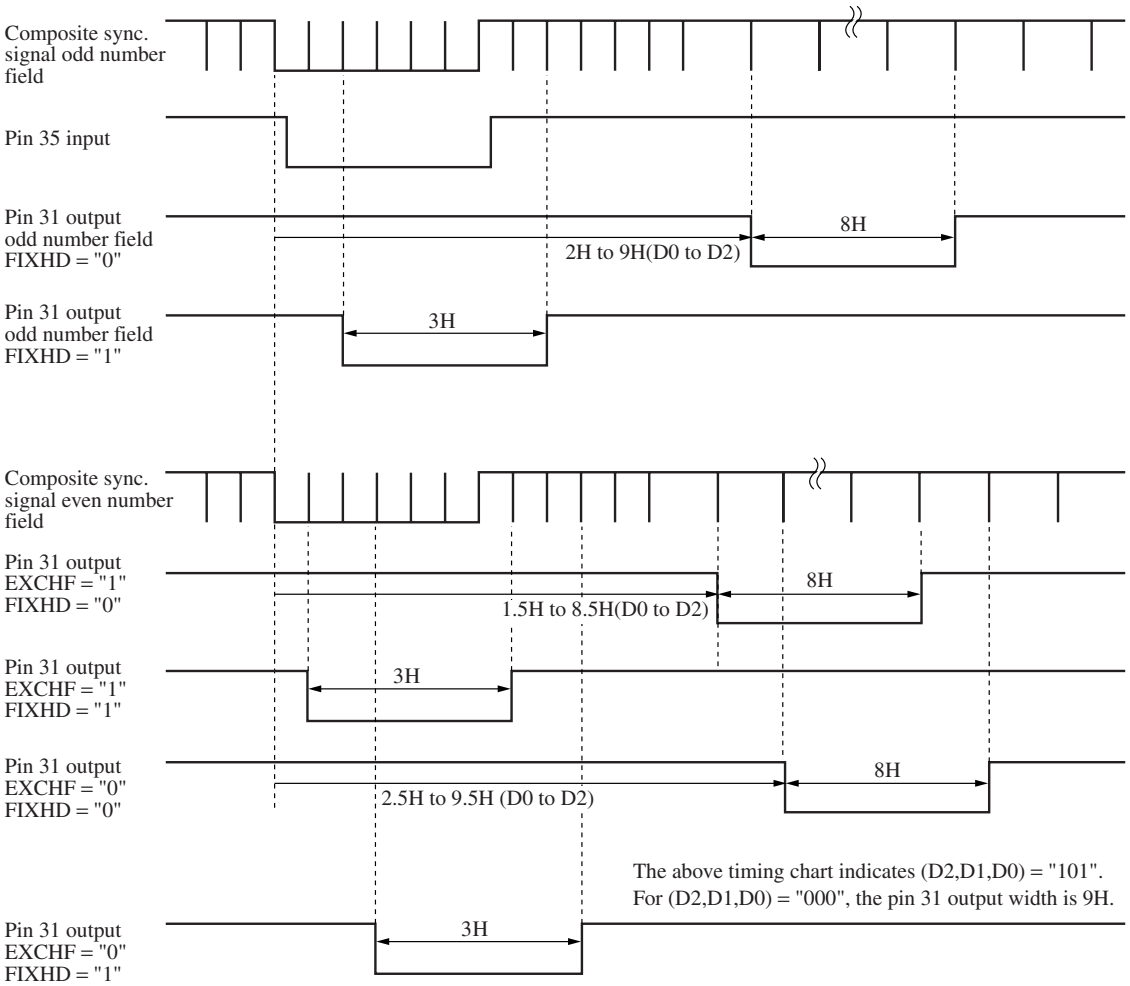
2) 3-line control mode (continued)

(3) Mode setting channel bits table (continued)

• ch.0: Vertical sync. output position adjustment

D11	D10	D9	D8	D7	D6	D5	D4 to D3	D2	D1	D0
				EXCHF	FIXHD	BOSC	Hor. PLL start position adjustment			
0	0	0	0	—	—	0	Automatic switching			
				—	—	1	263H/313H fixed (NTSC/PAL)			
				—	0	HD/VD output timing is serially variable				
				—	1	HD/VD output timing fixed				
				0	Odd number field: Advanced phase					
				1	Even number field: Advanced phase					

<Vertical sync. output timing adjusting range>



The pin 31 timing is synchronous with the pin 35 input timing.
The above timing chart is just for reference.

■ Technical Data (continued)

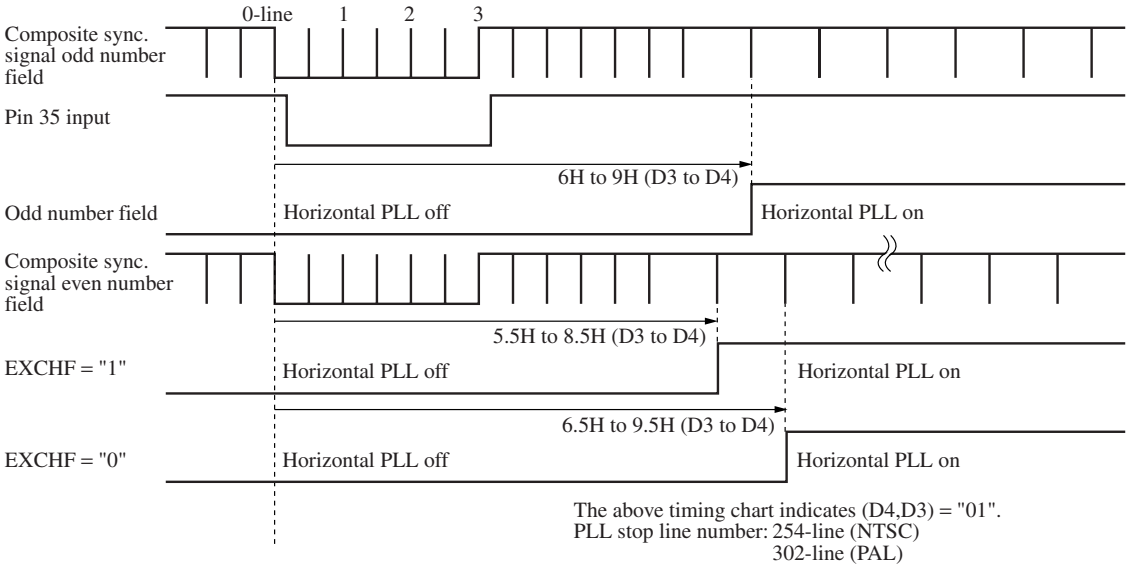
1. Serial interface description (continued)

2) 3-line control mode (continued)

(3) Mode setting channel bits table (continued)

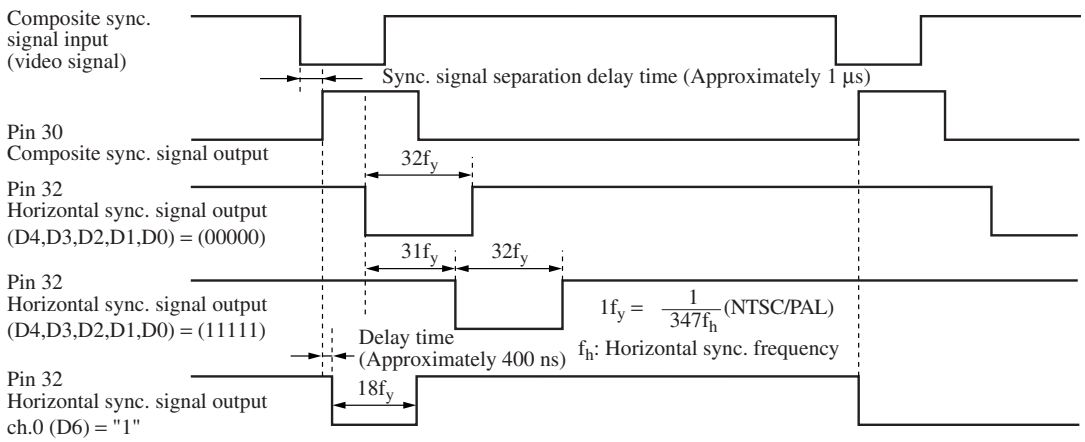
• ch.0: (continued)

<Horizontal PLL start position adjustment range>



• ch.1: Horizontal sync. output position adjustment

D11	D10	D9	D8	D7 V Mode	D6 YUV	D5 RGB	D4	D3	D2	D1	D0
1	0	0	0	—	—	0	Video signal input display mode				
				—	—	1	Analog RGB input display mode				
				—	0	Chrominance signal input mode					
				—	1	Color-difference signal input mode					
				0	PAL						
				1	NTSC						



■ Technical Data (continued)

1. Serial interface description (continued)

2) 3-line control mode (continued)

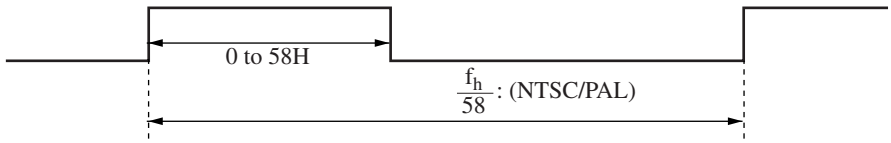
(3) Mode setting channel bits table (continued)

• ch.1: Horizontal sync. output position adjustment (continued)

The delay time of pin 30 output to video signal is likely to vary according to an external constant connected to pin 45. For an external constant, the characteristics in weak electric field must be evaluated adequately. Though the horizontal sync. signal output adjustment range is designed by referring to the center of pin 30 output pulse, there would be some error according to VCO free-run frequency.

• ch.2: PWM duty adjustment

D11	D10	D9	D8	D7 P mode	D6 YC mode	D5	D4	D3	D2	D1	D0
0	1	0	0	—	0	Composite input mode					
				—	1	Component input mode					
				0	Standard PAL mode						
				1	Quasi PAL/NTSC mode						



Note that adjustment characteristics come to discontinuation around max. duty.

(D5,D4,D3,D2,D1,D0) = (000000): t_w = 1H
= (000001): t_w = 3H
= (000010): t_w = 4H
= (110110): t_w = 56H
= (110111): t_w = 56H
= (111000): t_w = 0H
= (111001): t_w = 58H

• ch.3: Common pulse amplitude adjustment

D11	D10	D9	D8	D7 OSD	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	Analog OSD signal input mode						
				1	Digital OSD signal input mode						

• ch.5: Color gain adjustment

D11	D10	D9	D8	D7 HTS	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	1H reverse inhibit mode						
				1	1H reverse mode						

• ch.6: Hue adjustment

D11	D10	D9	D8	D7 CP	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	External clamp pulse input mode						
				1	Internal clamp (pedestal) mode						

■ Technical Data (continued)

1. Serial interface description (continued)

2) 3-line control mode (continued)

(3) Mode setting channel bits table (continued)

• ch.9: Y-aperture gain adjustment

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	00h, 01h: Test mode							

• ch.15: RGB contrast adjustment

D11	D10	D9	D8	D7 POL mode	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	Internal POL 1H reverse mode						
				1	External POL 1H reverse mode						

3) I^2C bus control mode

A serial data is capable of transferring 9-bit unit of 8-bit transfer data and 1-bit answering data using two kinds of signal lines of data and shift clock.

When a slave address after setting a start condition matches the address on the IC side, you can receive the data to be transmitted from then. Once the stop condition is set up, the next transmitting data will be ignored until the start condition is set up.

There are two kinds of transfer mode: an auto-increment mode which does not transmit subaddress, and data upgrade mode which transmits subaddress + data by 2 bytes.

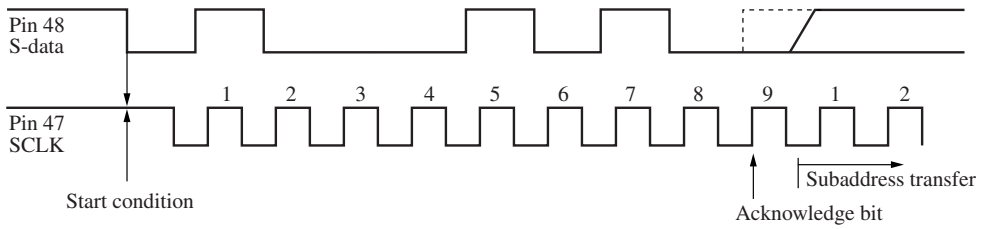
The typical models of communication sequence are shown below:

(1) Start condition

When the S-data changes from high level to low level at SCLK = high level, a data receiving mode becomes available.

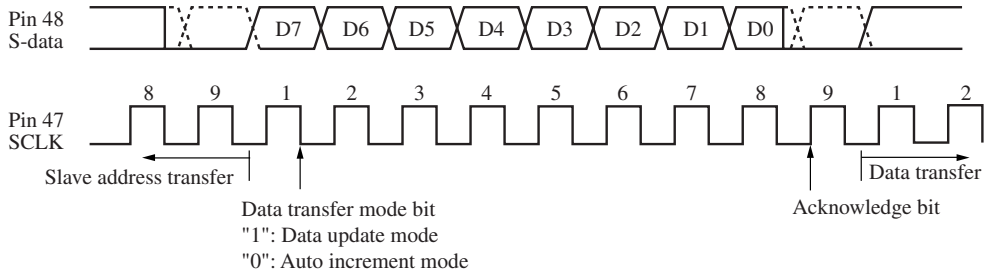
(2) Slave address transfer

The slave address of the AN2526NFH is 88h at pin 49 = high level and 8Ah at pin 49 = low level.



(3) Subaddress transfer

When a data transfer mode bit is 0, all the serial data columns transferred until a stop condition is set is regarded as the data block.

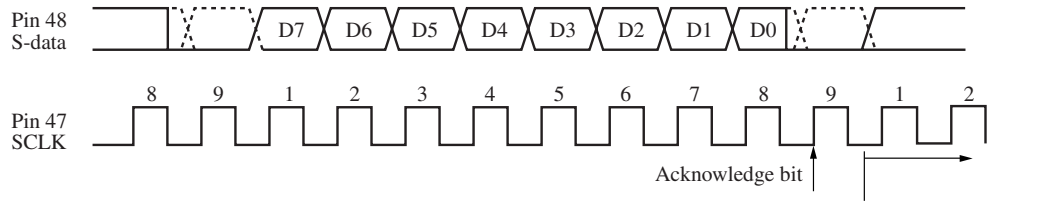


■ Technical Data (continued)

1. Serial interface description (continued)

3) I^2C bus control mode (continued)

(4) Data transfer



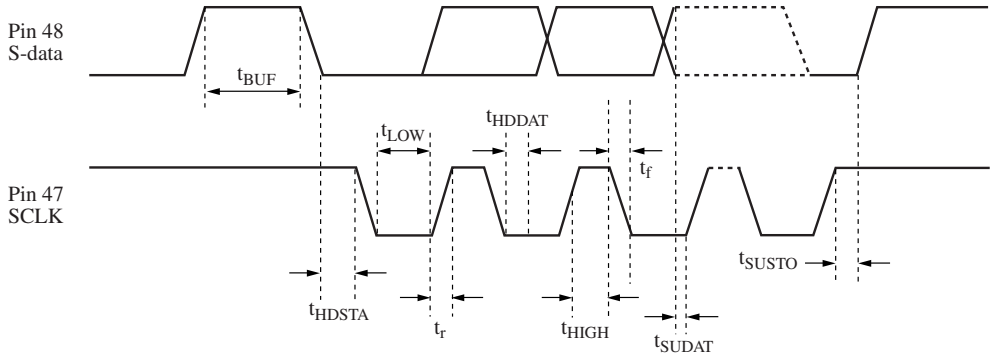
At auto increment mode: Data transfer
At data update mode: Subaddress transfer

(5) Stop condition

When S-data changes from low level to high level at SCLK = high level, data reception is halted.

(6) Pulse timing

Timing chart expanded diagram



Parameter	Symbol	Min	Typ	Max	Unit
SCLK clock frequency	t_{SCL}	0	—	400	kHz
Bus free-time for stop condition and start condition	t_{BUF}	1.3	—	—	µs
Hold time start condition	t_{HDSTA}	0.6	—	—	µs
SCLK clock low-state hold time	t_{LOW}	1.3	—	—	µs
SCLK clock high-state hold time	t_{HIGH}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	—	µs
Data setup time	t_{SUDAT}	100	—	—	ns
S-data and SCLK signal rise time	t_r	—	—	300	ns
S-data and SCLK signal fall time	t_f	—	—	300	ns
Stop condition setup time	t_{SUSTO}	0.6	—	—	µs

■ Technical Data (continued)

1. Serial interface description (continued)

3) I^2C bus control mode (continued)

(6) Pulse timing (continued)

D7	D6 to D4	D3	D2	D1	D0	Selection channel	EVR control function	Number of bits
Mode	Don't Care	0	0	0	0	0	Vertical sync. signal output position	3
		0	0	0	1	1	Horizontal sync. signal output position	5
		0	0	1	0	2	PWM duty	6
		0	0	1	1	3	Common pulse amplitude	7
		0	1	0	0	4	Y-gain	8
		0	1	0	1	5	Color gain	7
		0	1	1	0	6	Hue	7
		0	1	1	1	7	Black-limiter level	8
		1	0	0	0	8	Brightness	8
		1	0	0	1	9	Y-aperture gain	8
		1	0	1	0	10	R-ch. sub-brightness	8
		1	0	1	1	11	B-ch. sub-brightness	8
		1	1	0	0	12	White peak limiter	8
		1	1	0	1	13	Gamma-1 Knee level	8
		1	1	1	0	14	Gamma-2 Knee level	8
		1	1	1	1	15	RGB contrast	7

The mode setting of the each channel that the data bits number is less than 8 is made by using the data of the data block.
The content of each mode setting is same as three-wire control mode

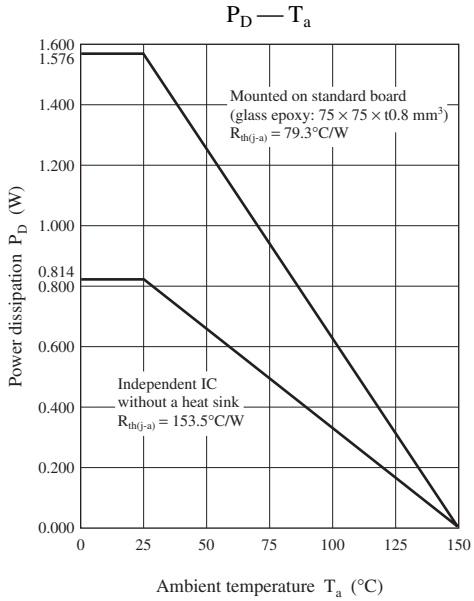
2. Recommended Operating Conditions

Parameter	Symbol	Range	Min	Typ	Max	Unit
Composite video input signal	Y_{IN}	Sync. chip - white	0.9	1.0	1.1	V[p-p]
Y-input signal voltage	Y_{IN}	Pedestal - white	0.6	0.7	0.8	V[p-p]
C-input signal voltage	C_{IN}	Burst signal amplitude	200	300	400	mV[p-p]
MOS input signal low-level voltage	V_{MOSL}		0	—	0.8	V
MOS input signal high-level voltage	V_{MOSH}		2.3	—	*1	V
Synchronizing signal input	H_{SYNC}	Pedestal - sync. chip	0.2	0.3	0.4	V[p-p]
Serial data transfer frequency	f_{SD}		—	—	1.0	MHz
Analog RGB input signal	RGB_{IN}	Pedestal - white	0.6	0.7	0.8	V[p-p]

Note) *1: Set it lower than V_{CC1} (Pin 1 voltage).

■ Technical Data (continued)

3. Power dissipation of package QFP064-P-1010



■ Application Notes

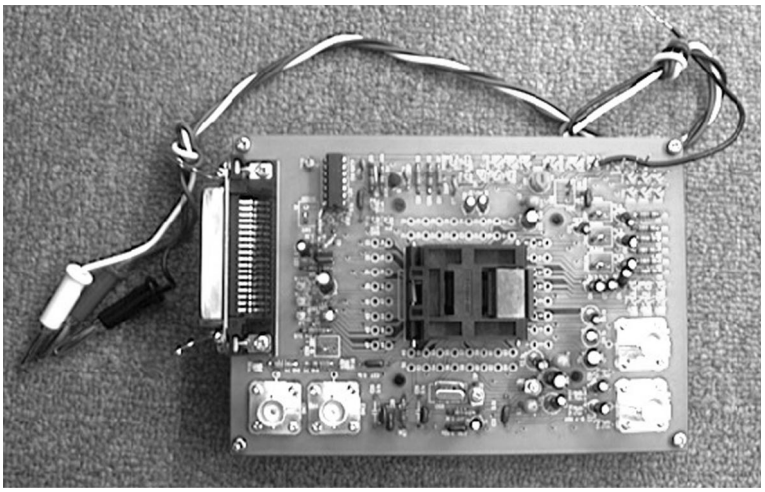
Shown below is the evaluation kit dedicated for AN2526/AN2526NFH. The characteristic chart or figures described on this data represent the typical ones for these two devices.

The kit is used by applying voltages of +5 V and +7.5 V.

A 3-line serial control is available via a parallel port of the personal computer. (AN2526/AN2526NFH features I^2C bus control.)

It is necessary to install the software, attached to this kit, into the specified folder of personal computer before using the kit.

(For details, refer to the paragraph of 3-line serial software installation.)



Evaluation kit for AN2526/AN2526NFH

■ Application Notes (continued)

[1] Description on IC inner operation

1. Operation of each block

Described below are the functions of signal processing block of AN2526/AN2526NFH including 1) brightness signal processing, 2) chrominance signal processing 3) driver and 4) synchronizing processing.

Measurements are done with V_{CC1} / V_{CC2} = 5.0 V/ 7.5 V unless otherwise specified.

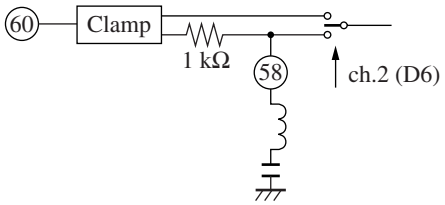
1) Brightness signal processing block

(1) Brightness signal input

Input of brightness signal processing block is pin 60, which is commonly used as an input pin for both composite and component video signals. For composite video signal, connect an LC serial resonant trap filter to pin 58 to reject chrominance signal element and for a large chroma leak of LCD drive output, use an adjusted trap or adjust a serial resonance point with a trimmer capacitor. There is no need for rejection of chroma element in component video signal, thus allowing for evasion of effect of pin 58 floating capacitance through serial control. Since pin 60 is a sync tip clamp type (diode clamp), set a signal source impedance of input signal to 100 Ω or less.

Video signal standard input level = 1 V[p-p]

Pin 58 output impedance = 1 kΩ ± 100 Ω



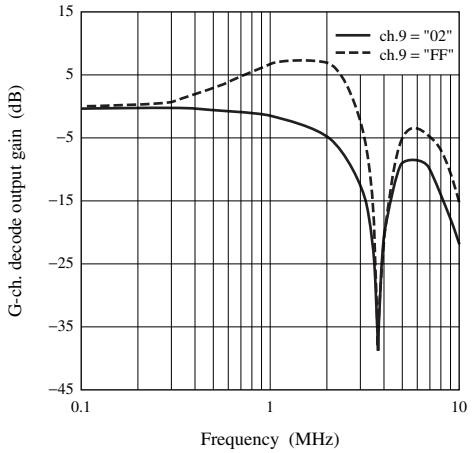
(2) Brightness signal sync cut circuit

Clamp a pedestal part of brightness signal and cut horizontal synchronizing signal to secure the dynamic range of post circuit signal processing block. Connect a capacitor of approx. 0.1 µF to pin 57 to maintain potential during horizontal period.

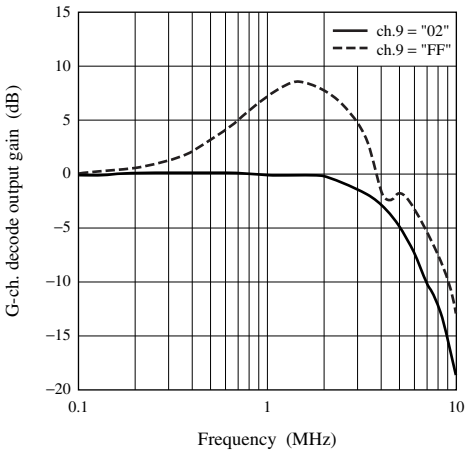
(3) Aperture circuit

An aperture circuit is made up by two stages of broad- band DL circuit constituting a secondary differentiated type circuit. The secondary differentiated signal superposed on a main signal can be adjusted by DAC ch.9. Frequency characteristics covering from input on pin 60 until video signal decode output are shown below.

Y-frequency characteristics (with Trap)



Y-frequency characteristics (without Trap)



■ Application Notes (continued)

[1] Description on IC inner operation (continued)

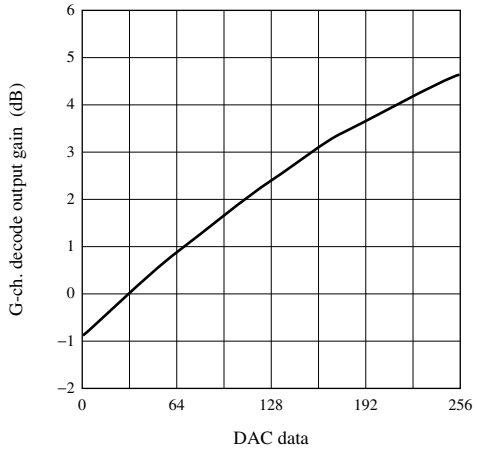
1. Operation of each block (continued)

1) Brightness signal processing block (continued)

(4) Y gain adjustment circuit

The circuit is meant to adjust a brightness signal level. Aperture level automatically varies as it is connected to the post stage of aperture circuit. In the system of inputting an analog RGB signal from outside and converting it to a video signal, adjusting amplitude on the video signal side enables you to coordinate each RGB drive output amplitude. It can be controlled by DAC ch.4.

Y gain control characteristics

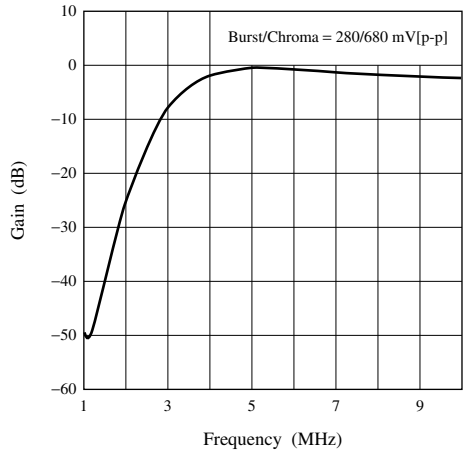


2) Chrominance signal processing block

(1) Chrominance signal input (HPF) block

Apply input onto pin 51 either in composite or component video signal so as to reject brightness signal element via HPF circuit.

Chrominance HPF characteristics



■ Application Notes (continued)

[1] Description on IC inner operation (continued)

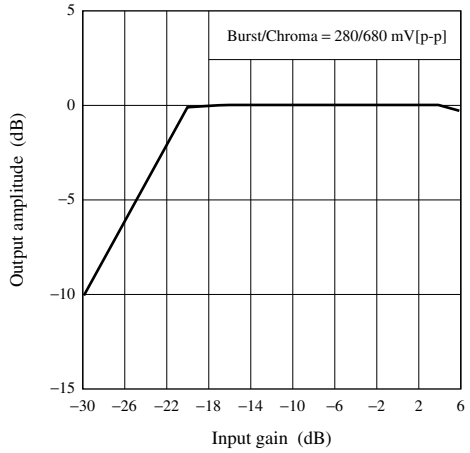
1. Operation of each block (continued)

2) Chrominance signal processing block (continued)

(2) ACC circuit

This circuit is meant to adjust automatically the chrominance signal level attenuated due to HPF and stabilize its modulated level. Connect a capacitor of approx. 0.1 µF to pin 50 as a loop filter of feedback loop.

ACC characteristics



(3) Killer circuit (PAL line discriminating circuit)

In the chrominance signal burst period, the circuit detects a burst signal synchronously and turns off the demodulation circuit in a weak electric field so as to prevent color S/N from dropping. Connect a capacitor of approx. 0.1 µF to pin 53 as a killer filter. It is possible to adjust a killer level by connecting a resistor between pin 53 and the power source or GND. Since a burst signal varies 90 degrees by 1H in PAL, it is necessary to discriminate the line of demodulation carrier and change over the demodulation carrier. A killer circuit, which executes a synchronizing detection to a burst signal, makes the same movement as a killer mode when the lines are not right. In AN2526NFH, the line discrimination is done by use of this characteristic and, therefore, it is likely to disable you to make line discrimination when you adjust a killer level by the resistor connected to pin 53. In this respect, an adequate study is required to specify the connecting constant in PAL.

Killer level : −38 dB NTSC

: −42 dB PAL

Measuring condition: burst/chrominance = 280 mV[p-p]/680 mV[p-p], no resistor connected to pin 53

(4) APC circuit

This circuit constitutes PLL to the burst signal of input chrominance signal and defines a modulation axis. VXO is constructed by connecting a crystal oscillator between pin 55 and pin 56. Connect a PLL loop filter to pin 54.

	NTSC	PAL
Lock range +	+590 Hz	+620 Hz
Pull-in range +	+590 Hz	+620 Hz
Pull-in range −	−1.2 kHz	−1.3 kHz
Lock range −	−1.2 kHz	−1.3 kHz

<Measurement condition> Crystal oscillator: NX1255GB

Series capacitor: 33 pF (NTSC) / 22 pF (PAL)

■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

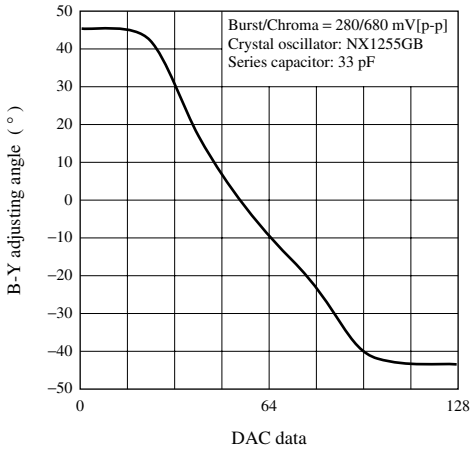
2) Chrominance signal processing block (continued)

(5) Tint adjustment circuit (NTSC)

By connecting a vector adder between tint adjustment circuit VXO and APC phase comparator, make a phase shift to change a demodulation axis. Since R-Y axis is switched for 90 degrees every 1H in PAL, tint adjustment function is only for NTSC.

Tint control channel: ch.6

TINT characteristics



(6) Chrominance signal demodulation circuit

Carry out demodulation detection for chrominance signal with a demodulation carrier determined by APC circuit and take out a color difference signal. In this time, R-Y and B-Y signals are output from pin 61 and pin 62, respectively. In an STD_PAL mode, these signals are input again to pin 63 and pin 64 via external 1H delay line and adder, respectively.

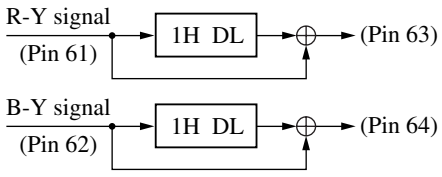
Color difference signal standard output level (at 75% white color bar signal)

R-Y signal: 280 mV[p-p]

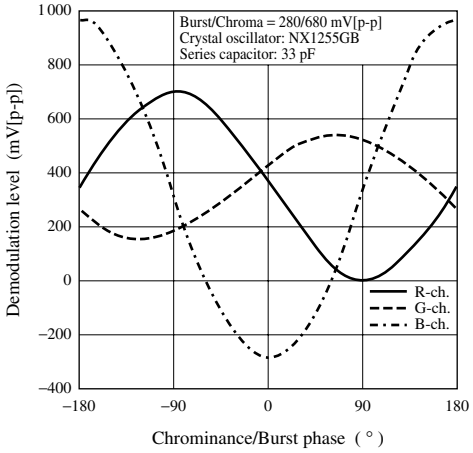
B-Y signal: 360 mV[p-p]

Demodulation angle: 90 degrees (NTSC/PAL)

STD_PAL mode connection model



Chrominance demodulation characteristics



■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

2) Chrominance signal processing block (continued)

(7) Color adjustment circuit

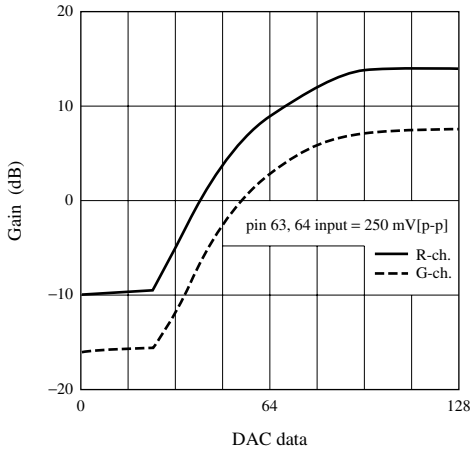
Carry out a level adjustment of color difference signal in the gain control circuit to make a color saturation level variable. Select control signal to color adjustment circuit with a serial data.

Color adjustment control channel: ch.5

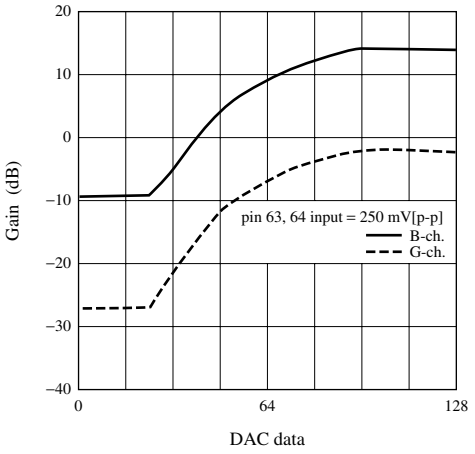
Chrominance/color difference changeover: ch.1 (D6)

Q_PAL (NTSC)/STD_PAL changeover: ch.2 (D7)

Color difference GCA control characteristics 1



Color difference GCA control characteristics 2



(8) Matrix circuit

By generating G-Y signal from R-Y/B-Y signals and adding it to brightness signal, the primary RGB color signal is generated. The generated RGB signal clamps its H-sync part with the clamp circuit and is output from pin 6, pin 7 and pin 8 after DC voltage is stabilized.

Output amplitude varies depending on Y-GCA circuit, but its standard set-up values are as follows:

Output DC voltage (pedestal block): 2.0 V

Brightness signal input/output gain: 2.5 dB

Color bar standard output amplitude: 0.54 V[p-p]

Brightness signal systems delay time: 376 ns with trap filter

270 ns without trap filter

Chrominance signal processing systems delay time: 270 ns ACC circuit passing

■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

3) Driver signal processing block

(1) Driver signal input block

The signals input into a driver block come in the following three modes:

(i) Inner decode signal

Standard setting mode

(ii) Analog RGB input 1 (car navigation system input)

Ch.1 D5 = "1"

Pin 9, pin 10, pin 11 input signal

(iii) Analog RGB input 2 (analog OSD mode)

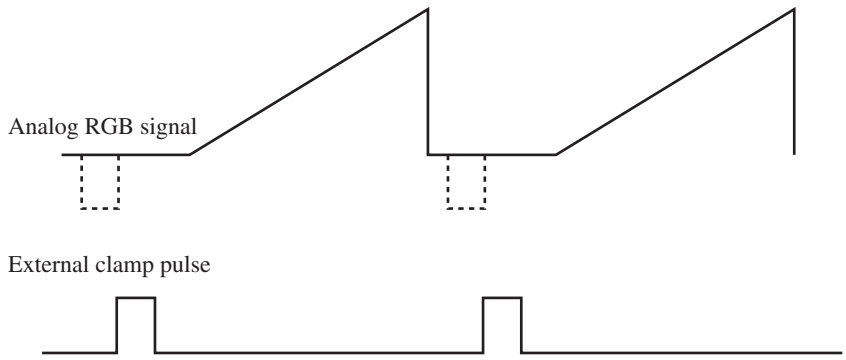
Ch.3 D7 = "0" and pin 42 = high

Pin 12, pin 13, pin 14 input signal

Analog RGB signal is clamped at its input block to secure the same potential as inner decode signal. In this time, with a clamp circuit at the input block an RGB signal should be input in capacitive coupling mode. The RGB signal to be input into AN2526/AN2526NFH is based on a flat waveform in its pedestal part and, therefore, once any difference in level is found, it is necessary to input a clamp pulse from outside to make it possible to clamp during a flat period.

External clamp pulse input mode: ch.6 D7 = "0"

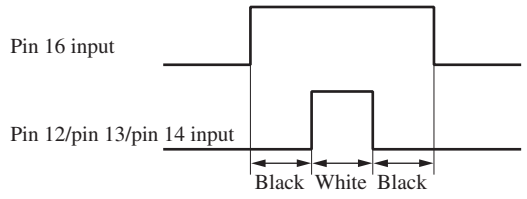
External clamp pulse input pin: pin 38



(2) Character insertion (OSD) circuit

For character insertion signal, it is able to select either digital (8 colors) mode or analog (full color) mode based on a binary signal. Analog mode is just as mentioned previously and, in the digital mode, a white level control pulse is input from OSD input pin and a black level one from pin 16. A black level signal is controlled commonly with RGB and a white level signal has priority over a black level signal. It is recommended, therefore, to input in the following timing:

Input sideblack signal to pin 15 to realize a display of 4:3 aspect ratio on a wide panel.



OSD control signal threshold voltage = 1.5 V (common to pin 12, pin 13, pin 14, pin 15, pin 16)

OSD black level = pedestal

OSD white level = adjusted with white limiter

■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

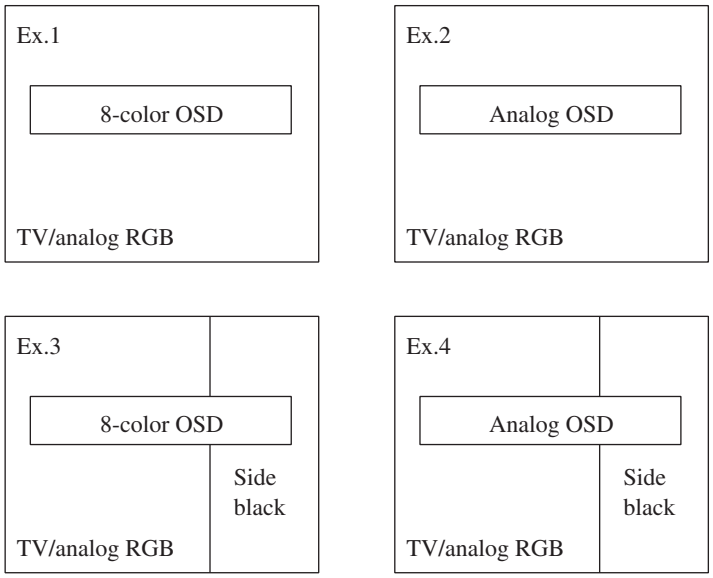
3) Driver signal processing block (continued)

(2) Character insertion (OSD) circuit (continued)

Display priority is as follows:

Video < OSD black < OSD white < Blanking

Displayable modes on the OSD are as follows:

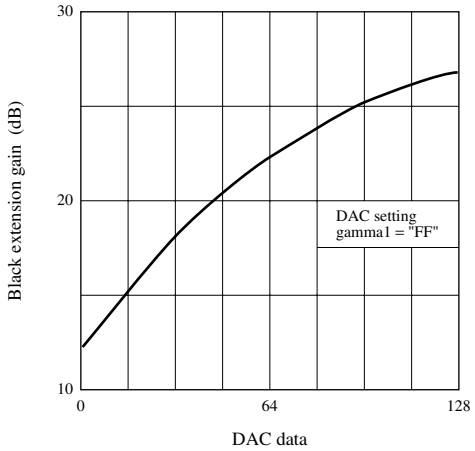


(3) Contrast adjustment circuit

The circuit is meant for contrast adjustment of RGB signal.

Contrast control channel: ch.15

Black extension gain control characteristics



■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

3) Driver signal processing block (continued)

(4) Brightness/sub-brightness adjusting circuit

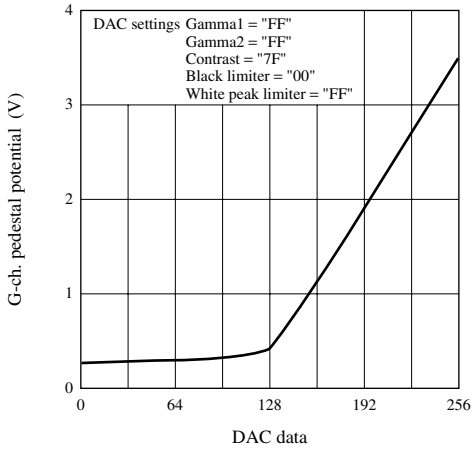
This circuit functions as pedestal potential adjustment of RGB drive output. Since there are independent control channels for R-ch. and B-ch., respectively for sub-brightness adjustment, match R-ch. and B-ch. to G-ch. output.

Brightness control channel: ch.8

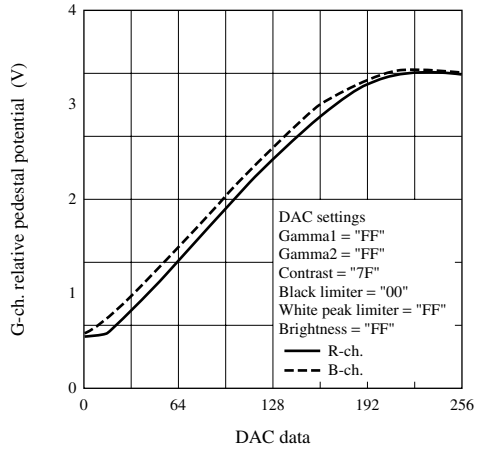
R-ch. sub-brightness control channel: ch.10

B-ch. sub-brightness control channel: ch.11

Brightness control characteristics



Sub-brightness control characteristics

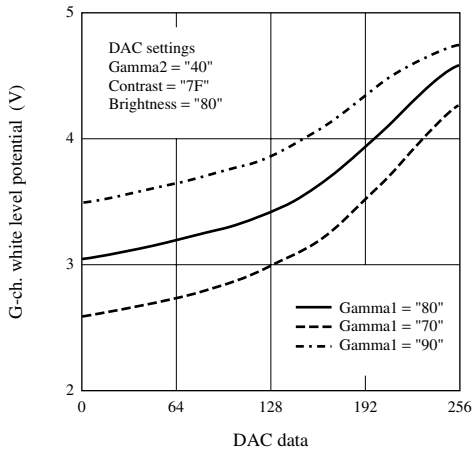


(5) White peak limiter circuit

Since application of higher voltage than common voltage to liquid crystal panel causes brightness to be inverted, limitation is imposed on the white side. Meanwhile, OSD white level system is based on optimization by white limiter circuit. Therefore, never fail to set it to the optimal value.

White limiter level control channel: ch.12

White peak limiter control characteristics



■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

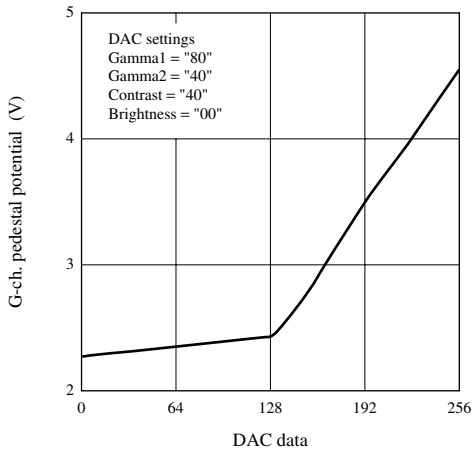
3) Driver signal processing block (continued)

(6) Black limiter circuit

Since AN2526/AN2526NFH is based on 5 V source driver panel, GND-side operating range is notably small to standard pedestal potential. If brightness adjustment is done in this state, an output transistor in the RGB driver output circuit is likely to enter a saturating region. To prevent it, a black limiter level is set.

Black limiter level control channel: ch.7

Black limiter control characteristics



(7) Gamma circuit

When applying voltage to LCD, the relationship between voltage and transmittivity is displayed not by linearity but an enlarged contrast ratio and the driver output signal is displayed in a line graph characteristic for correction.

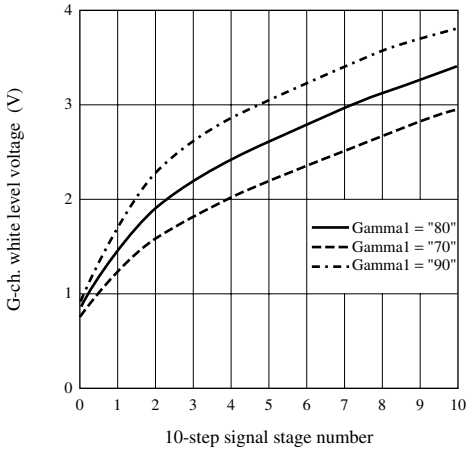
There are two Knee points on both black and white sides. Each of the points should be adjusted independently. Since gamma circuit is in the post stage of contrast and brightness circuits, the Knee point to the panel remains unchanged even if you make contrast and brightness adjustment.

Black side (gamma 1) Knee point control channel: ch.13

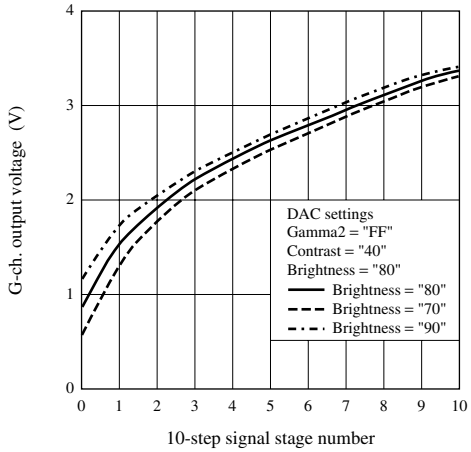
White side (gamma 2) Knee point control channel: ch.14

Precaution on gamma Knee setting value should be taken to prevent it from interfering with pedestal potential.

Gamma1 control characteristics



Brightness control characteristics



■ Application Notes (continued)

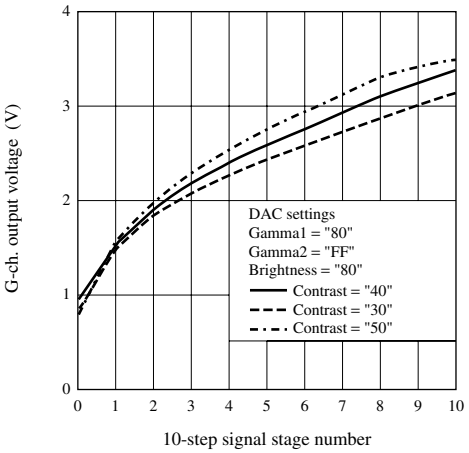
[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

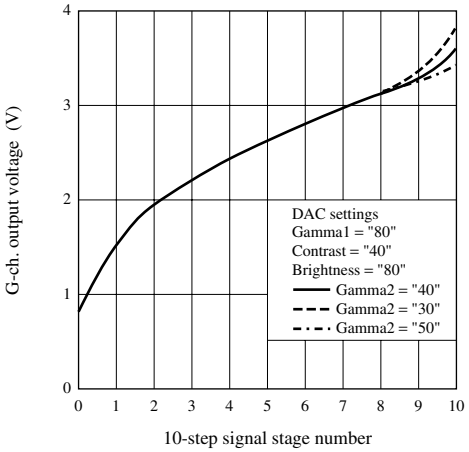
3) Driver signal processing block (continued)

(7) Gamma circuit (continued)

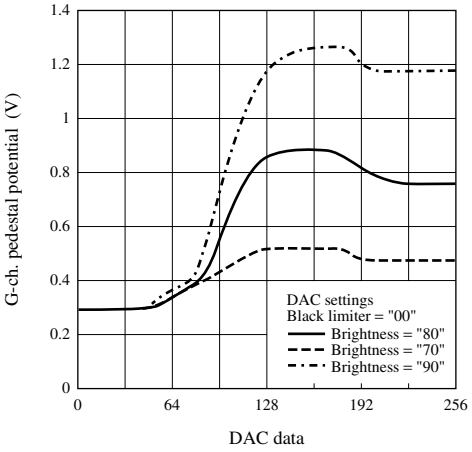
Contrast control characteristics



Gamma2 control characteristics



Gamma1 — Dependence-on-pedestal characteristics



(8) RGB driver output circuit

The circuit generates LCD driver signal. To prevent screen persistence on LCD displays, it switches the polarity of voltage applied to LCD between the fields. And it outputs polarity inversion every 1H to counter the flickers. Polarity inverting pulse can be taken from either external source or internal generation. But, in the system of inverting common polarity of LCD, it is recommended that you take an external input mode to facilitate polarity matching with RGB output. Meanwhile, in the system where RGB output is not inverted, inversion disable mode is built in and RGB output is in a forward mode.

DC operating points on RGB output signals converts each output signal into DC voltage via integration circuit and automatically adjusts it by a feedback loop.

Preset voltage is 1/2 V_{CC1}, but it is possible to adjust it due to pin 21 applied voltage. However, input the pin 21 voltage so as not to exceed V_{CC1} voltage.

Also, connect a capacitor as a loop filter (integration circuit) of feedback filter. Connecting constant differs according to the status of display signal, but 2.2 µF to 10 µF is expected.

■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

3) Driver signal processing block (continued)

(8) RGB driver output circuit (continued)

5 V source driver panel is characteristic of A-class output in its output mode because operating range to GND is very small (approx. 0.7 V) in the system not using a negative power source. In this respect, therefore, adequate study should be made to load capacitance and operating frequency. Also full care should be taken to PWB design to achieve a wider bandwidth.

RGB reverse pulse input mode switching: ch.15 (D7)

RGB reverse disable mode: ch.15 (D7)

RGB output DC voltage (1H reverse mode): 1/2 V_{CC1} ± 0.2 (V)

Pin 21 control sensitivity: 1 V/V

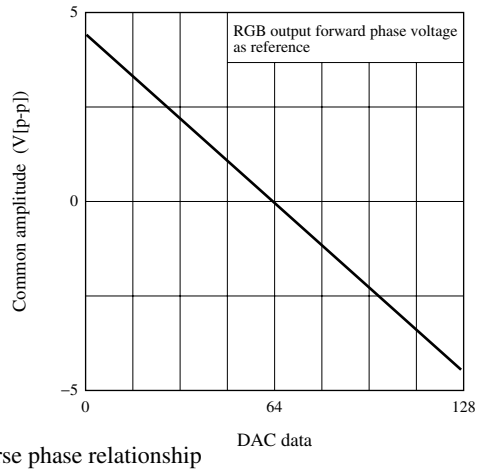
(9) Common pulse generating circuit

The circuit generates a voltage for common electrodes of LCD panel. It output signal comes in a pulse in sync with RGB output reverse pulse. Pulsed signal amplitude can be adjusted by DAC, but its DC voltage is fixed and must be optimized by the external circuit. And the standard output amplitude is 2 V[p-p] and gain deficiency must be made up by the external fixed amp (Gain: 3-fold).

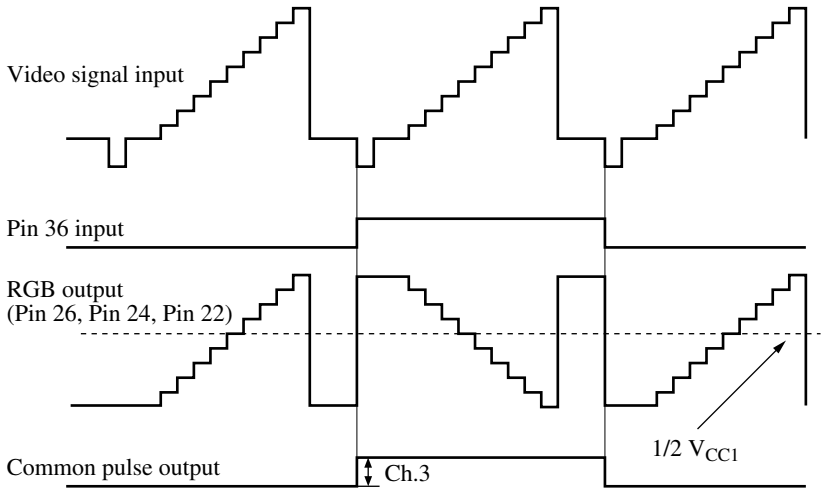
Note that common pulse control is not linked with RGB output signal.

Common pulse control channel: ch.3

Common control characteristics



1H reverse phase relationship



■ Application Notes (continued)

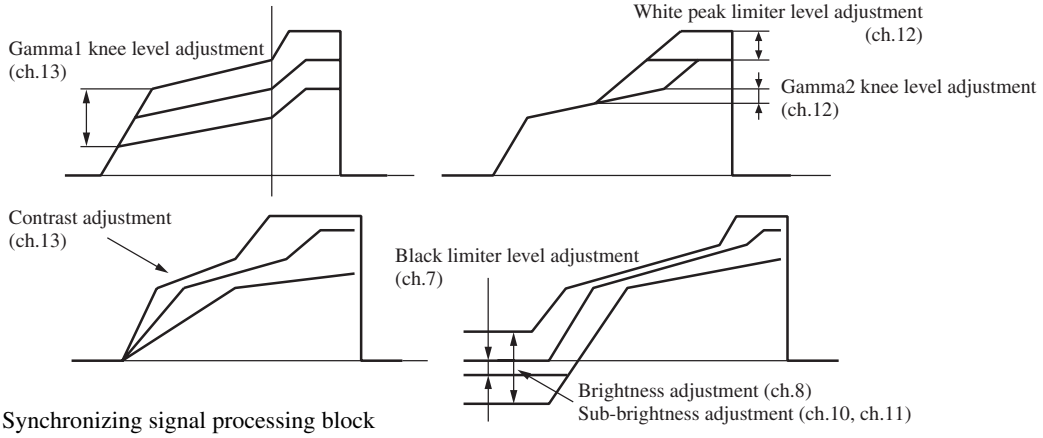
[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

3) Driver signal processing block (continued)

(9) Common pulse generating circuit (continued)

Driver block control characteristics



4) Synchronizing signal processing block

(1) Reset circuit

In power activation, this circuit with a capacitor connected to pin 34 generates reset pulse using a rise-up transient characteristic to reset initially a logic circuit and boost lead-in response characteristic of vertical synchronizing signal.

(2) Synchronizing separation circuit

Taking out composite synchronizing signal from video signal inputted from pin 45, this circuit carries out PLL for horizontal system and count-down processing for vertical system. There will be no problem even if this signal is used when synchronizing signal processing is performed with a timing controller IC.

To prevent synchronizing separation circuit from making operation error due to the chrominance signal (burst signal) contained in composite video signal, LPF is connected to the input block so that high frequency element may be reduced. This LPF is effective to stabilize a horizontal PLL to noise element in a weak field mode. It is recommended to assess weak electric field and set up the constant.

Synchronizing separation performance: −10 dB or more
Composite synchronizing signal output amplitude: 5 V[p-p]
Composite synchronizing signal output pin impedance: 100 Ω or less

(3) Horizontal PLL circuit

VCO frequency phase is locked to the horizontal synchronizing signal separated by synchronizing separation circuit. VCO free-run frequency is determined by resistance value connected to pin 44. VCO free-run frequency designed value (pin 44-connected resistor = 10 kΩ) is 10.92 MHz and the basic clock of the inner counter is the VCO free-run frequency divided by two. In other words, PLL is constructed so as to match the basic clock frequency divided by 347 (NTSC/PAL) to the input frequency. In the case that a synchronizing signal is without signal, the circuit detects no input signal and output HD pulse from pin 32 by dividing the VCO free-run frequency. Setting 384fy (NTSC/PAL) as decode value, detection of no signal input is done in such manner that it is judged as no signal input when synchronizing signal is not inputted up to this decode value.

Since input synchronizing signal and HD pulse phase are made variable due to serial control, this function enables you to adjust display position of OSD.

NTSC: f_{CK} = 5.46 MHz, 1fy = 183 ns
PAL: f_{CK} = 5.42 MHz, 1fy = 184 ns
HD pulse position control channel: ch.1
HD pulse free-run output cycle: 347fy
HD pulse output amplitude: 5 V[p-p], negative polarity
HD pulse width: 32fy
HD pulse position adjustment variable width: 31fy

Refer to the paragraph of serial control for the relationship between the input signal and the HD pulse output phase.

■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

4) Synchronizing signal processing block (continued)

(4) Vertical countdown circuit

This circuit counts horizontal synchronizing signal and outputs horizontal synchronizing signal (HD pulse) divided by 263 or by 265 (by 313 or by 315 for PAL) in case of the omission or no signal of the vertical synchronizing signal. A masking period of vertical synchronizing signal is approximately 95% (NTSC: 247H, PAL: 294H) and then becomes in a standby mode. Like VCR rev mode, its detecting circuit changes countdown decode value to the increase of horizontal synchronizing signal during one vertical synchronizing period (NTSC: 282H, PAL: 334H), so as to output according to the input vertical synchronizing signal.

Vertical synchronizing signal input into pin 35 is extracted from the composite synchronizing signal outputted to pin 34 via an external filter. The constant of filter can be set by evaluating vertical synchronizing stability in a weak electric field on the set.

Since equalizing pulse is inserted into the composite synchronizing signal during vertical synchronizing period, operation error occurs on the horizontal PLL due to synchronizing separation circuit. Though it is necessary to free PLL during this period, if the freed period is too long, top curl phenomenon appears on the upper part of screen. The re-start position of PLL can be controlled serially and its proper value can be determined after evaluation of characteristics of the weak electric field.

LCD equipment is characteristic of interlace display and, to display TV signal of interlace display on LCD, display line numbers between fields must be determined. VD output phase relationship of ODD/EVEN field can be selected by serial control.

VD pulse output position adjustment control channel: ch.0

VD pulse ODD/EVEN phase selection: ch.0 (D7)

VD pulse free-run output cycle: NTSC = 263H, PAL = 313H

VD pulse output amplitude: 5 V[p-p], negative polarity

VD pulse width: 8H (9H only at ch.0: D2, D1, D0 = 0, 0, 0)

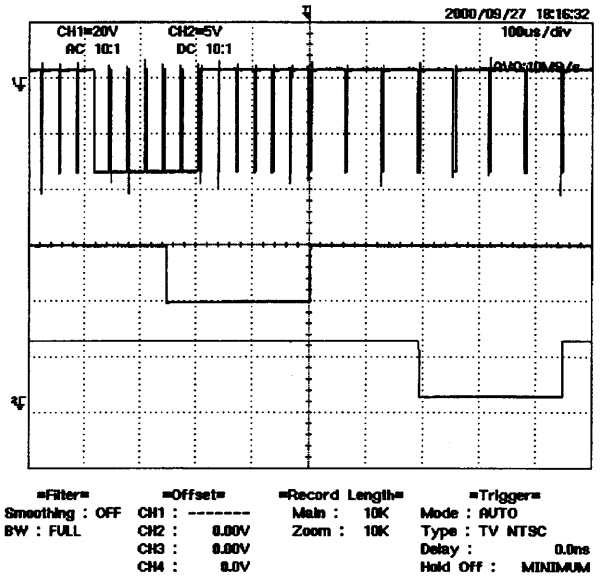
VD pulse output position adjustment range: 2H to 9H

PLL stop position control channel: ch.0

PLL stop position variable range: 6H to 9H

PLL open line: 254 lines (NTSC), 302 lines (PAL)

Refer to the paragraph of serial control for the relationship between the input signal and VD pulse output phase.



VD position adjustment

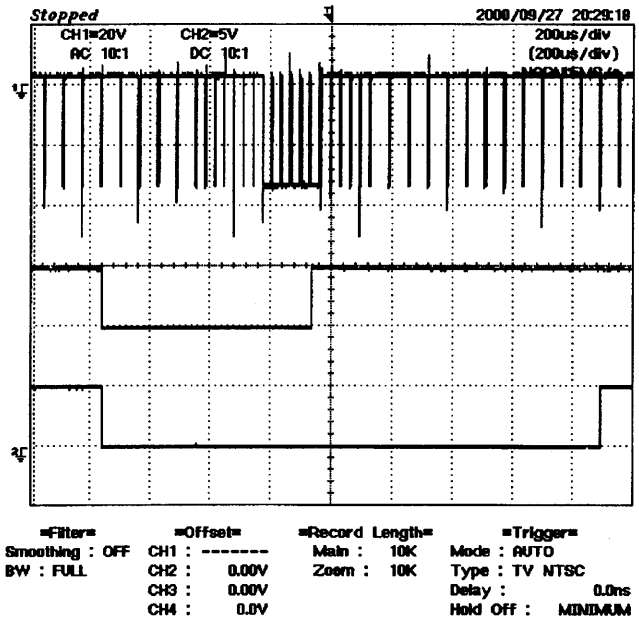
■ Application Notes (continued)

[1] Description on IC inner operation (continued)

1. Operation of each block (continued)

4) Synchronizing signal processing block (continued)

(4) Vertical countdown circuit (continued)



Input signal

Minimum setting

Maximum setting

PLL stop position adjustment

(5) PWM pulse output circuit

The circuit generates PWM control pulse for backlight control.

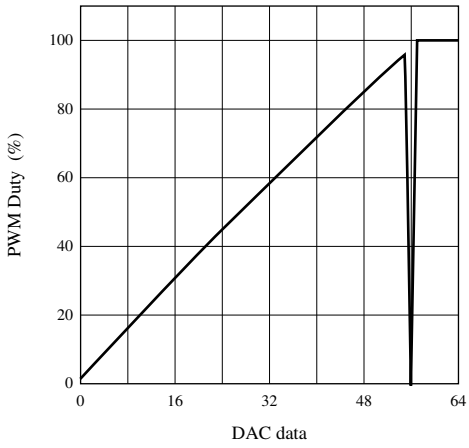
Duty control channel: ch.2

Duty variable range: 0% to 100%

Basic frequency: $64f_h$, common for both NTSC and PAL

PWM output pulse amplitude: 5 V[p-p]

PWM Duty control characteristics



■ Application Notes (continued)

[1] Description on IC inner operation (continued)

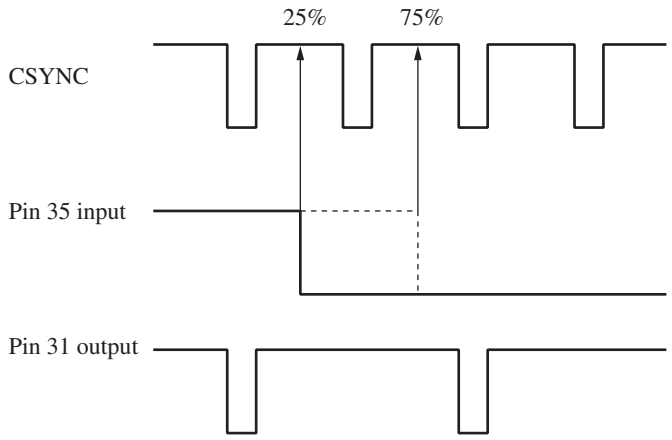
1. Operation of each block (continued)

4) Synchronizing signal processing block (continued)

(6) Precautions on VD input timing

In AN2526/AN2526NFH, VD input is pulled inside at the half edge of CSYNC. If VD rise-up and half edge becomes same in the waveform timing, pull-in comes in two ways due to a subtle timing.

Therefore, set the filter constant between pin 30 and pin 35 so as to make pin 35 input pulse fall to 25% or 75% of CSYNC 1H.



2. I^2C bus control

Philips developed a simple bi-directional 2-wire bus for efficient inter-IC control.

This bus is called the Inter IC or I^2C-bus.

- Features of I^2C bus

(1) Being constructed by only two bus lines of a serial data line (SDA) and a serial clock line (SCL), transfer is done by 9-bit unit of 8-bit transfer data and 1-bit response data. (bi-directional serial data transfer)

(2) Each device connected to the bus has the unique address which enables to specify the address of each device with software.

(3) The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

Note that this evaluation kit is applicable to 3-line serial control. If you need I^2C bus control, you can add an open drain like DN74LS03 to pin 47 and pin 48.

For actual system design, refer to the I^2C bus specification of Philips Semiconductors.

3. 3-line serial control

This is 3-line system of transmitting independently three kinds of signal of SCLK: pin 47, SDATA: pin 48, LD: pin 49.

The data to be transmitted is made up by 12 bits in total of address (4 bits) and data (8 bits).

Switching to I^2C bus control and 3-line serial control can be done by the voltage to be applied to pin 46.

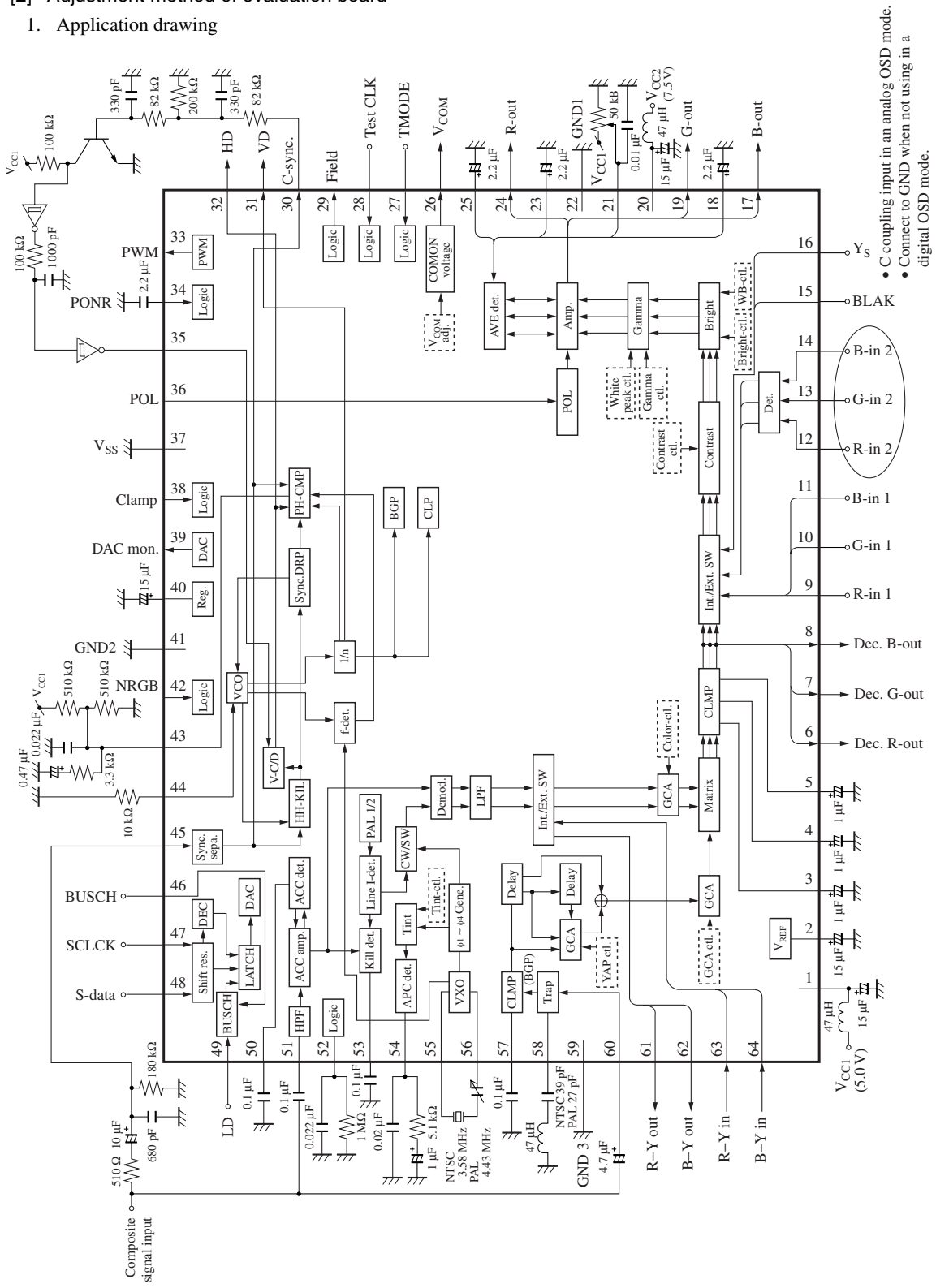
3-line control mode: pin 46 = low (connected to GND)

I^2C bus control mode: pin 46 = high (connected to 5 V)

■ Application Notes (continued)

[2] Adjustment method of evaluation board

1. Application drawing



■ Application Notes (continued)

[2] Adjustment method of evaluation board (continued)

2. Quick start guide

1) I²C bus software installation

Install all ten files of a floppy disc packed herewith into the holder of a personal computer.
an2526evr.exe: execution file
Data 1.evr to Data9.evr: Files for storing a setup data

2) Connection of a personal computer to an evaluation kit

Connect one end of printer cable to the parallel port of personal computer and other end to an evaluation kit.

3) Evaluation kit startup

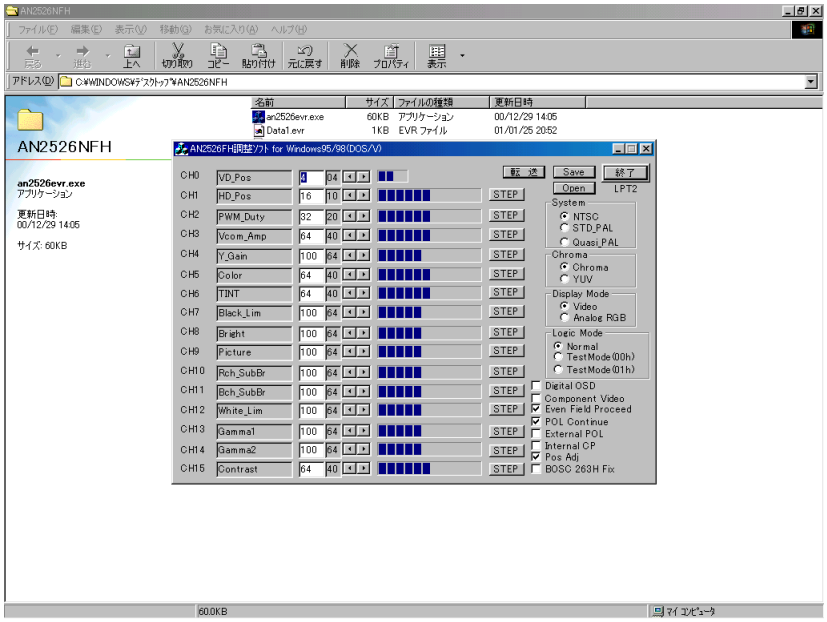
(1) Connect a power cord to the source.

Black banana clip → GND
Red banana clip → +5 V
White banana clip → +7.5 V

(2) Since an evaluation board normally corresponds to CPS (composite signal input), connect the video signal (standard white signal, 1 V[p-p]) to BNC connector on the evaluation board.

(3) Rise up the adjustment software according to the following paragraph of 4) "I²C bus software startup".

4) I²C bus software startup



(1) Double-click the an2526evr.exe file.

(2) The screen of "AN2526NFH adjustment software for Windows95/98 (DOS/V) comes up. (Adjustment screen)

(3) Move the pointer to your desired item on the screen with the mouse and click the button for setting.

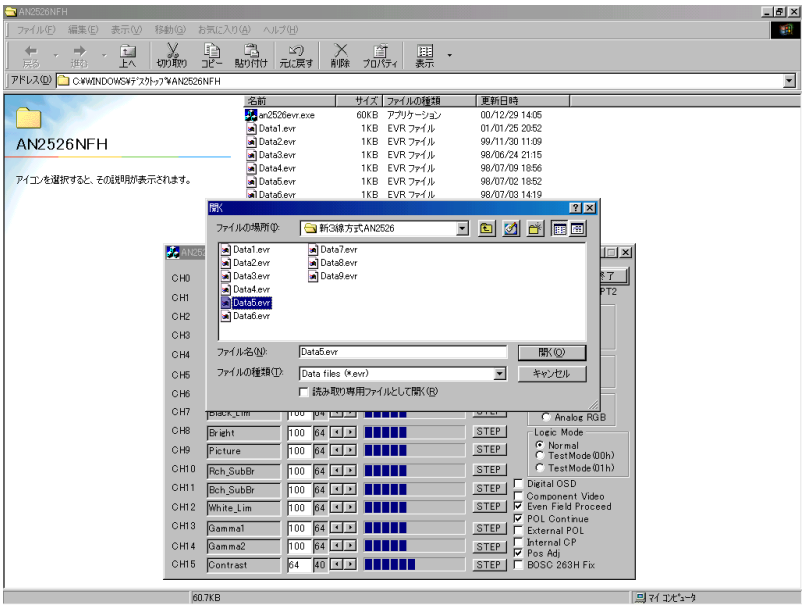
(4) Press the "Save" button when you want to save the setup status.

■ Application Notes (continued)

[2] Adjustment method of evaluation board (continued)

2. Quick start guide (continued)

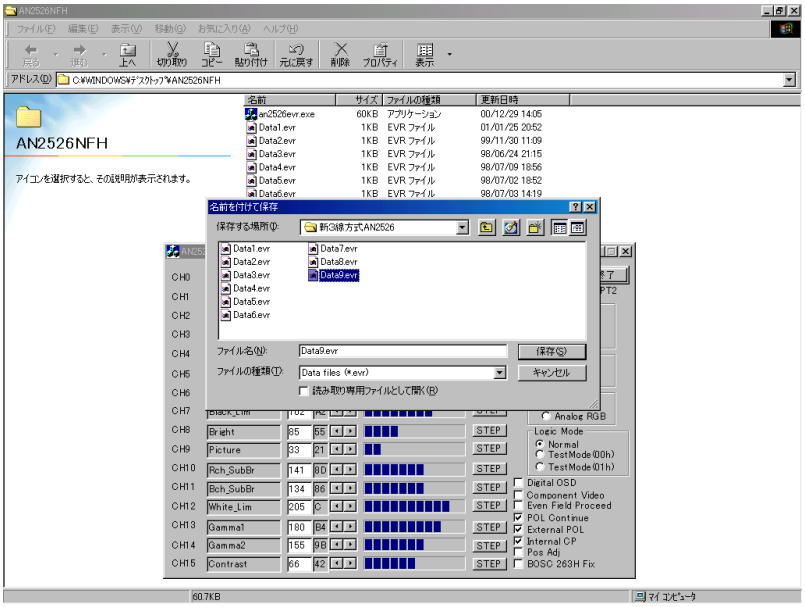
4) I²C bus software startup (continued)



(5) The window <Data1.evr to Data9.evr> comes up on the screen and click the button of Open (O) after choosing your desired data so that you can store its setting status there. (The example shown above is for saving Data5.evr.)

(6) To call up the already saved setting status, click the "Open" button to fetch the window for selecting from Data1.evr. to Data9.evr. Select the data saving file where your desired setting is saved and click the button of Open (O).

(7) When you want to select NTSC/STD_PAL/Quasi_PAL, the necessary mode is likely to be not chosen even if you call up the saved files. Check it again and select your desired mode.



■ Application Notes (continued)

[2] Adjustment method of evaluation board (continued)

2. Quick start guide (continued)

5) RGB waveform adjustment step

Initial setting condition

NTSC, video input mode

DAC initial settings

Y gain	40
Color	40
Hue	40
Black limiter	00
Brightness	80
Y aperture	40
R-ch. sub-contrast	80
B-ch. sub-contrast	80
White peak limiter	FF
Gamma1	80
Gamma2	40
Contrast	40

RGB output adjustment value:

Forward side pedestal to reverse side pedestal = 2.5 V

Forward side white level to reverse side white level = 2.5 V

(1) Black limiter adjustment

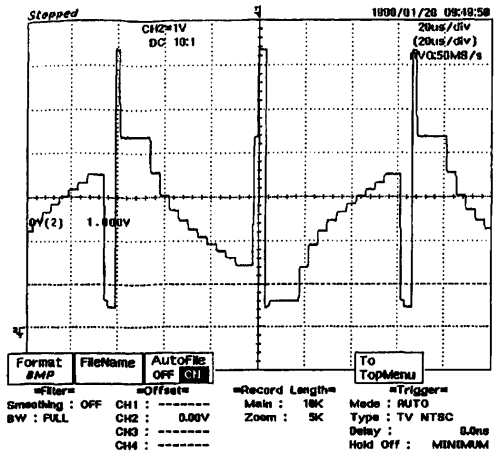
Adjust pin 19 (G-ch.) output signal black limiter level (forward side pedestal potential)

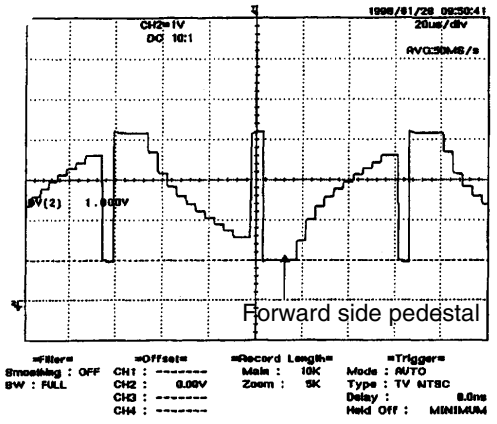
DAC: ch.7

Adjustment range: 00 (hex) to FF (hex)

Adjustment precision: 1 V ± 50 mV

Reference data value: A0 (hex)





(2) White peak limiter adjustment

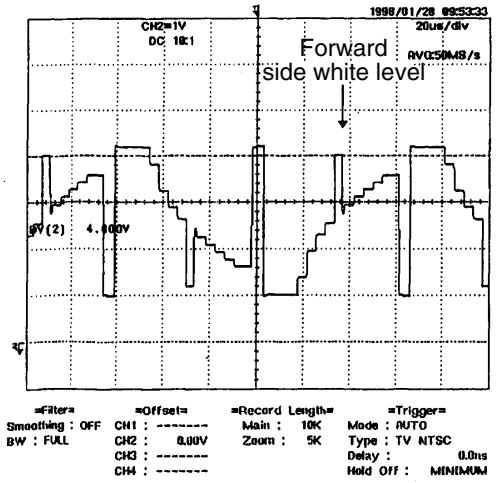
Input OSD pulse to pin 13 and adjust white limiter level of pin 19 forward side output signal.

DAC: ch.12

Adjustment range: 00 (hex) to FF (hex)

Adjustment precision: 4 V ± 50 mV

Reference data value: BA (hex)



■ Application Notes (continued)

[2] Adjustment method of evaluation board (continued)

2. Quick start guide (continued)

5) RGB waveform adjustment step (continued)

(3) Y gain adjustment

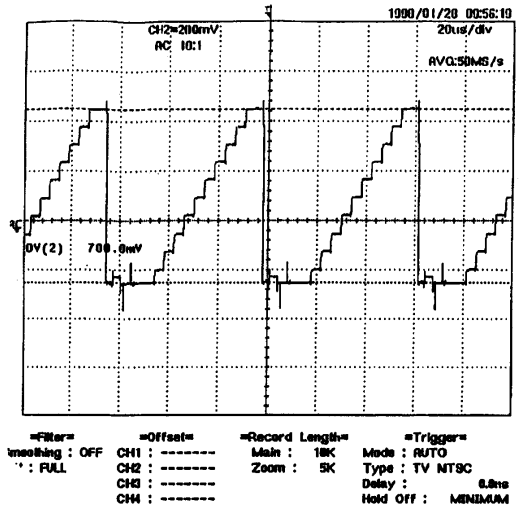
Adjust amplitude of pin 7 (G-ch. decode output)

DAC: ch.4

Adjustment range: 00 (hex) to FF (hex)

Adjustment precision: 700 mV ± 5 mV

Reference data value: 15 (hex)



(4) Brightness (pedestal) adjustment

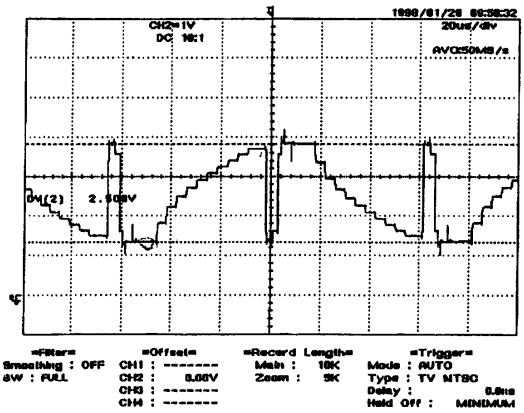
Adjust amplitude (forward side pedestal to reverse side pedestal) of pin 19 (G-ch.) output signal.

DAC: ch.8

Adjustment range: 00 (hex) to FF (hex)

Adjustment precision: 2.5 V ± 50 mV

Reference data value: 93 (hex)



(5) Contrast/gamma adjustment

Change an input signal to Ramp waveform and adjust contrast/gamma Knee point of pin 19 (G-ch.) output.

- Contrast

DAC: ch.15

Adjustment precision: 2.5 V ± 50 mV

Reference data value: 3C (hex)

- Gamma1

DAC: ch.13

Adjustment precision: 00 (hex) to FF (hex)

Reference data value: 80 (hex)

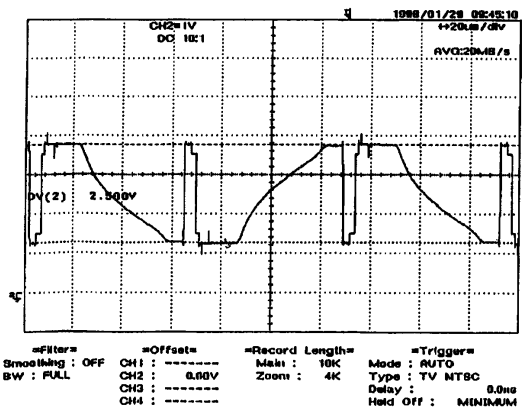
- Gamma2

DAC: ch.14

Adjustment precision: 00 (hex) to FF (hex)

Reference data value: 2C (hex)

Use it so as not to cause any affect on pedestal potential.



■ Application Notes (continued)

[2] Adjustment method of evaluation board (continued)

2. Quick start guide (continued)

5) RGB waveform adjustment step

(6) R-ch. sub-brightness adjustment

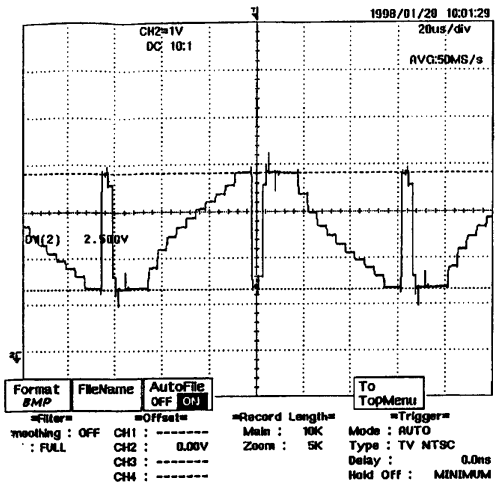
Change an input to 10-step waveform and adjust amplitude (forward side pedestal to reverse side pedestal) of pin 24 (R-ch.) output signal.

DAC: ch.10

Adjustment range: 00 (hex) to FF (hex)

Adjustment precision: 2.5 V ± 50 mV

Reference data value: 8A (hex)



(7) B-ch. sub-brightness adjustment

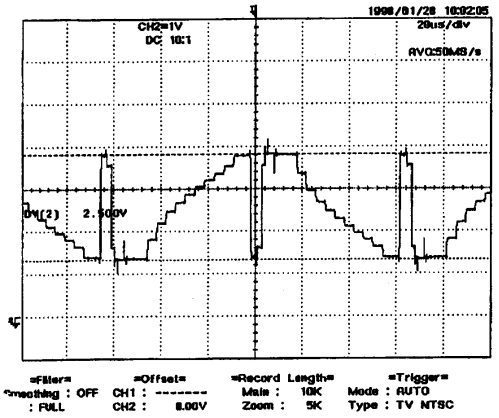
Adjust amplitude (forward side pedestal to reverse side pedestal) of pin 17 (B-ch.) output signal.

DAC: ch.11

Adjustment range: 00 (hex) to FF (hex)

Adjustment precision: 2.5 V ± 50 mV

Reference data value: 7C (hex)



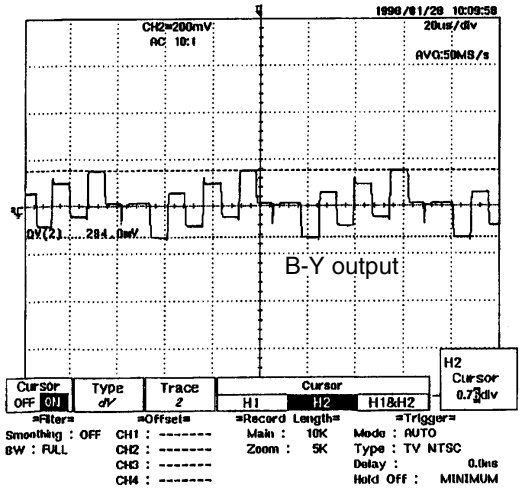
(8) Hue adjustment

Change an input signal to full color bar signal and adjust hue monitoring pin 62 (B-Y output) waveform. Adjust capacitance of a capacitor connected to a crystal oscillator in series so that hue may come in the waveform around DAC center as shown in the drawing to the right. However, full care should be taken to APC pull-in range.

DAC: ch.6

Adjustment range: 00 (hex) to FF (hex)

Reference data value: 40 (hex)



■ Application Notes (continued)

[2] Adjustment method of evaluation board (continued)

2. Quick start guide (continued)

5) RGB waveform adjustment step (continued)

(9) Color adjustment

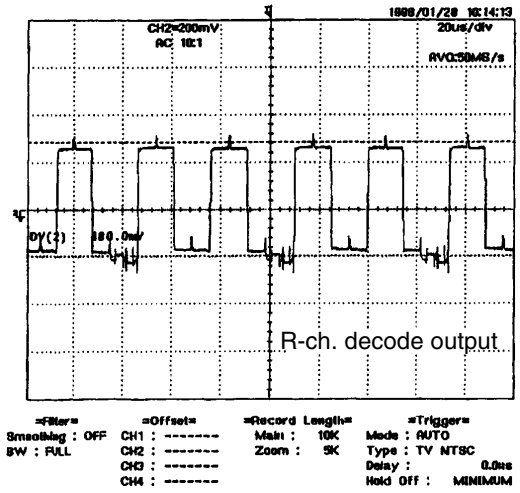
Adjust color monitoring pin 8 (B-ch. decode output) waveform.

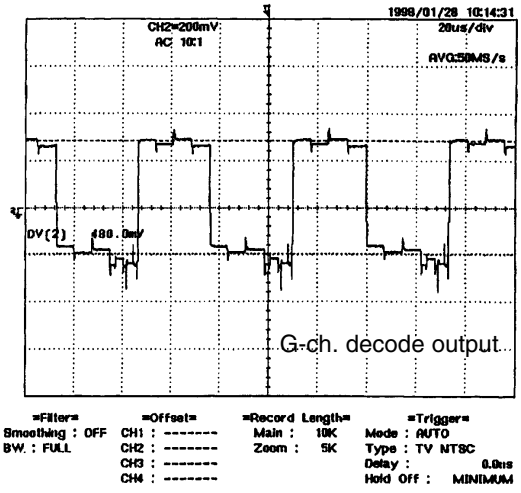
DAC: ch.5

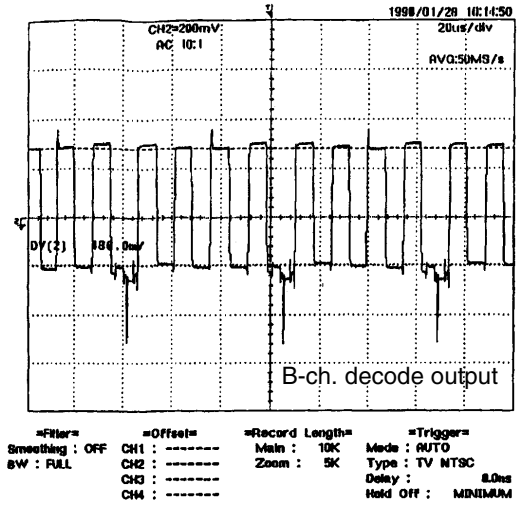
Adjustment range: 80 (hex) to FF (hex)

Adjustment precision: Adjust so each color has B/W characteristics as shown in the right drawing.

Reference data value: 37 (hex)







■ Application Notes (continued)

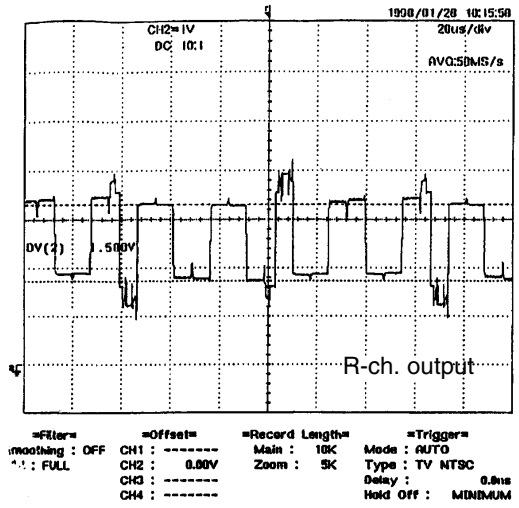
[2] Adjustment method of evaluation board (continued)

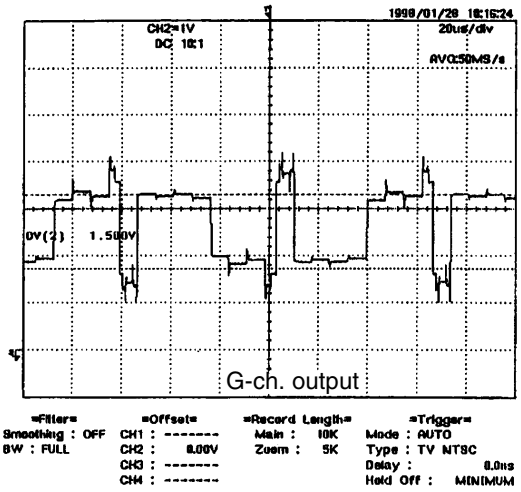
2. Quick start guide (continued)

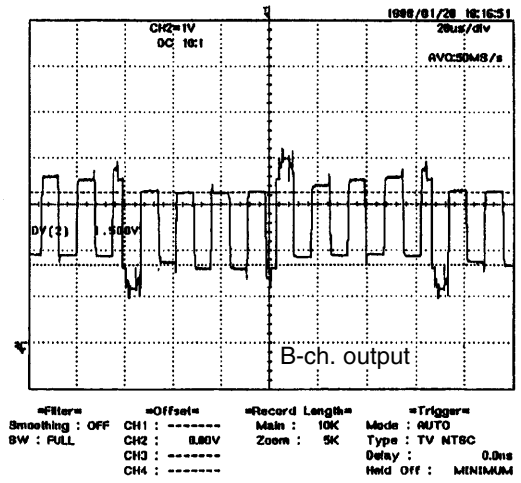
5) RGB waveform adjustment step (continued)

(10) Driver output

Check that the driver outputs (pin 17, pin 19 and pin 24) are just as shown on the drawing to the right.







6) Special parts list

Socket: Yamaichi Electronics Co., Ltd.
P/N: IC51-0844-807

Crystal oscillator:
Nihon Dempa Kogyo Co., Ltd.
P/N: NX1255GB
NTSC: 3.579545 MHz
PAL: 4.43361875 MHz

Hex Inverting Schmitt Trigger:
P/N: 74HC14

Printer cable connector (IEEE1284) between I^2C bus evaluation board and PC:
Hirose Electric Co., Ltd.
P/N: RC10-type RC10-36R-LW

Panel connector:
Japan Aviation Electronics Industry, Ltd.
P/N: IL-FPR-U30S-HF

■ Application Notes (continued)

[3] Troubleshooting

1. No RGB output waveforms come out.
   → Is plugged to source?
   → Is the specified voltage applied to the power source pin of each IC?
   → Is a socket contact in place for a socket-type evaluation kit?
   → Is an input signal ready?
   → Is it controlled by I^2C bus or 3-line serial?
   → Is brightness signal outputted to RGB output?
   → Is crystal oscillated?
   → Did you adjust capacitance inserted into crystal in serial?
2. There is a delay of color signal level by 1H in PAL mode screen.
   → Do you external 1H delay of R-Y/B-Y signal return to the IC through an adder?
   (Philips' TDA4665 is recommended as 1H delay + adder.)
   → Are you setting I^2C bus or 3-line serial to QUASI_PAL mode?
3. When inputting CPS, chroma element is superposed on RGB output.
   → Is pin 58 external Trap setting optimized?
   (L = 47 µH, C = 39 pF for NTSC → Optimize on PWB of the set.)
   (L = 47 µH, C = 27 pF for PAL → Optimize on PWB of the set.)

[4] Q & A

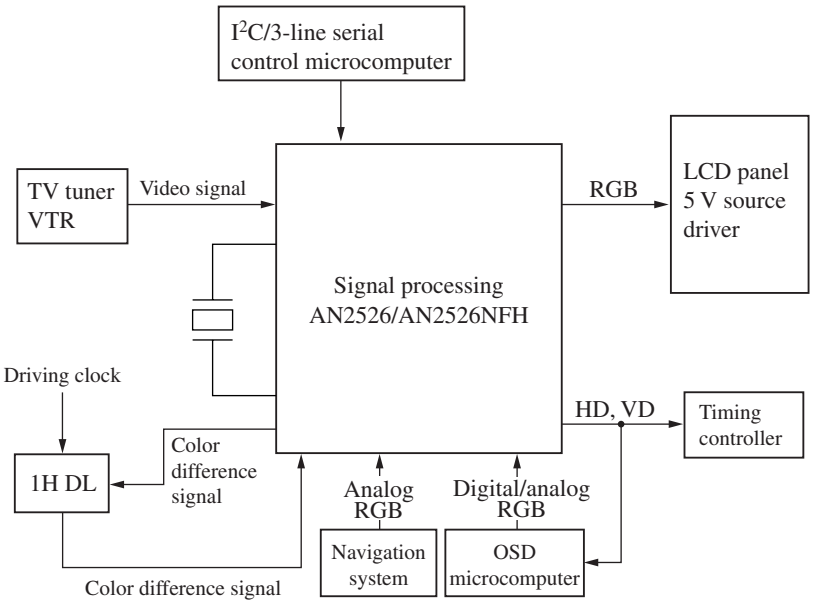
1. What broadcasting system to be corresponded?
   → NTSC/PAL
2. Capacitance attached to pin 18, pin 23 and pin 25 (R/G/B out_det) is 2.2 µF, which is fairly big. Is there no problem even in 0.22 µF?
   → It is impossible. 1H stripe pattern caused flickers.
3. Is 1 µF capacitor coupling necessary even if we don't use pin 3, pin 4 and pin 5?
   → No problem if any sagging occurs at H rate.
4. Pin 60 Y input (composite signal input) is clamped by sync tip clamp circuit prior to the input to the pin. How about DC coupling?
   → It doesn't make sense. Never fail to do capacitor coupling.
5. Is it possible to make capacitances for pin 2 V_{REF} and pin 40 smaller?
   → Possible. Make it smaller after checking that there is no occurrence of noise on video output.

■ Application Notes (continued)

[4] Q & A (continued)

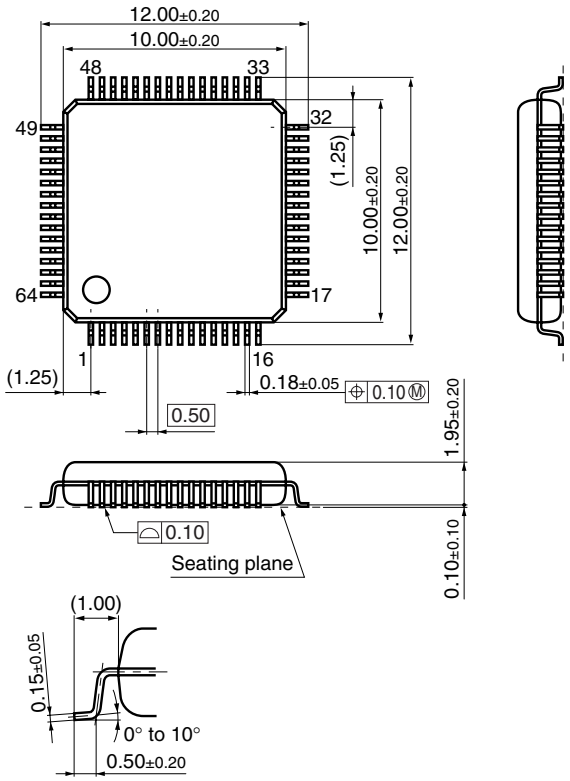
6. Is performance of H-sync separation or V-sync separation inside AN2526/AN2526NFH identical with digital separation by synchronous counter?
   (In the case that badly synchronized video signal is inputted, it often caused no function in digital separation.)
   → In the case that input signal is unstable in weak electric field, analog separation adopted in this IC would guarantee more stability.
   LPF is constructed by external constant for pin 45. V separation is done by the filters of pin 30 to pin 35.
7. How is it different between vertical sync signal input with VDBin of pin 35 and inside sync separation?
   → In AN2526/AN2526NFH, vertical sync separation is not done inside.
   The external separation gives you much resistance to noise in weak electric field of car navigation system.
8. I wonder if pin 37 MOS GND or pin 41 pulse GND is separated from analog GND inside the LSI. (I would like to know as a yardstick for outside separation of GND.)
   → It is separated inside in terms of wiring.

[5] Drawing of car navigation system



■ New Package Dimensions (Unit: mm)

• QFP064-P-1010A (Lead-free package)



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