Optical disc ICs

10bit 6-channel D/A converter

BU2507FV

BU2507FV is an IC that incorporates 10bit 6-channel D/A converter using the R-2R system. Each channel output incorporates a Rail to Rail type output with buffer amplifier. This IC utilizes the TTL level input method. RESET pin can keep the output voltage in the lower reference voltage range.

●**Applications**

DVD, CD-R, CD-RW, DVC, Digital camera, and other industrial equipments.

●**Features**

1) High-performance 10bit 6-channel D/A converter adopting the R-2R system.
2) Power supply voltage : 4.5~5.5V.
3) Each channel output incorporates a Rail to Rail type output with buffer amplifier.
4) RESET pin can keep output voltage of all channels within the lower reference voltage range.
5) Digital input compatible with TTL levels.
6) 10MHz input frequency.
7) 14bit 3wire serial data + RESET signal input. (4bit address + 10bit data)

●**Absolute maximum ratings** (Ta=25°C)

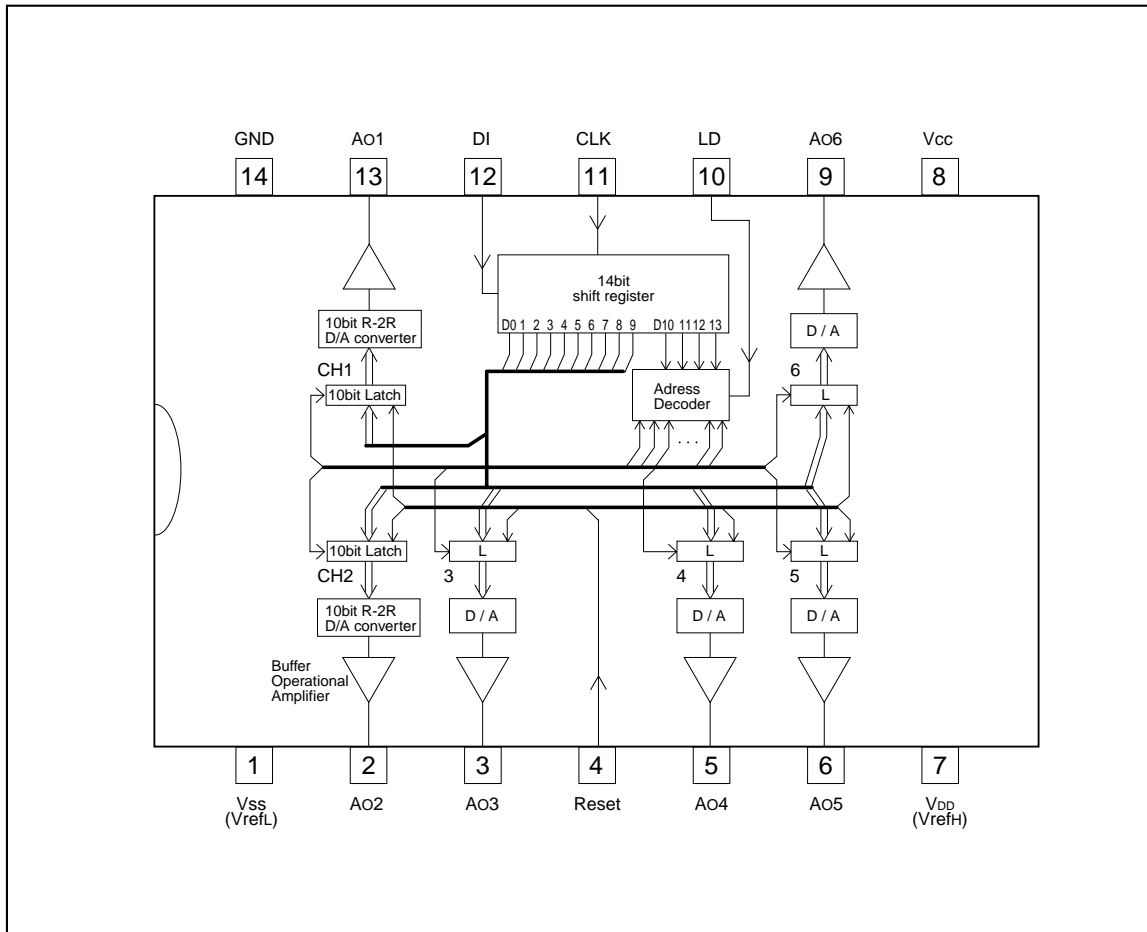| Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	−0.3~+6.0	V
Upper reference voltage of D/A converter	V_{DD}	−0.3~+6.0	V
Input voltage	V_{IN}	−0.3~+6.0	V
Output voltage	V_{OUT}	−0.3~+6.0	V
Power dissipation	Pd	350*	mW
Operating temperature	Topr	−25~+85	°C
Storage temperature	Tstg	−55~+125	°C

∗ Operating at higher than Ta=25°C, 3.5mW shall be redused per 1°C.

●**Recommended operating conditions** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	4.5~5.5	V

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●Block diagram

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●**Pin descriptions**

Pin No.	Pin name	Analog / Digital	I / O	Function	Equivalent Circuit
1	Vss	Analog	–	D/A converter lower reference voltage (VrefL) input terminal	6
2	Ao2	Analog	O	10bit D/A converter output terminal (CH2)	4
3	Ao3	Analog	O	10bit D/A converter output terminal (CH3)	4
4	Reset	Digital	I	The analog output of all channels is fixed for "L"	2
5	Ao4	Digital	O	10bit D/A converter output terminal (CH4)	4
6	Ao5	Analog	O	10bit D/A converter output terminal (CH5)	4
7	VDD	Analog	–	D/A converter upper reference voltage (VrefH) input terminal	5
8	Vcc	–	–	Power supply terminal	–
9	Ao6	Analog	O	10bit D/A converter output terminal (CH6)	4
10	LD	Digital	I	When H-level signal is input to this terminal, the value stored in 14-bit shift register is loaded in decoder and D/A converter output register	1
11	CLK	Digital	I	Shift clock input terminal. Input signal at DI pin is input to 14-bit shift register at rise of shift clock pulse	1
12	DI	Digital	I	Serial data input terminal to input 14-bit (address 4 bit + deta 10bit) long serial data	1
13	Ao1	Analog	O	10bit D/A converter output terminal (CH1)	4
14	GND	–	–	GND terminal	–

●**Input / Output terminal equivalent circuit**

∗1 At the time of Vcc=5.0V, 25kΩ. (It alters by the applied voltage.)

● **Electrical characteristics**

• Digital characteristics (unless otherwise noted, V$_{CC}$=5V, VrefH=5V, VrefL=0V, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	I$_{CC}$	–	0.85	2.8	mA	CLK=10MHz operation, V$_{CC}$=5V, I$_{AO}$=0μA
Input leak current	I$_{ILK}$	–5	–	5	μA	V$_{IN}$=0~V$_{CC}$
Input low voltage	V$_{IL}$	–	–	0.8	V	
Input high voltage	V$_{IH}$	2.0	–	–	V	
Output low voltage	V$_{OL}$	0	–	0.4	V	I$_{OL}$=2.5mA
Output high voltage	V$_{OH}$	4.6	–	5	V	I$_{OH}$=–2.5mA

• Analog characteristics (unless otherwise noted, V$_{CC}$=5V, VrefH=5V, VrefL=0V, Ta=25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Comsumption current		Iref$_H$	–	4.5	7.5	mA	Vref$_H$=5V, Vref$_L$=0V Data condition : Maximum Current
D/A converter upper reference voltage range		Vref$_H$	3.0	–	5	V	Reference voltage can not always be set to any value in this range, because it is restricted to the buffer amplifier output volateg range.
D/A converter lower reference voltage range		Vref$_L$	0	–	1.5	V	
Buffer amplifier output voltage range		V$_O$	0.1	–	4.9	V	Io=±100μA
			0.2	–	4.75		Io=+1.0mA
Buffer amplifier output drive range		Io	–2	–	2	mA	Upper saturation voltage=0.35V Lower saturation voltage=0.23V
Accuracy	Differential nonlinearity error	S$_{DL}$	–1.0	–	1.0	LSB	Vref$_H$=4.796V, Vref$_L$=0.7V V$_{CC}$=5.5V (4mV / LSB) Without load (Io=+0mA)
	Nonlinearity error	S$_L$	–3.5	–	3.5		
	Zero code error	S$_{ZERO}$	–25	–	25	mV	
	Full scale error	S$_{FULL}$	–25	–	25		
Buffer amplifier output impedance		R$_O$	–	5	15	Ω	
Pull-up I/O-cell internal R value		Rup	12.5	25	37.5	kΩ	Win : 0V (Resistance value alters by the applied voltage)

Ⓒ This product is not designed for protection against radioactive rays.

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• AC characteristics (unless otherwise noted, Vcc=5V, VrefH=5V, VrefL=0V, Ta=25°C)

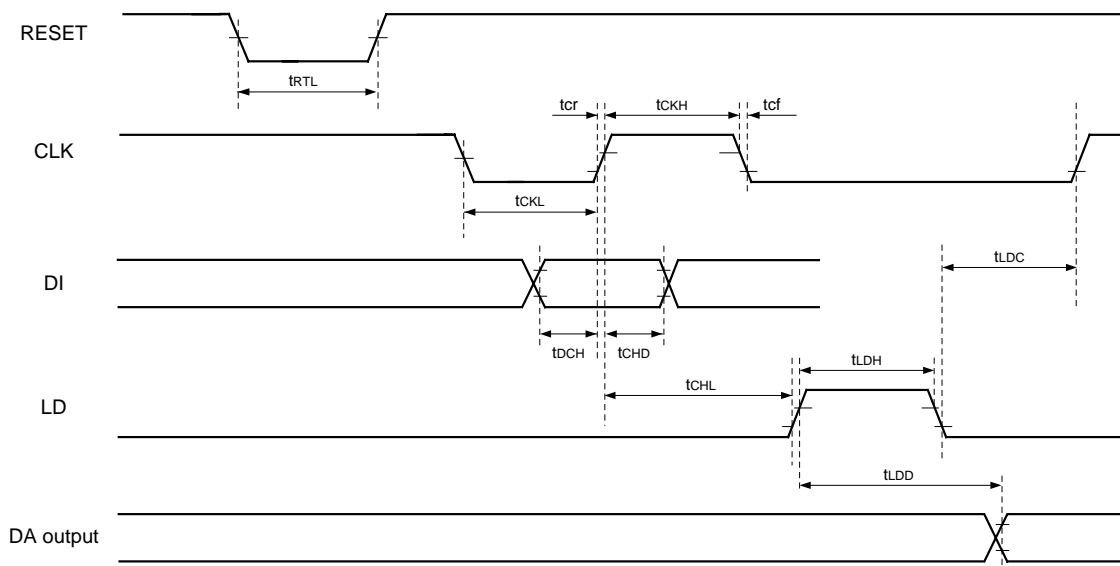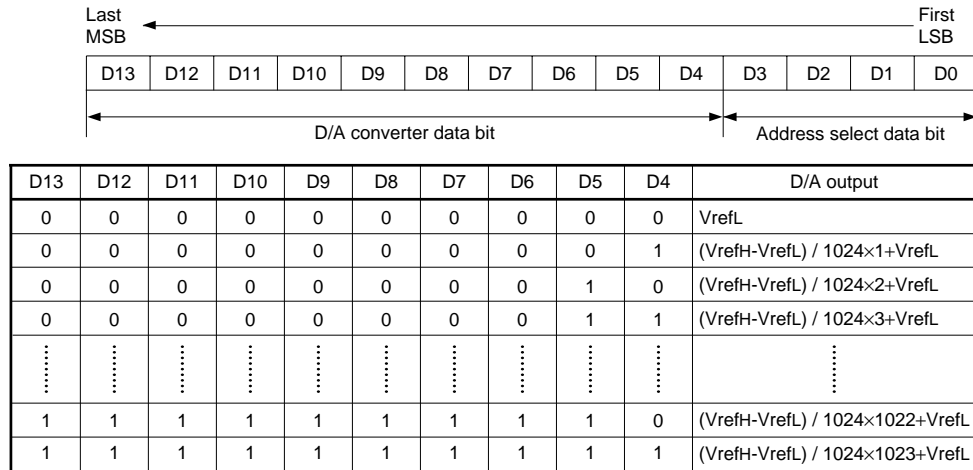| Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reset "L" pulse width	t_{RTL}	50	–	–	ns	
Clock "L" pulse width	t_{CKL}	50	–	–		
Clock "H" pulse width	t_{CKH}	50	–	–		
Clock rise time Clock fall time	tcr tcf	–	–	50		
DATA set up time	t_{DCH}	20	–	–		
DATA hold time	t_{CHD}	40	–	–		
LD set up time	t_{CHL}	50	–	–		
LD hold time	t_{LDC}	50	–	–		
LD "H" pulse duration	t_{LDH}	50	–	–		
D / A output setting time	t_{LDD}	–	7	20	μS	$C_L \leq 1000pF$ $V_O : 0.5V \Leftrightarrow 4.5V$ The time until the becomes the final value of 1/2 LSB.

Fig.1

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● **Circuit operations**

• Digital data format (data : LSB first)

Last MSB													First LSB
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A converter data bit — Address select data bit

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output
0	0	0	0	0	0	0	0	0	0	VrefL
0	0	0	0	0	0	0	0	0	1	$(VrefH-VrefL) / 1024 \times 1 + VrefL$
0	0	0	0	0	0	0	0	1	0	$(VrefH-VrefL) / 1024 \times 2 + VrefL$
0	0	0	0	0	0	0	0	1	1	$(VrefH-VrefL) / 1024 \times 3 + VrefL$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	1	1	0	$(VrefH-VrefL) / 1024 \times 1022 + VrefL$
1	1	1	1	1	1	1	1	1	1	$(VrefH-VrefL) / 1024 \times 1023 + VrefL$

∗ $VrefH = V_{DD}$ $VrefL = V_{SS}$

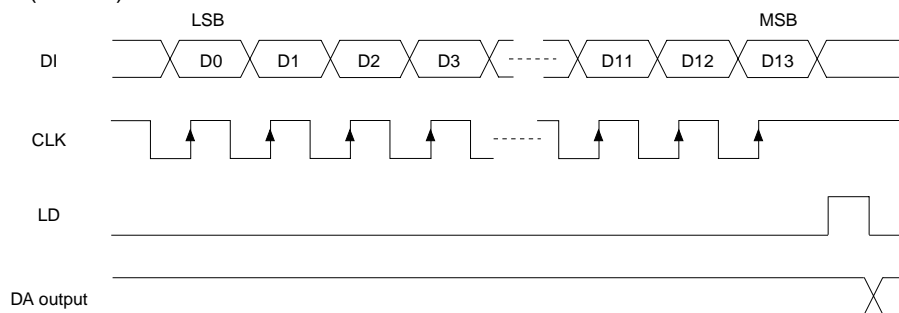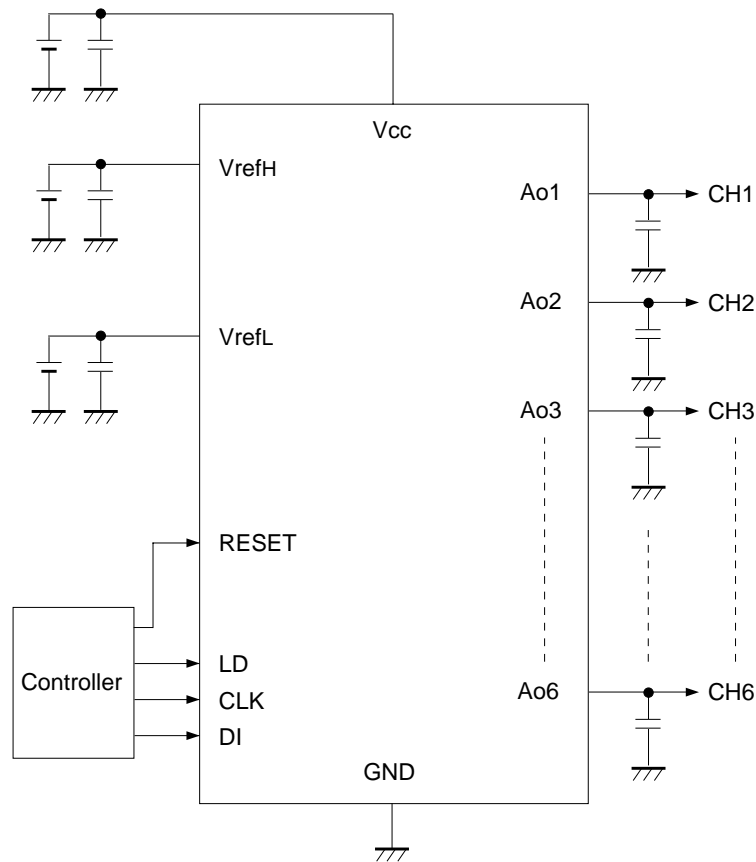| D3	D2	D1	D0	Address selection
0	0	0	0	Don't Care
0	0	0	1	Don't Care
0	0	1	0	AO1 selection
0	0	1	1	AO2 selection
0	1	0	0	Don't Care
0	1	0	1	AO3 selection
0	1	1	0	AO4 selection
0	1	1	1	Don't Care
1	0	0	0	AO5 selection
1	0	0	1	AO6 selection
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Command for test
1	1	1	1	Command for test

• Timing chart (MODEL)

Fig.2

●**Application circuit**

●**Operation notes**
• There are 3 different type of power supply terminal and 1 type of GND terminal in this IC.
  Each of there terminalsrequires the constant power supply for operating.

• Pile up ripple and noise to there power supply terminals, it can't keep accuracy of the D/A converter.
  Therefore external bypass capacitor recommend to set as close as possible to the terminals between V_{DD} and GND
  in order to stabilizes the D/A converter.

• The capacitor between output and GND recommend to set under 100pF including parasitic capacitor in order
  to reduces jitter from layout of the output line and noise.

• RESET terminal uses the I/O-cell of the internal pull-up resistance, adding a capacitor between this terminal and
  GND, this IC will have equivalent function as power-on-reset, by making a time-delay.
  When a reset signal is inputted from the controller, it is possible that the output of all channels are fixed on Low-level in
  the "L" section on the pulse.

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●**External dimensions** (Units : mm)

SSOP-B14

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