

**CMOS Hex Buffer/Converter**

CD4010BMS Hex Buffer/Converter may be used as CMOS to TTL or DTL logic-level converter or CMOS high-sink-current driver.

The CD4050B is the preferred hex buffer replacement for the CD4010BMS in all applications except multiplexers. The CD4010BMS is supplied in these 16 lead outline packages:

- Braze Seal DIP H4S
- Frit Seal DIP H1E
- Ceramic Flatpack H6W

**Features**

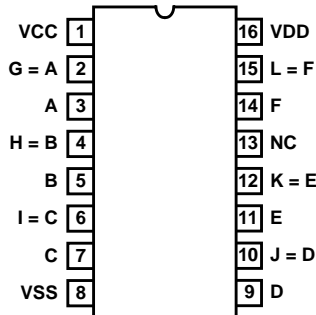
- Non-Inverting Type
- High-Voltage Type (20V Rating)
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1 $\mu$ A at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25 $^{\circ}$ C
- 5V, 10V and 15V Parametric Ratings

**Applications**

- CMOS To DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-to-Low Logic-Level Converter
- Multiplexer - 1 to 6 or 6 to 1

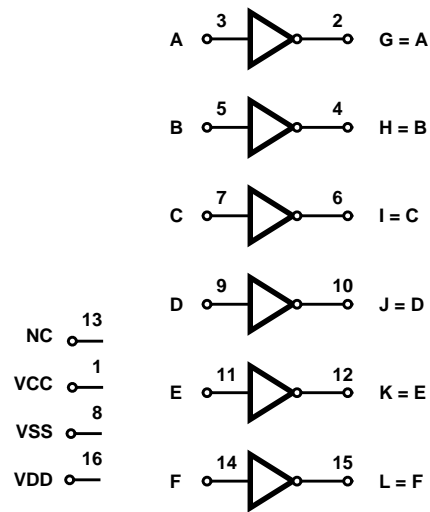
**Pinout**

CD4010BMS  
TOP VIEW



NC = NO CONNECTION

**Functional Diagram**



NC = NO CONNECTION

# CD4010BMS

## Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V  
 (Voltage Referenced to VSS Terminals)  
 Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V  
 DC Input Current, Any One Input . . . . . ±10mA  
 Operating Temperature Range . . . . . -55°C to +125°C  
 Package Types D, F, K, H  
 Storage Temperature Range (TSTG) . . . . . -65°C to +150°C  
 Lead Temperature (During Soldering) . . . . . +265°C  
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for  
 10s Maximum

## Reliability Information

Thermal Resistance . . . . .  $\theta_{ja}$   $\theta_{jc}$   
 Ceramic DIP and FRIT Package . . . . . 80°C/W 20°C/W  
 Flatpack Package . . . . . 70°C/W 20°C/W  
 Maximum Package Power Dissipation (PD) at +125°C  
 For TA = -55°C to +100°C (Package Type D, F, K) . . . . . 500mW  
 For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate  
 Linearity at 12mW/°C to 200mW  
 Device Dissipation per Output Transistor . . . . . 100mW  
 For TA = Full Package Temperature Range (All Package Types)  
 Junction Temperature . . . . . +175°C

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
			VDD = 18V	2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
			VDD = 18V	2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.0	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	8.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	24.0	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.2	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-0.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-0.45	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-1.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C		1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5		V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C		4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11		V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.  
 2. Go/No Go test with limits applied to inputs

# CD4010BMS

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	T <sub>PHL</sub>	VDD = 5V, VIN = VDD or GND	9	+25°C	-	130	ns
			10, 11	+125°C, -55°C	-	175	ns
Propagation Delay	T <sub>PLH</sub>	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	T <sub>THL</sub>	VDD = 5V, VIN = VDD or GND	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	94	ns
Transition Time	T <sub>TLH</sub>	VDD = 5V, VIN = VDD or GND	9	+25°C	-	350	ns
			10, 11	+125°C, -55°C	-	473	ns

**NOTES:**

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	μA
				+125°C	-	30	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	μA
				+125°C	-	60	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	μA
				+125°C	-	120	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+25°C	2.6	-	mA
				+125°C	1.8	-	mA
				-55°C	3.2	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.1	-	mA
				-55°C	3.75	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	5.6	-	mA
				-55°C	10.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	16.0	-	mA
				-55°C	30.0	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.15	mA
				-55°C	-	-0.25	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-0.58	mA
				-55°C	-	-1.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.33	mA
				-55°C	-	-0.55	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-1.1	mA
				-55°C	-	-1.65	mA

# CD4010BMS

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL	VDD = 10V, VCC = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V, VCC = 15V	1, 2, 3	+25°C	-	50	ns
Propagation Delay	TPLH	VDD = 10V, VCC = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V, VCC = 15V	1, 2, 3	+25°C	-	70	ns
Propagation Delay	TPHL	VDD = 10V, VCC = 5V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	40	ns
Propagation Delay	TPLH	VDD = 10V, VCC = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	70	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

**NOTES:**

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL	VDD = 5V, VCC = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns
	TPLH						

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

**TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C**

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

# CD4010BMS

**TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE:

1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

**TABLE 7. TOTAL DOSE IRRADIATION**

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

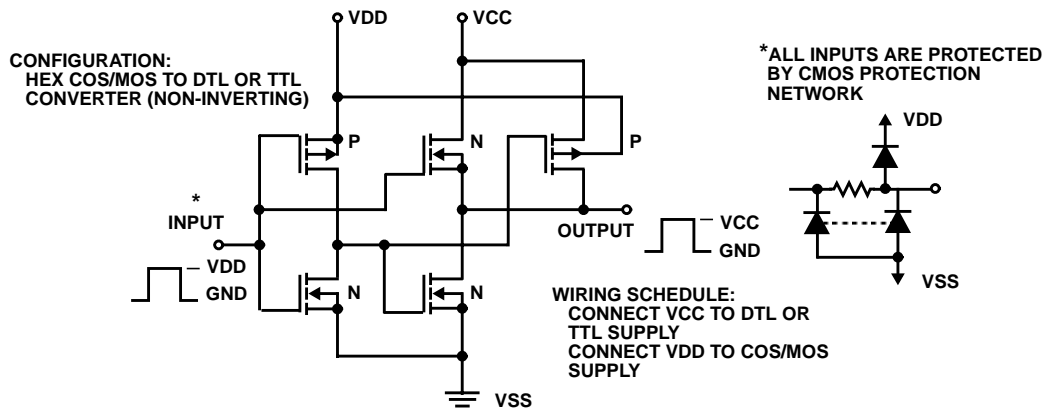
**TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS**

FUNCTION	OPEN	GROUND	VDD	9V ± 0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 13, 15	3, 5, 7 - 9, 11, 14	1, 16			
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			
Dynamic Burn-In (Note 3)	13	8	1, 16	2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			

NOTES:

1. Each pin except VDD and Pin 1 and GND will have a series resistor of  $10K \pm 5\%$ ,  $VDD = 18V \pm 0.5V$
2. Each pin except VDD and Pin 1 and GND will have a series resistor of  $47K \pm 5\%$ ; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures,  $VDD = 10V \pm 0.5V$
3. Each pin except VDD and Pin 1 and GND will have a series resistor of  $4.75K \pm 5\%$ ,  $VDD = 18V \pm 0.5V$

## Schematic Diagram



Typical Performance Characteristics

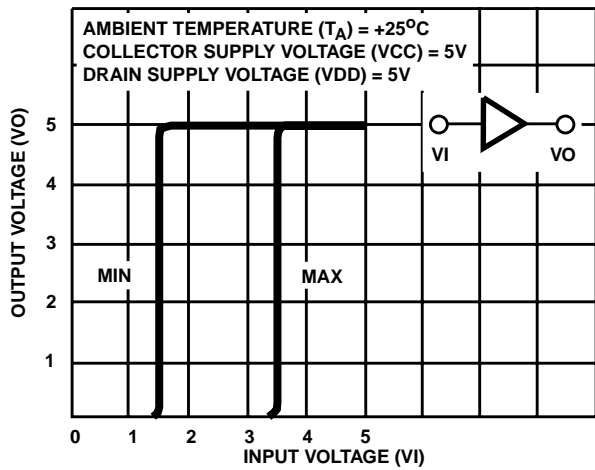


FIGURE 1. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS (VDD = 5)

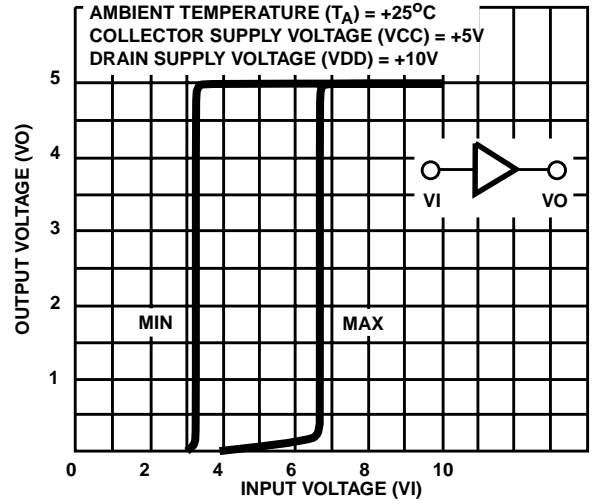


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS (VDD = 10)

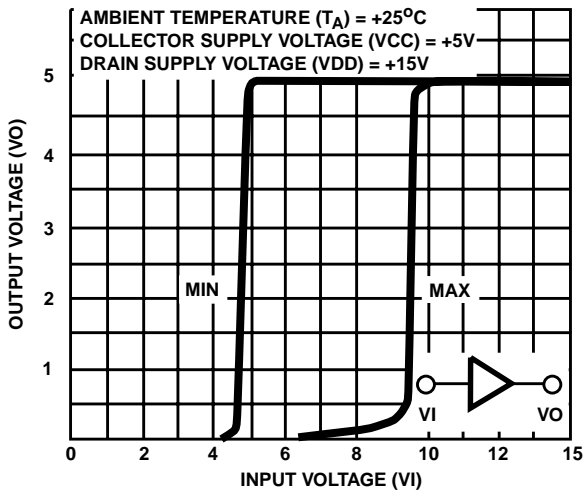


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS (VDD = 15)

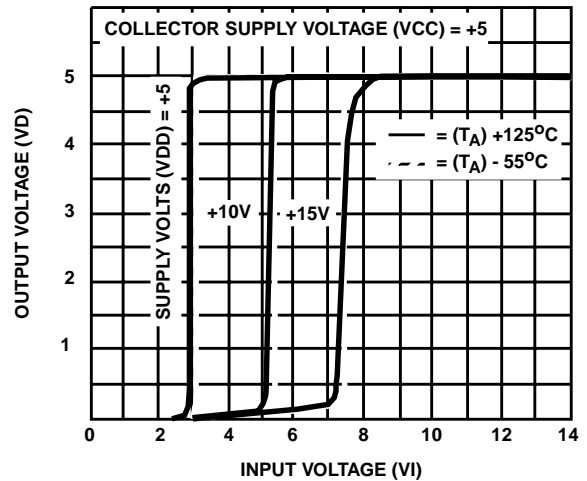


FIGURE 4. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

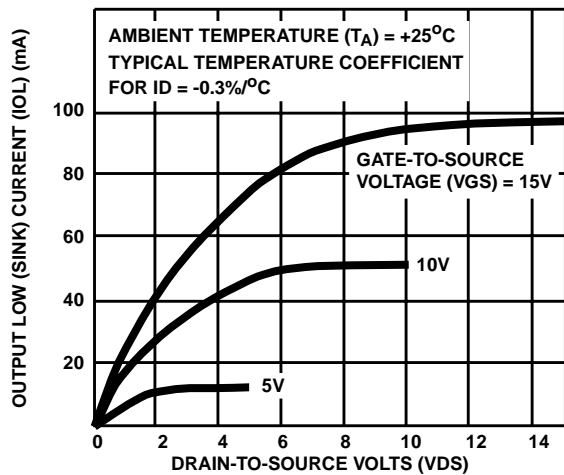


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

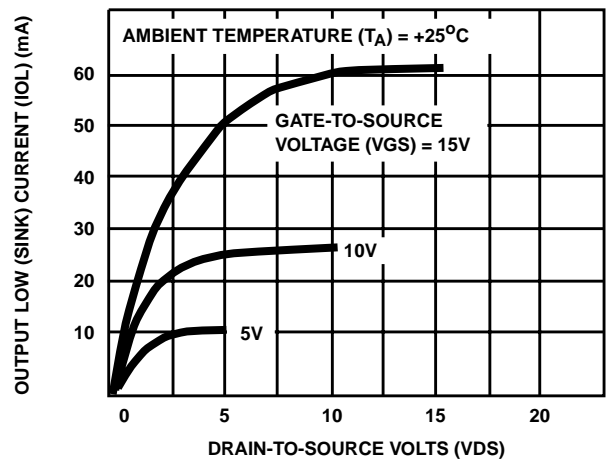


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

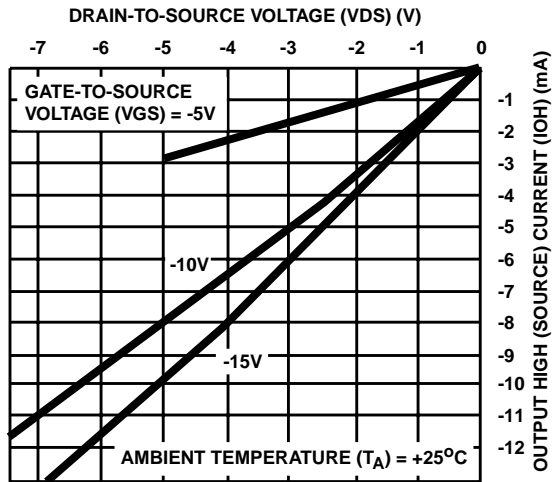


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

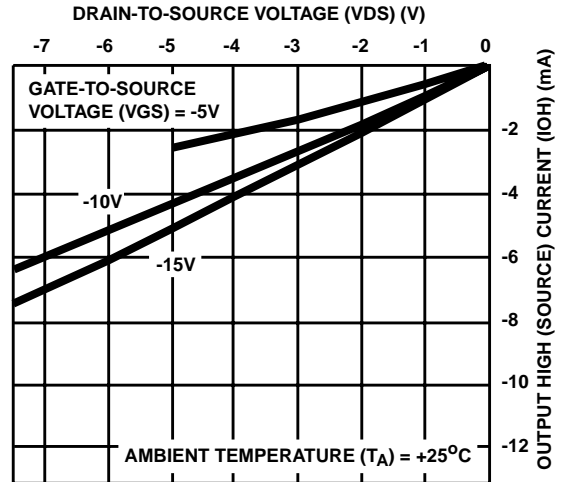


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

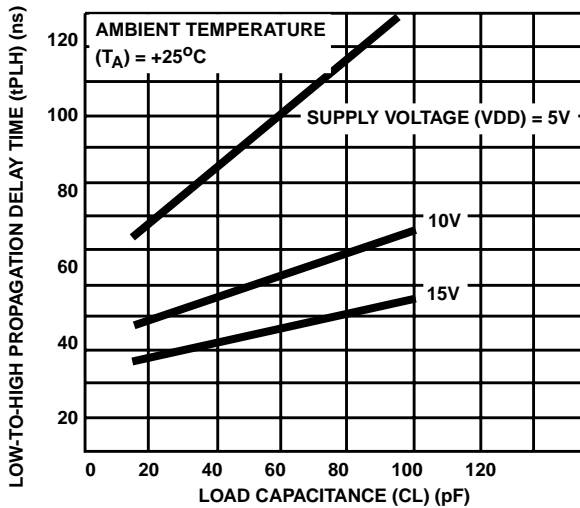


FIGURE 9. TYPICAL LOW-TO-HIGH PROPAGATION DELAYTIME vs LOAD CAPACITANCE

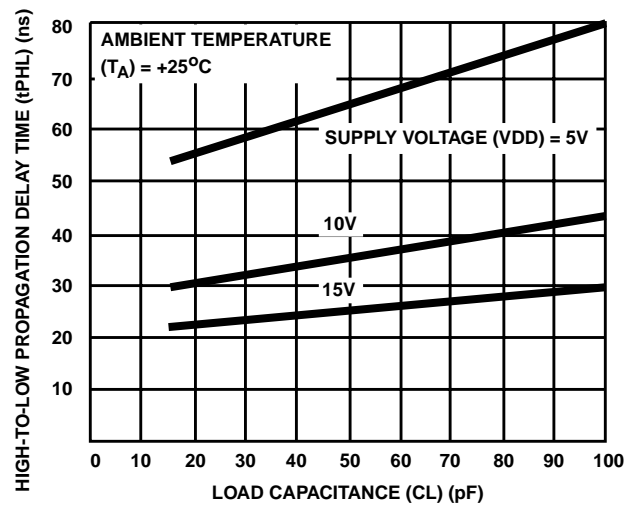


FIGURE 10. TYPICAL HIGH-TO-LOW PROPAGATION DELAYTIME vs LOAD CAPACITANCE

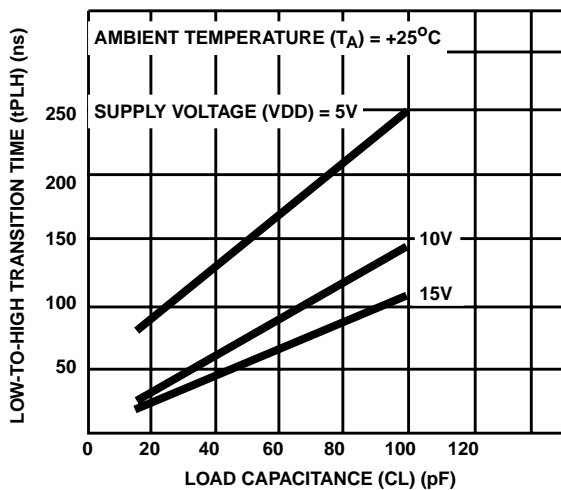


FIGURE 11. TYPICAL LOW-TO-HIGH TRANSITION TIME vs LOAD CAPACITANCE

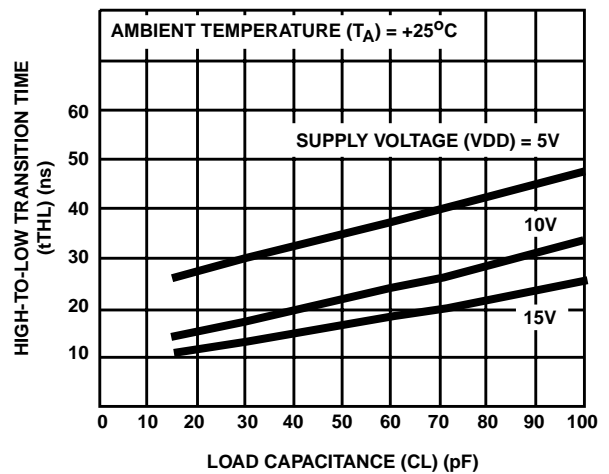


FIGURE 12. TYPICAL HIGH-TO-LOW TRANSITION TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

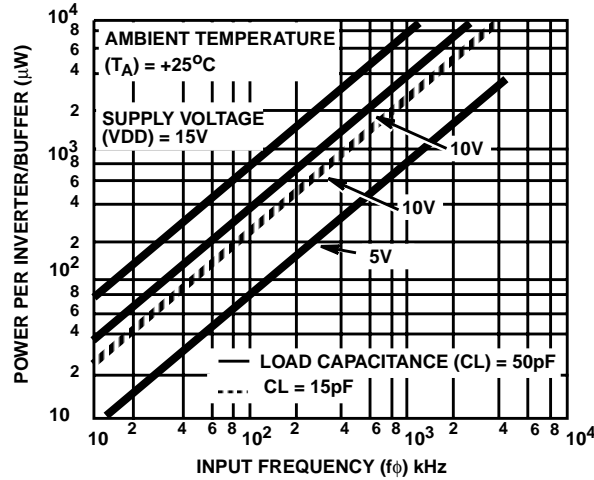
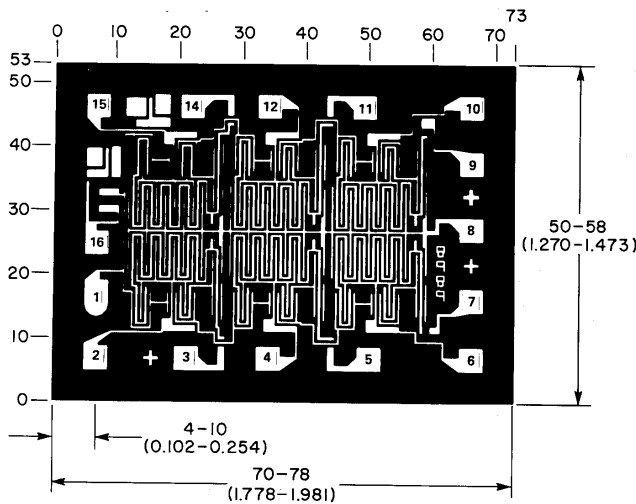


FIGURE 13. TYPICAL DISSIPATION CHARACTERISTICS

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch)

- METALLIZATION:** Thickness:  $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$ , AL.
- PASSIVATION:**  $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$ , Silane
- BOND PADS:** 0.004 inches X 0.004 inches MIN
- DIE THICKNESS:** 0.0198 inches - 0.0218 inches

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Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

**ASIA**  
Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029