National Semiconductor

ADVANCE INFORMATION

CGS74B303/CGS74B304/CGS74B305
Octal Divide-by-2 Circuits/Clock Drivers

General Description

These minimum skew clock drivers are designed for Clock Generation & Support (CGS) applications. The devices guarantee minimum output skew across the outputs of a given device and also from device-to-device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. These octal dividers contain eight flip-flops designed to have minimum skews between the outputs. The '303 is a minimum skew clock driver with six in-phase with CLK and two out-of-phase outputs. The '304 is a minimum skew clock driver with eight in-phase with CLK outputs. The '305 is a minimum skew clock driver with four in-phase with CLK and four out-of-phase outputs.

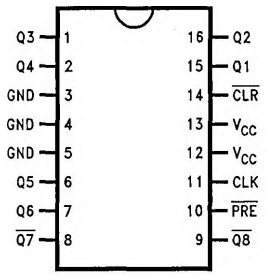
Features

- Functionality compatible to industry standard AS303, AS304 and AS305
- Maximum output skew of less than 1 ns to meet the tight skew budget required in hi-speed clocking schemes
- Specifications for device-to-device variation of output skew to ensure tight skew over process variations
- Specification for transition skew to meet near-50% output duty cycle requirements
- Center pin V_{CC} and GND configuration to minimize high speed switching noise
- Capability of current sourcing 48 mA and current sinking of 64 mA
- Lowest dynamic power consumption at high frequencies

Connection Diagrams

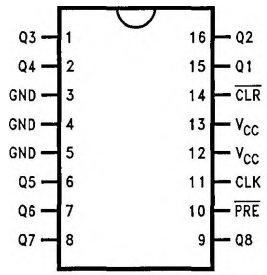
Pin Assignment for DIP and SOIC

'303



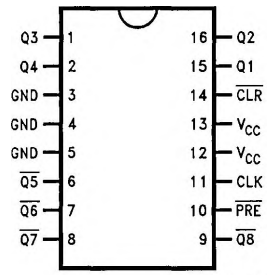
TL/F/10966–1

'304



TL/F/10966–2

'305



TL/F/10966–3

National Semiconductor

CGS74B2525
1-to-8 Minimum Skew Clock Driver

General Description

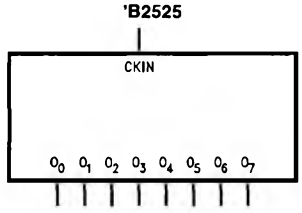
This minimum skew clock driver is designed for Clock Generation and Support (CGS) applications operating well above 20 MHz (33 MHz, 50 MHz). The device guarantees minimum output skew across the outputs of a given device and also from device-to-device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The 'B2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications.

Features

- Clock Generation and Support (CGS) Device—Ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST® LSI process
- 1-to-8 low skew clock distribution
- Sub 1 ns pin-to-pin output skew
- Specifications for device-to-device variation of propagation delay
- Specification for transition skew to meet duty cycle requirements
- Center pin V_{CC} and GND configuration to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 4

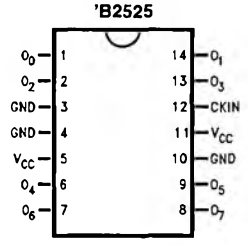
Logic Symbol



TL/F/10907–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10907–2

Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when the ('B2525) clock distribution chip is selected.

Pin Description

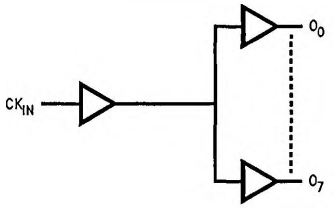
Pin Names	Description
CK_{IN}	Clock Input ('B2525)
O_0–O_7	Outputs

Truth Table

'B2525

Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'B2525



TL/F/10907–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V	
Input Voltage (V_I)	7.0V	
Operating Free Air Temperature	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	
Typical θ_{JA}		
Plastic (N) Package	104	°C/W
JEDEC SOIC (M) Package	120	°C/W

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage—High (V_{IH})	2.0V
Input Voltage—Low (V_{IL})	0.8V
High Level Output Current (I_{OH})	−48 mA
Low Level Output Current (I_{OL})	+64 mA
Free Air Operating Temperature (T_A)	0°C to +70°C

DC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = −48 mA, V_{CC} = 4.5V		2.0			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 64 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IH} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		8	15	mA
			Outputs Low		32	42	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Symbol	Parameter	CGS74B			Units
		V_{CC} = 4.5V to 5.5V R_L = 500Ω, C_L = 50 pF			
		Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay CK to O_n ('2525)	2 2	2.9 3.0	4.8 4.8	ns

Extended AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74B $R_L = 500\Omega$, $C_L = 50$ pF, $T_A = 0°C$ to $70°C$			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation (Note 1)	5.0		0.7	1.5	ns
t_{PV}	Maximum Skew Part-to-Part Variation Skew (Note 2)	5.0			1.75	ns
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6	1.5	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (from 0.5/2.4V to 2.4/0.5V at 33 MHz, $T_A = 25°C$)	5.0 5.0		1.90 1.15		ns ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.