GSM 4 W power amplifier CGY2010G

FEATURES

- Power amplifier (PA) final stage efficiency 65%
- 34.5 dB PA gain, temperature compensated
- PA gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < –133 dBm/Hz in GSM RX band
- Wide operating temperature range –20 to +85 °C
- LQFP 48 package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

APPLICATIONS

- 890 to 915 MHz hand-held transceivers for GSM applications
- 900 MHz TDMA systems.

GENERAL DESCRIPTION

The CGY2010G is a GSM class 4 GaAs power amplifier specifically designed to operate at 4.8 V supply. The chip also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. It can be switched off and its power varied by monitoring the actual drain voltage applied to its drains.

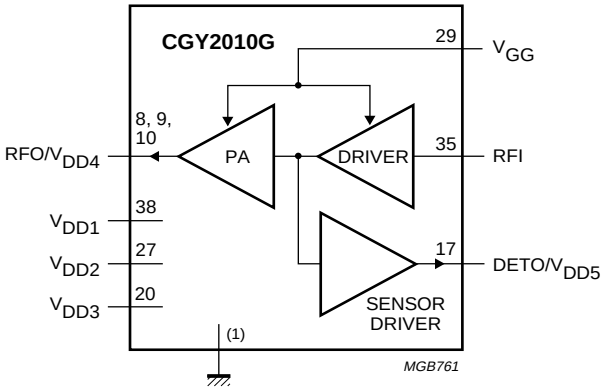
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	–	4.2	5.5	V
I_{DD}	supply current	–	1.8	2.2	A
T_{amb}	operating ambient temperature	–20	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2010G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 7, 11 to 16, 18 and 19, 21 to 26, 28, 30 to 34 36 and 37 and 39 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 7	ground
RFO/V_{DD4}	8 to 10	power amplifier output and supply voltage 4
GND	11 to 16	ground
DETO/V_{DD5}	17	power sensor output and supply voltage 5
GND	18 and 19	ground
V_{DD3}	20	third stage supply voltage 3
GND	21 to 26	ground
V_{DD2}	27	second stage supply voltage 2
GND	28	ground
V_{GG}	29	negative gate supply voltage
GND	30 to 34	ground
RFI	35	power amplifier input
GND	36 and 37	ground
V_{DD1}	38	first stage supply voltage 1
GND	39 to 48	ground

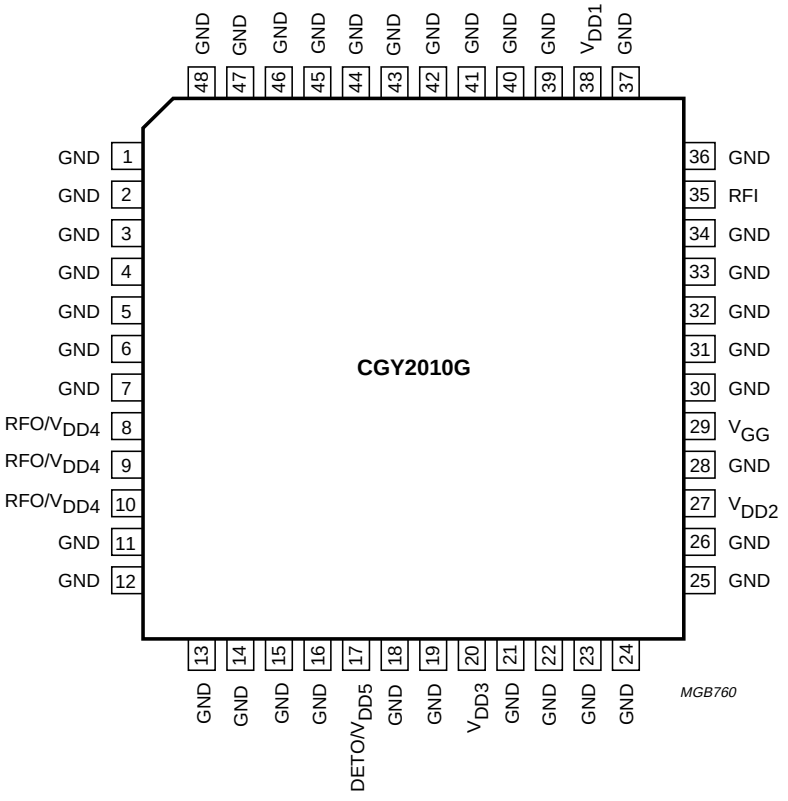


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply. The amplifier bias is set by means of a negative voltage applied at pin V_{GG}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress of the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage. Impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–	7	V
V_{GG}	negative gate supply voltage	–	–10	V
$T_{ch(max)}$	maximum operating channel temperature	–	+150	°C
T_{stg}	storage temperature	–	+150	°C
P_{tot}	total power dissipation	–	1	W

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	tbf	K/W

DC CHARACTERISTICS

V_{DD} = 4.2 V, T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	supply voltage		0	4.2	5.5	V
I_{DD}	supply current		–	1.8	2.2	A
Pin V_{GG}						
V_{GG}	negative bias voltage	note 1	–	–1.5	–	V
I_{GG}	negative bias current		–	3	12	mA

Note

1. The negative bias V_{GG} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

V_{DD} = 4.2 V, T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_{in}	input power		–1.5	–	1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	–8	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{out(max)}$	maximum output power	T_{amb} = 25 °C	34.5	–	–	dBm
		T_{amb} = –20 to +55 °C	32.5	–	–	dBm
η	efficiency		45	–	–	%
$P_{out(min)}$	minimum output power	V_{DD} = tbf	–	–	–20	dBm
N_{RX}	output noise in RX band		–	–	–133	dBm/Hz
H2	2nd harmonic level		–	–	–33	dBc
H3	3rd harmonic level		–	–	–38	dBc
	stability	load VSWR 6 : 1; all phases	–	–	tbf	dBc
Power sensor driver						
$P_{out(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–18	–16	–14	dBc
$\Delta P_{out(DET)}$	driver output power variation	load VSWR <6 : 1 at PA output	–	–	tbf	dB

Note

1. Including the 110 Ω resistor connected in parallel at the power amplifier input on the application board.

APPLICATION INFORMATION

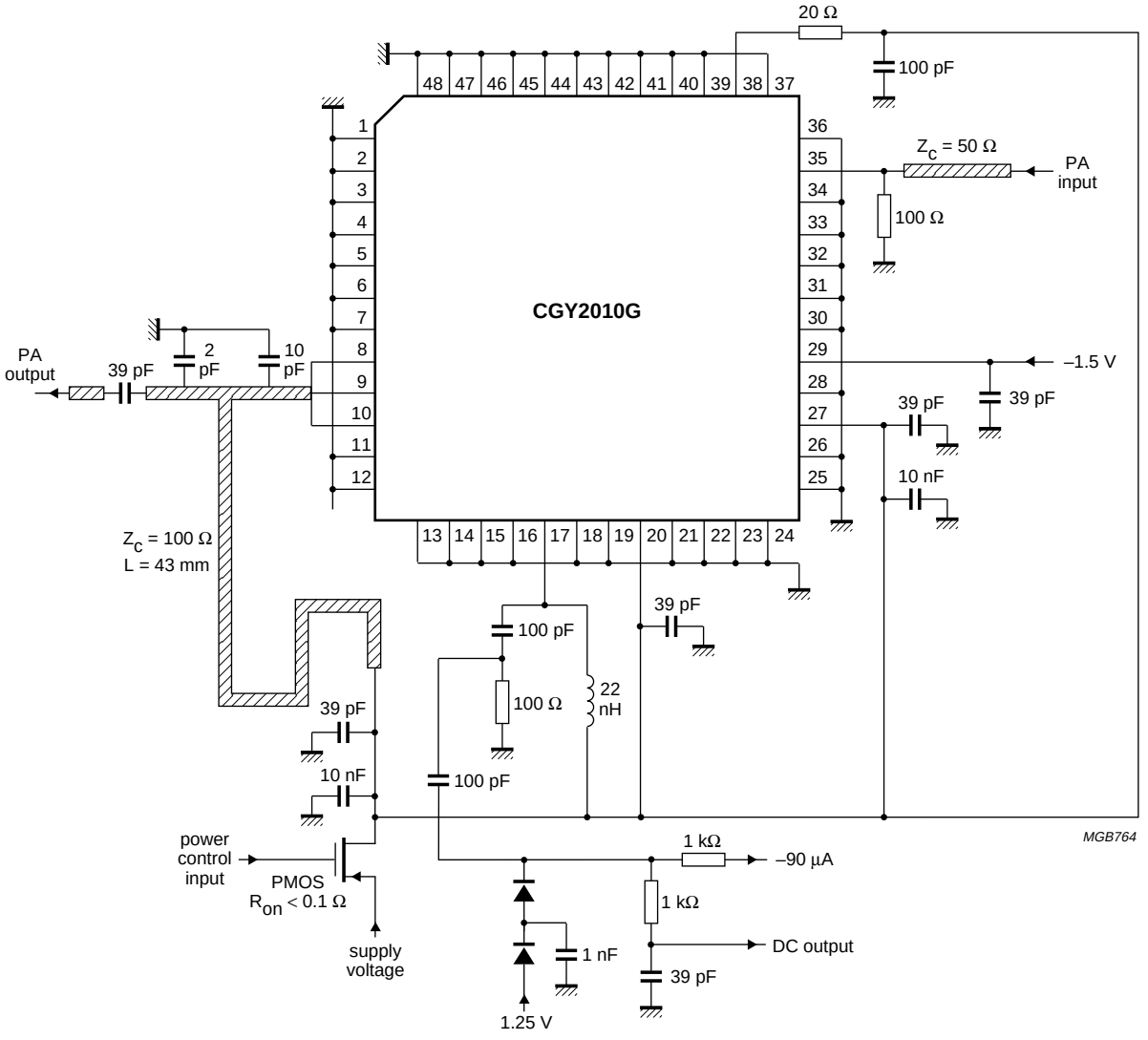


Fig.3 Application diagram.