CS1088

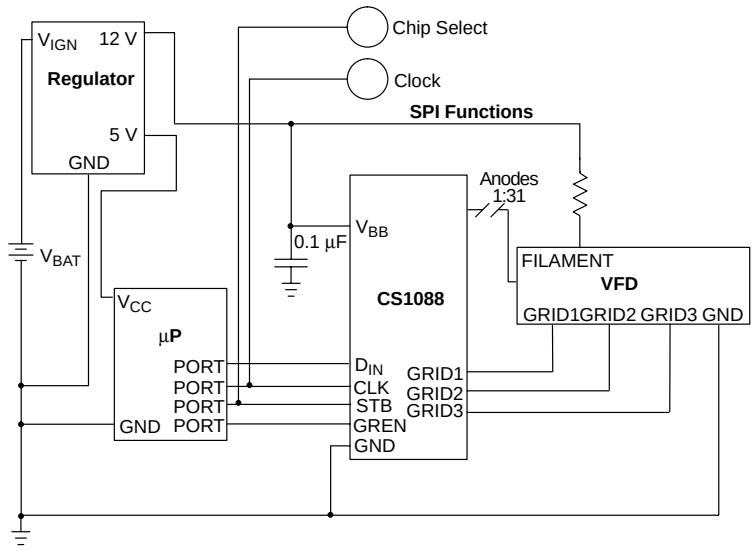
Vacuum Fluorescent Display Tube Driver

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 34–bit shift register, a 34–bit transparent data latch, a metal mask ROM, six 20 mA anode output drivers, twenty–five 2 mA anode output drivers, and three 50 mA grid drivers with output enables. The metal mask programmable ROM (at factory request) allows the 31 anode outputs and 3 grid outputs to be assigned to any of the 34 serial data bits.

Features

- Metal Mask ROM
- Six 20 mA Anode drivers
- Twenty–five, 2 mA Anode drivers
- Three, 50 mA Grid drivers
- Power On Reset
- Display Dimming Possible

APPLICATION DIAGRAM



ON Semiconductor

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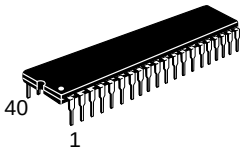


DIP–40
WIDE BODY
N SUFFIX
CASE 711

ORDERING INFORMATION

Device	Package	Shipping
CS1088XN40	DIP–40 WIDE BODY	9 Units/Rail

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

ABSOLUTE MAXIMUM RATINGS*

Parameter		Value	Unit
Supply Voltage (V_{BB})		–0.6 to +18	V
Input Voltages (D_{IN}, CLK, STB, GREN)		–0.6 to +6.0	V
Junction Temperature Range		–40 to +150	°C
Storage Temperature Range		–55 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV
ESD Susceptibility (Machine Model)		200	V
Lead Temperature Soldering:	Wave Solder (through hole styles only) Note 1. Reflow (SMD styles only) Note 2.	260 Peak 230 Peak	°C

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ($8.0\ V \le V_{BB} \le 16.5\ V$, Gnd = 0 V, $-40°C \le T_J \le 105°C$; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BB} Input					
V_{BB} Input Voltage	–	8.0	–	16.5	V
I_{BB0} Current	No outputs active, V_{BB} = 16.5 V	–	2.0	5.0	mA
Reset Mode	All outputs forced low.	–	6.5	7.5	V
D_{IN}, CLK, STB Inputs					
V_{IL1}, Input Low Voltage	–	–	–	1.6	V
V_{IH}, Input High Voltage	–	3.3	–	–	V
I_{IL}, Input Current	$V_{IN} = V_{IH}$	0	7.5	20.0	μA
GREN Input					
V_{IL}, Input Low Voltage	–	–	–	1.6	V
V_{IH}, Input High Voltage	–	3.3	–	–	V
I_{IH}, Input Pull–down Current	V_{IN} = 3.325 V	–	30	60	μA
GRID1, GRID2, GRID3 Outputs					
I_{OL}	Sink Current	1.0	–	–	mA
I_{OH}	Source Current	50	–	–	mA
V_{OL}	I_{OUT} = 1.0 mA	–	–	0.5	V
V_{OH}	I_{OUT} = –50 mA, V_{BB} = 12 V	V_{BB} – 0.75	–	V_{BB}	V
AN24 – AN29 Outputs					
I_{OL}	Sink Current	400	–	–	μA
I_{OH}	Source Current	20	–	–	mA
V_{OL}	I_{OUT} = 400 μA	–	–	0.5	V
V_{OH}	I_{OUT} = –20 mA, V_{BB} = 12 V	V_{BB} – 0.5	–	V_{BB}	V
AN1 – AN23 Outputs					
I_{OL}	Sink Current	100	–	–	μA
I_{OH}	Source Current	2.0	–	–	mA
V_{OL}	I_{OUT} = 100 μA	–	–	0.5	V
V_{OH}	I_{OUT} = –2.0 mA, V_{BB} = 12 V	V_{BB} – 0.5	–	V_{BB}	V

ELECTRICAL CHARACTERISTICS (continued) (8.0 V ≤ V_{BB} ≤ 16.5 V, Gnd = 0 V, –40°C ≤ T_J ≤ 105°C; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
AC Characteristics: Input and Output Timing					
F_C, CLK Frequency	–	0	–	1.0	MHz
T_{CL}, CLK Low Time	–	200	–	–	ns
T_{CH}, CLK High Time	–	200	–	–	ns
T_{CR}, CLK Rise Time	–	–	–	100	ns
T_{CF}, CLK Fall Time	–	–	–	100	ns
T_{SC}, STB Low to CLK High Time	–	50	–	–	ns
T_{ST}, STB High Time	–	500	–	–	ns
T_{AN}, STB High to Anode Output Propagation Delay	–	–	–	5.0	μs
T_{GL}, Grid Turn On Propagation Delay	V_{BB} = 12 V	–	–	2.0	μs
T_{G0}, Grid Turn Off Propagation Delay	V_{BB} = 12 V	–	–	5.0	μs
T_{GR}, Grid Rise Time	At rated load. Note 1.	0.50	–	2.00	μs
T_{GF}, Grid Fall Time	At rated load. Note 1.	0.35	–	2.00	μs
T_{AR}, Anode Rise Time	At rated load. Note 1.	0.40	–	2.00	μs
T_{AF}, Anode Fall Time	At rated load. Note 1.	0.40	–	2.50	μs

1. Grid and anode rise / fall times are measured from 10% and 90% points. Output currents are at the maximum rated currents for the respective stages.

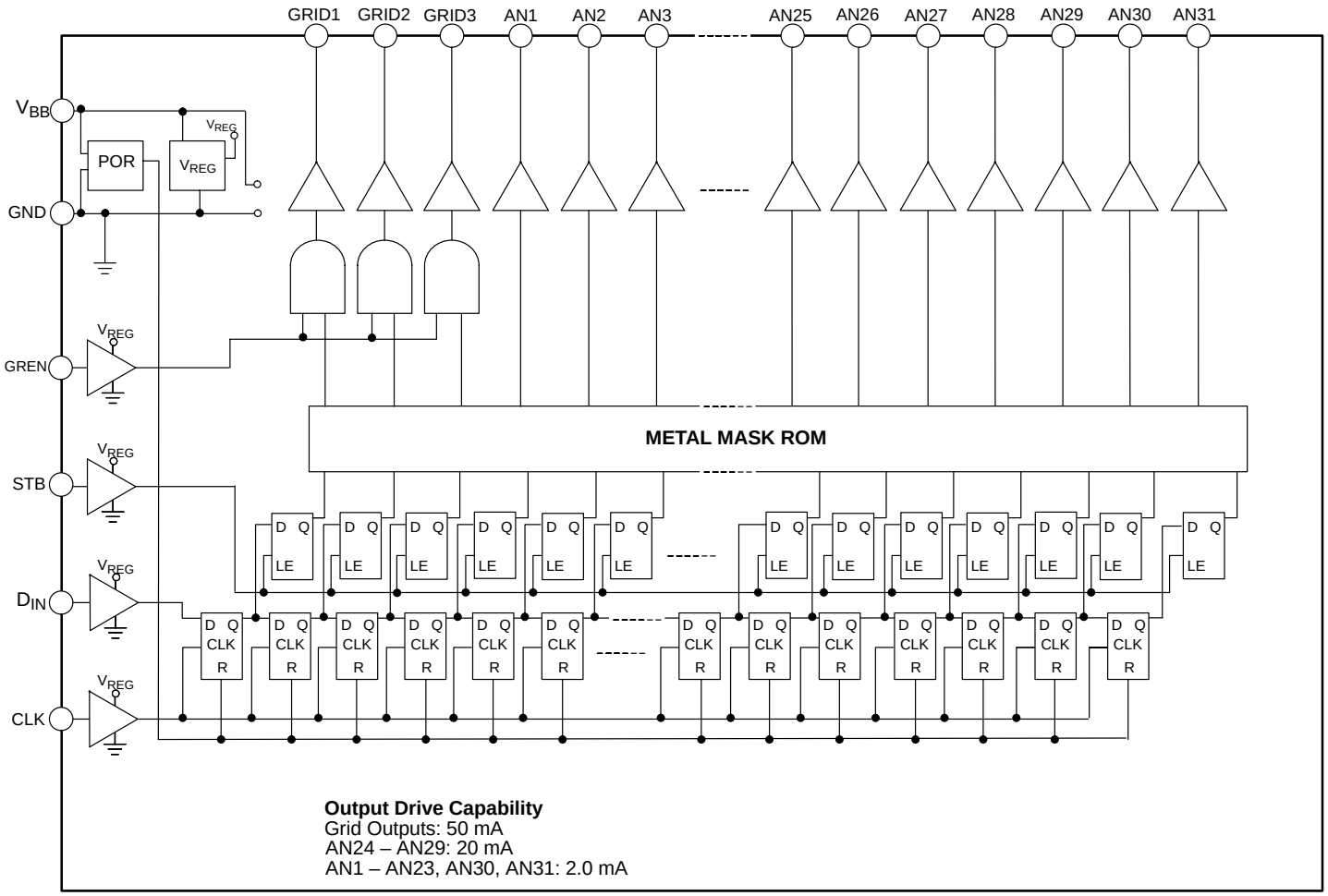
PACKAGE LEAD DESCRIPTION

Package Lead Number	Lead Symbol	
40L DIP	(31 Anode Configuration)	Function
1	GRID1	50 mA grid output.
2	GRID2	50 mA grid output.
3	GRID3	50 mA grid output.
4	AN1	2.0 mA anode output.
5	AN2	2.0 mA anode output.
6	AN3	2.0 mA anode output.
7	AN4	2.0 mA anode output.
8	AN5	2.0 mA anode output.
9	AN6	2.0 mA anode output.
10	AN7	2.0 mA anode output.
11	AN8	2.0 mA anode output.
12	AN9	2.0 mA anode output.
13	AN10	2.0 mA anode output.
14	AN11	2.0 mA anode output.
15	AN12	2.0 mA anode output.
16	AN13	2.0 mA anode output.
17	AN14	2.0 mA anode output.
18	AN15	2.0 mA anode output.
19	AN16	2.0 mA anode output.

PACKAGE LEAD DESCRIPTION (continued)

Package Lead Number	Lead Symbol	
40L DIP	(31 Anode Configuration)	Function
20	GND	Ground connection.
21	AN17	2.0 mA anode output.
22	AN18	2.0 mA anode output.
23	AN19	2.0 mA anode output.
24	AN20	2.0 mA anode output.
25	AN21	2.0 mA anode output.
26	AN22	2.0 mA anode output.
27	AN23	2.0 mA anode output.
28	AN24	20 mA anode output.
29	AN25	20 mA anode output.
30	AN26	20 mA anode output.
31	AN27	20 mA anode output.
32	AN28	20 mA anode output.
33	AN29	20 mA anode output.
34	AN30	2.0 mA anode output.
35	D_{IN}	Shift register data input.
36	CLK	Shift register clock input.
37	STB	Transfer contents of shift registers to output stages.
38	GREN	Grid outputs enable.
39	AN31	2.0 mA anode output.
40	V_{BB}	Supply voltage input.

BLOCK DIAGRAM



OPERATION DESCRIPTION

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the D_{IN} pin at the rising edge of the CLK input. Thirty four bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN31 are always enabled.

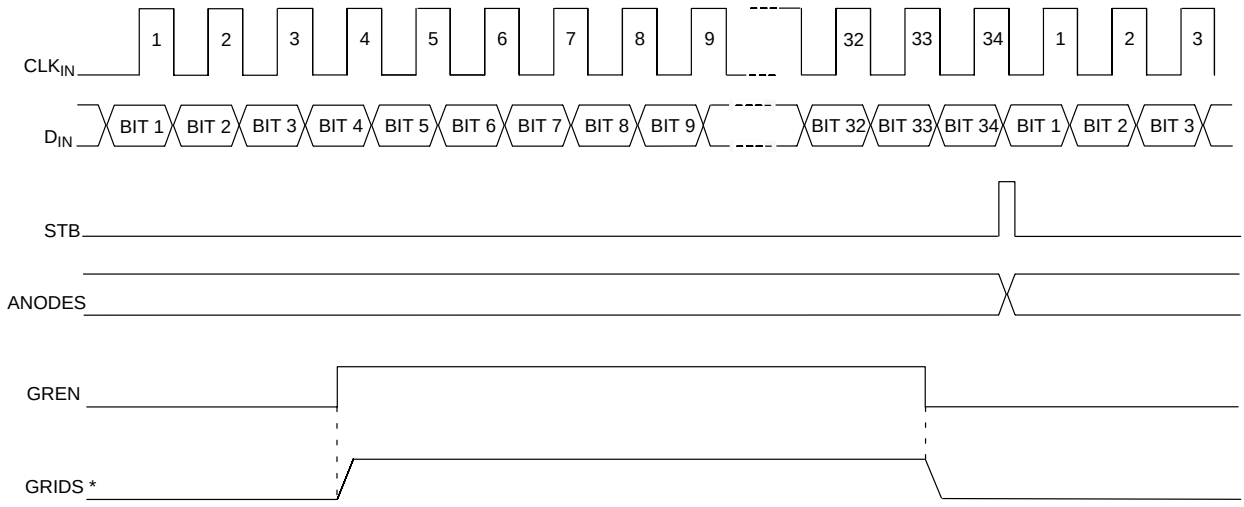
APPLICATION INFORMATION

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Pin Name	G1	G2	G3	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14

Bit #	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
Pin Name	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31

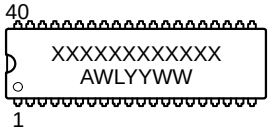
Table 1: Bit Pattern, G = Grid, A = Anode.

TYPICAL OPERATION



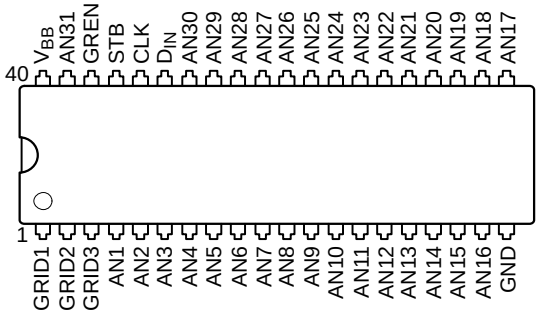
* Selected grid goes high only if input bit pattern from shift register to grid is high.

MARKING DIAGRAMS



DIP–40
WIDE BODY
N SUFFIX
CASE 711

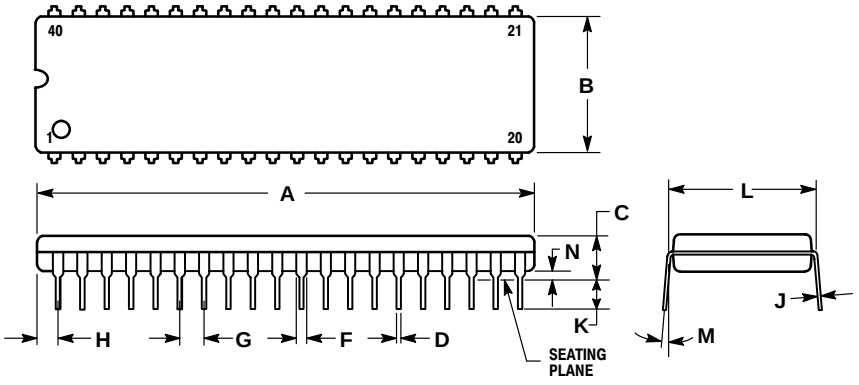
PIN CONNECTIONS



XXX... = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

DIP–40
WIDE BODY
N SUFFIX
CASE 711–03
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

PACKAGE THERMAL DATA

Parameter		DIP–40 WIDE BODY	Unit
$R_{\Theta JC}$	Typical	20	°C/W
$R_{\Theta JA}$	Typical	45	°C/W

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
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