SONY

CXA1314P/CXA1414P

Video Switch Compatible with I²C Bus

For the availability of this product, please contact the sales office.

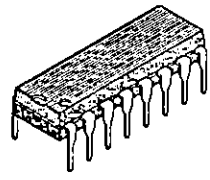
Description

CXA1314 and CXA1414 were developed as video switches for the I²C bus.

Features

- Serial control through I²C bus.
- 3 channels for video input and 2 channels for video output.
- The 2 channels for video output are respectively independent and allow for input selection at will.
- Composite/S pin signal discrimination output.
- Video input 1 selection information output.
- Gain=6 dB amplifier built-in video system.
- Wide band video amplifier (15 MHz, −3dB)
- Slave address for CXA1314 and CXA1414 differ.
  CXA1314: 92H
  CXA1414: 94H

16pin DIP (Plastic)



Applications

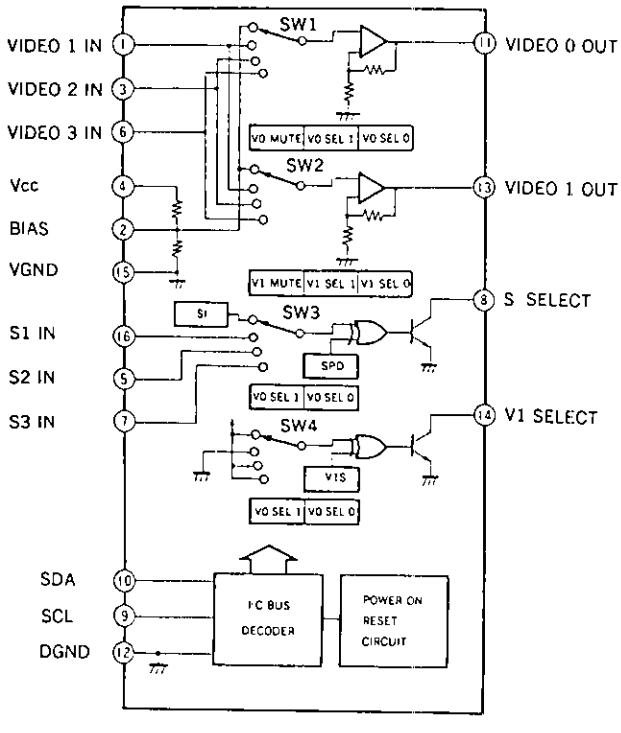
Usage of CXA1114 in conjunction with CXA1314 and CXA1414 form an AV switch block where there are 4 channels for input and 3 for output for each of video and audio respectively. When CXA 1314 and 1414 are combined S video features 3 channels for input and 2 for output.

Structure

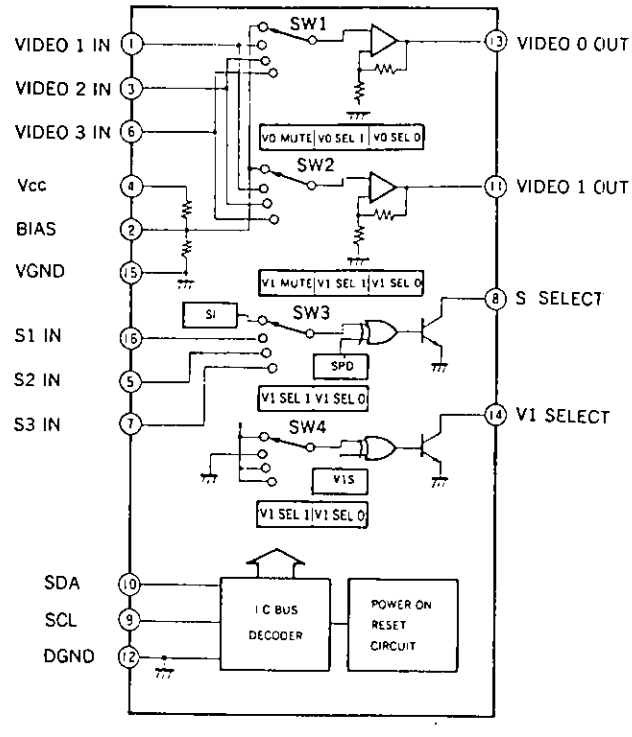
Bipolar silicon monolithic IC

Block Diagram

CXA1314



CXA1414



E88Z46A02-HP

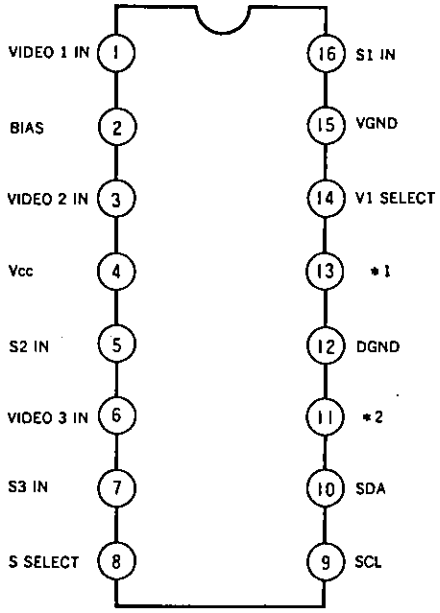
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to 150	°C
• Allowable power dissipation	P_D	960	mW

Recommended Operating Conditions

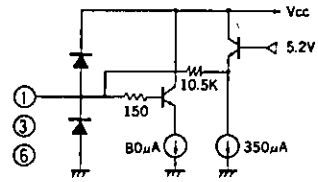
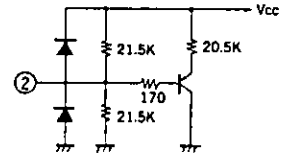
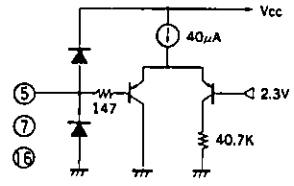
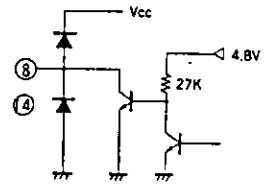
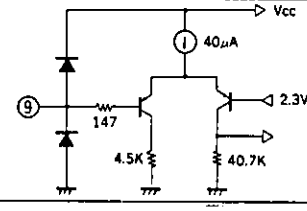
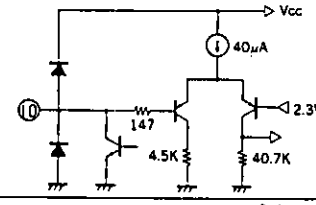
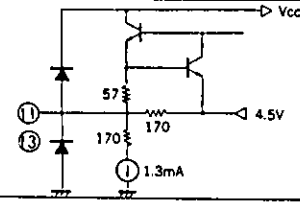
• Supply voltage	V_{CC}	8 to 10	V
• Operating temperature	T_{opr}	−20 to +75	°C

Pin Configuration (Top View)



* 1 CXA1314: VIDEO 1 OUT
  CXA1414: VIDEO 0 OUT
* 2 CXA1314: VIDEO 0 OUT
  CXA1414: VIDEO 1 OUT

Pin Description

No.	Symbol	Pin Voltage	Equivalent circuit	Description
1 3 6	VIDEO 1 IN VIDEO 2 IN VIDEO 3 IN	4.5V		Video input 1, 2, 3 input pins.
2	BIAS	4.6V		Builds up $V_{CC}/2$ that becomes the internal bias reference. Supply ripple is suppressed by installing a capacitor. Cut off frequency is supplied through $f_0=\frac{1000}{2\pi\times11\times C\ (\mu F)}$ [Hz]
4	V_{CC}	9.0V		Supply voltage pin.
5 7 16	S 2 IN S 3 IN S 1 IN			S signal 1, 2, 3 selection information pin. Threshold level is set to about 2.3V.
8 14	S SELECT V1 SELECT			Pin 8 (S SELECT) outputs the control signal for the select switch of S signal/composite video signal. Switch of S signal/composite video signal. Pin 14 (V1 SELECT) is the output pin for the select infomation of video signal 1. (For details refer to the paragraph for operation description). Both pins are for open collector output.
9	SCL			SCL (Serial Clock Line) of I²C bus standards. Threshold level is set to about 2.3V.
10	SDA			SDA (Serial Data Line) of I²C bus standards. Threshold level is set to about 2.3V.
11 (13) 13 (11)	VIDEO 0 OUT VIDEO 1 OUT	4.5V		Video output 0, 1 output pin.
12	DGND			Digital GND pin.
15	VGND			Video GND pin.

*( ): CXA1414

Electrical Characteristics

Ta=25°C, V_{CC}=9V

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Consumption current	I_{CC}	V_{CC}=9V, No signal, No load	(Fig. 1)	12	20	28	mA
BIAS	$V_{CC}/2$	V_{CC}=9V, No signal, No load	(Fig. 6)	4.2	4.6	5.0	V

Video System (Symbol/Condition)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
I/O pin voltage	V_{vpin}	V_{CC}=9V No signal, No load	(Fig. 6)	4.1	4.5	4.9	V
Frequency characteristics	F_{bwv}	0.3Vp-p input,	(Fig. 3)	10	15	—	MHz
Gain	GV_V	f=100kHz, 0.3Vp-p input	(Fig. 3)	5.5	6.0	6.5	dB
Input dynamic range	V_{dv}	f=1kHz, distortion<MAx. input of 1.0%	(Fig. 3)	2.0	3.0	—	Vp-p
Crosstalk between video outputs	V_{ctv}	f=4.43MHz, 1Vp-p input	(Fig. 3)	—	−55	−50	dB
Input resistance	R_{inv}	Tested at DC	(Fig. 2)	7	11	15	kΩ
Ripple rejection ratio	RR_V	f=100Hz, 0.3Vp-p added to V_{CC}	(Fig. 4)	—	−35	−30	dB
Output impedance	R_{OV}	f=100kHz, 2Vp-p input	(Fig. 5)	—	12	30	Ω

I²C BUS logic system

See Fig. 7

Item	Symbol	Min.	Typ.	Max.	Unit
High level input	V_{IH}	3.0	—	5.0	V
Low level input voltage	V_{IL}	0	—	1.5	V
Low level output voltage	V_{OL}	0	—	0.4	V
During SAD, 3mA inflow	f_{SCL}	0	—	100	kHz
Min. waiting time for data modification	t_{BUF}	4.7	—	—	μs
Min. waiting time for start of data transfer	$t_{HD,STA}$	4.0	—	—	μs
Low level clock pulse width	t_{LOW}	4.7	—	—	μs
High level clock pulse width	t_{HIGH}	4.0	—	—	μs
Min. waiting time for start preparation	$t_{SU,STA}$	4.7	—	—	μs
Min. data hold time	$t_{HD,DAT}$	5	—	—	μs
Min. data preparation time	$t_{SU,DAT}$	250	—	—	ns
Rising time	t_R	—	—	1	μs
Falling time	t_F	—	—	300	ns
Min. stop preparation time	$t_{SU,STO}$	4.7	—	—	μs

S pin information logic system

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IHS}	S1 to 3 IN	3.0	—	9.0	V
Low level input voltage	V_{ILS}	S1 to 3 IN	0	—	1.5	V
Low level output voltage	V_{OLS}	SSEL, VISEL, during 1mA flow in	0	—	0.4	V

Electrical Characteristics Test Circuit

* 1: CXA1314: V1 OUT, CXA1414: V0 OUT
* 2: CXA1314: V0 OUT, CXA1414: V1 OUT

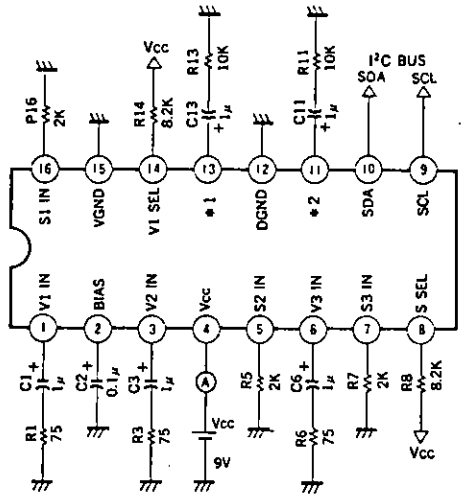


Fig. 1

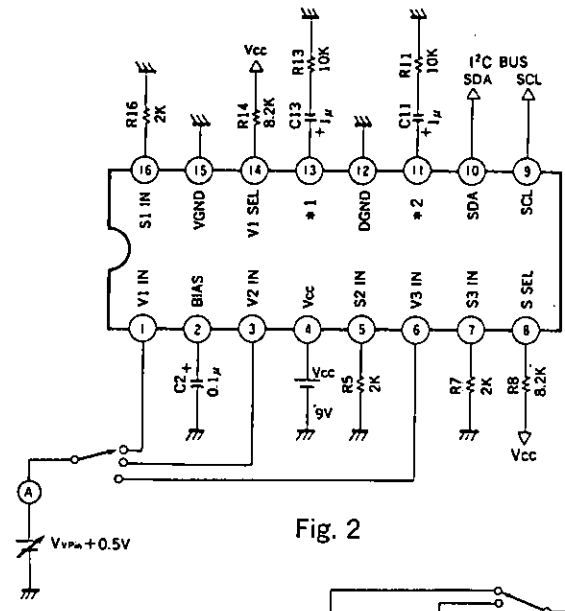


Fig. 2

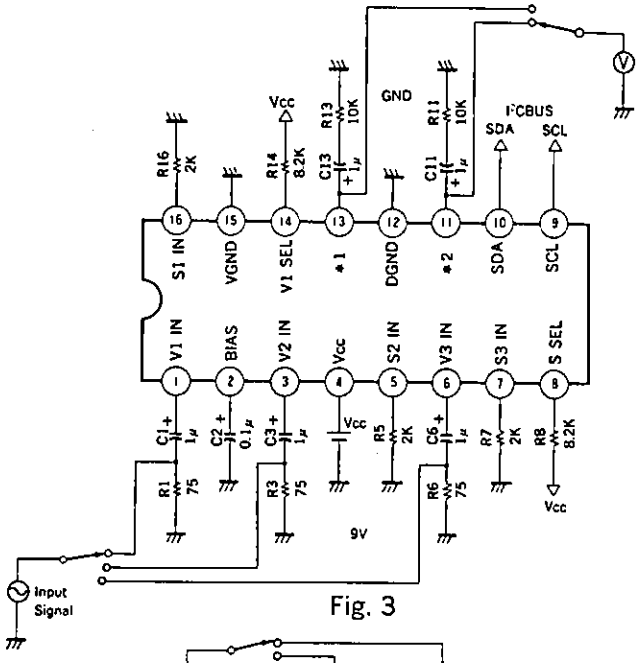


Fig. 3

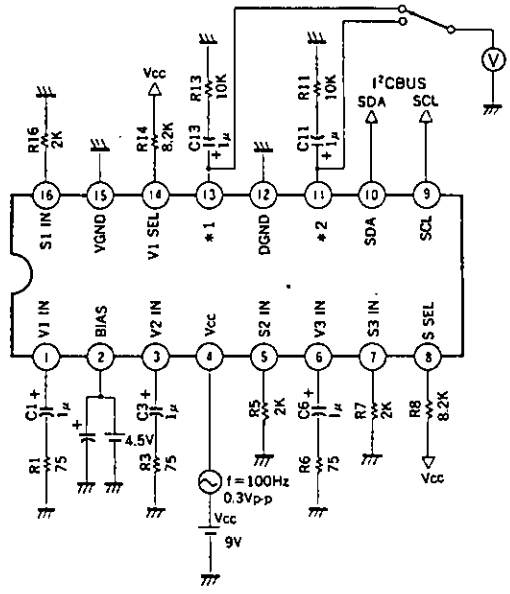


Fig.4

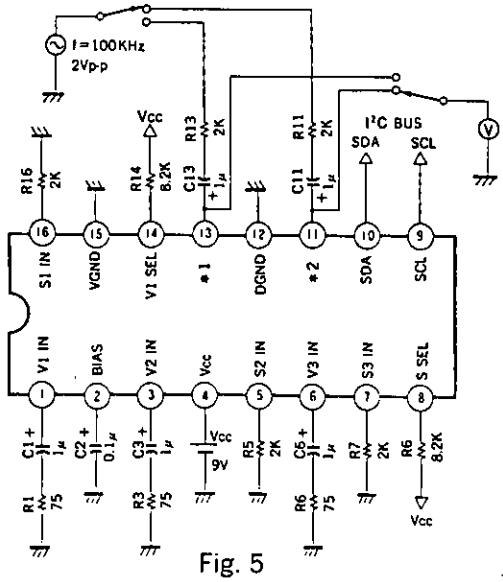


Fig. 5

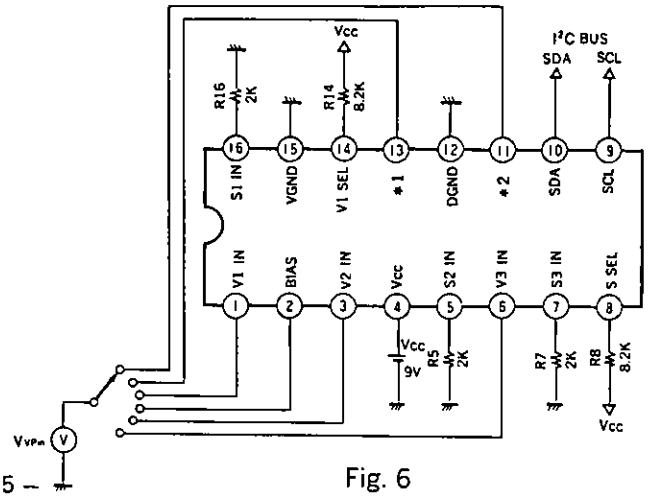


Fig. 6

I²C BUS control signal

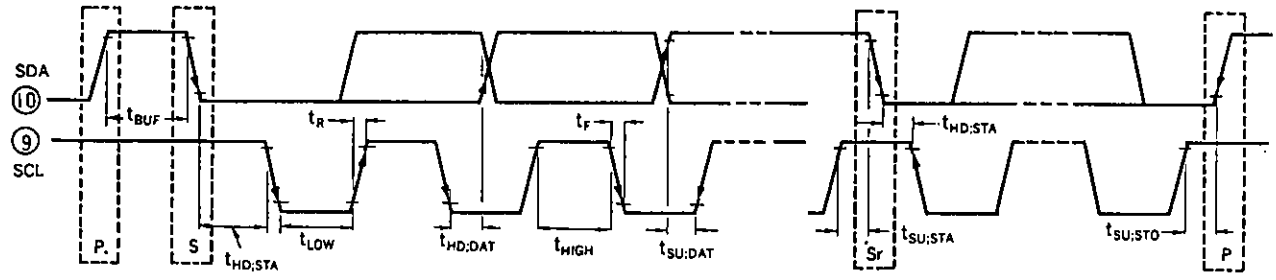


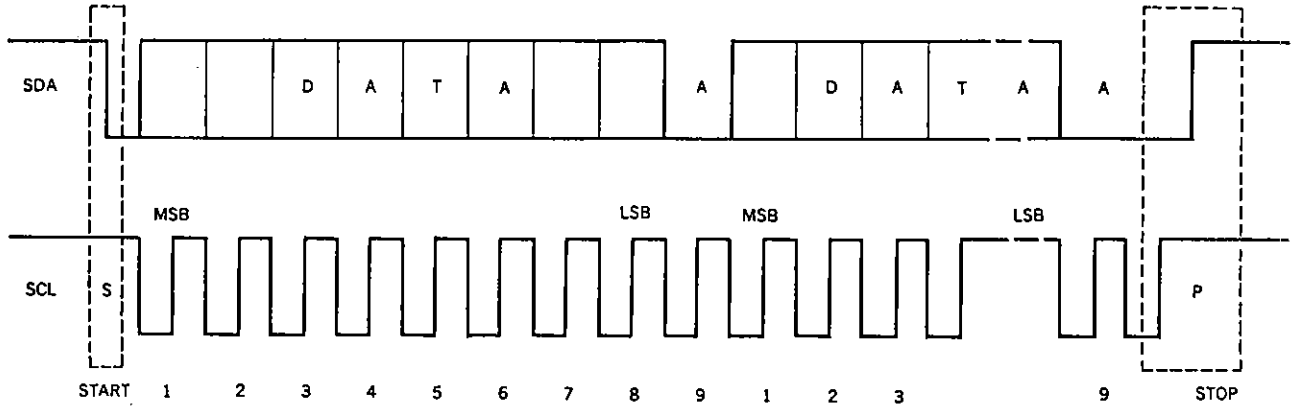
Fig. 7

Operation

CXA1314/CXA1414 is video switches which feature 3 channels for video input and 2 channels for video output. At the respective outputs an amplifier of about 6dB is built in. Respective outputs can independently select the desired output. This is executed through I²C bus.

1. I²C BUS

I²C bus (Inter IC bus) is a bus system inside the equipment developed by Philips. Start, Stop, Data transfer, Sync, and Collision prevention can be executed through two lines, SDA and SCL. The output of respective IC's is either an open collector or an open drain, shaped into a wired OR and forming the bus line . The bus signal structure is indicated as follows.



S : Start Condition .....High to Low transition of the SDA while SCL is High.
P : Stop Condition.....Low to High transition of the SDA while SCL is High.
A : Acknowledge .....Reply signal coming from slave.

Data is transferred by MSB first. 8 bits in one unit. Afterthat aknowledge is set on to confirm the signal from Slave.*1 Normally, Slave IC's take in data with the rising edge of SCL while Master*2 IC's change data with the falling edge of SCL. The actual data format is indicated as follows.

S	Slave address $92_H/94_H$	A	DATA 0	A	DATA 1	A	DATA 2	A	P

Slave address is an address proper to the IC that is assigned to each IC according to its functions. From the 8-bits the upper 7-bits are proper addresses while the last bit is allocated to R/W. This R/W bit turns to Read*3 at 1 and Write*4 at 0. For CXA1314/CXA1414 92H/94H is assigned as slave address. (Write only as there is no Read mode)

* 1. Slave: IC controlled by the master. Normally, all IC's except microcomputers are slaves.
* 2. Master: Modicates IC's on the side that controls, such as microcomputers.
* 3. Read: Mode in which Master reads out data from slave.
* 4. Write: Mode in which data is read out from master to slave.

2. CXA1314/CXA1414 control

CXA1314/CXA1414 control is perfomed by writing 3 bytes of data into 3 control registers composed of 8-bits (as 5-bits are empty actually 3-bits) that control the output selection circuits of 2 systems. First byte data (DATA 0) performs the input selection of VIDEO 0 OUT and second byte data (DATA 1) that of VIDEO 1 OUT. Third byte data (DATA 2) controls other I/O modes. CXA1314/CXA1414 slave address is 92H/94H for Write mode only.

S	Slave address $92_H/94_H$	A	DATA 0	A	DATA 1	A	DATA 2	A	P

S : Start condition
A : Aknowledge emitted by slave (CXA1314/CXA1414)
P : Stop condition

Control Register Structure

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
[DATA 0]	X	V0MUTE	V0SEL 1	V0SEL 0	X	X	X	X
[DATA 1]	X	V1MUTE	V1SEL 1	V1SEL 0	X	X	X	X
[DATA 2]	X	SI	* 1	* 2	X	X	X	X

*X: Undefined
*All registers are set to 0 at the IC reset.
*1 CXA1314: SPD, CXA1414: V1S
*2 CXA1314: V1S, CXA1414: SPD

Registers Description

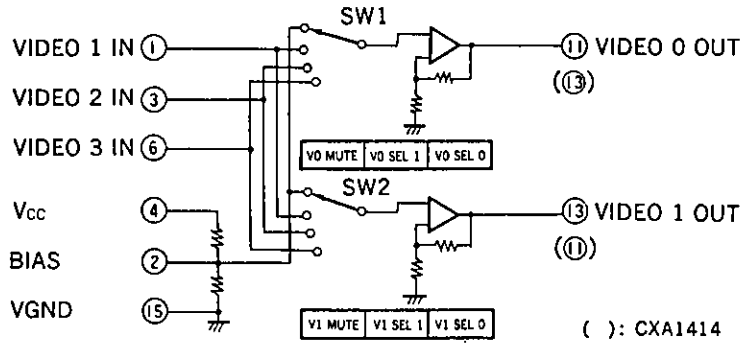
[DATA 0] : SW_1 control data (Source select of VIDEO 0 OUT)

[DATA 1] : SW_2 control data (Source select of VIDEO 1 OUT)

V* MUTE	V* SEL 1	V* SELO	Input pin
0	X	X	Mute (blanking)
1	0	0	Mute
1	0	1	VIDEO 1 IN
1	1	0	VIDEO 2 IN
1	1	1	VIDEO 3 IN

* *: Either 0 or 1.

* X: Undefined.



[DATA 2] : Select information control data of S signal/video signal and video signal 1.

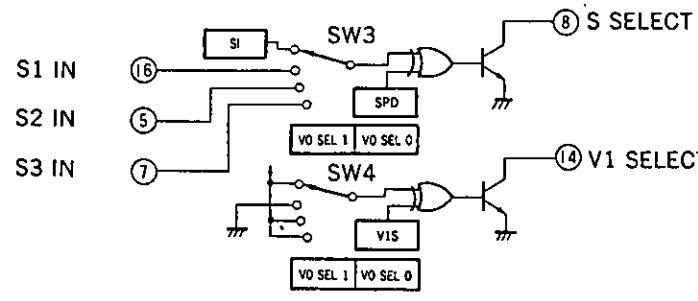
SI : When S pin is selected, set to the reverse polarity of S1 IN through S3 IN input polarity. If S pin selection is defined as "0" for S1 IN to S3 IN , SI is at "1". When S pin selection is defined as "1", SI is set to "0".

In CXA1314 SW3 is controlled by V0 SEL 1 and V0 SEL 0.

In CXA1414 SW3 is controlled by V1 SEL 1 and V1 SEL 0.

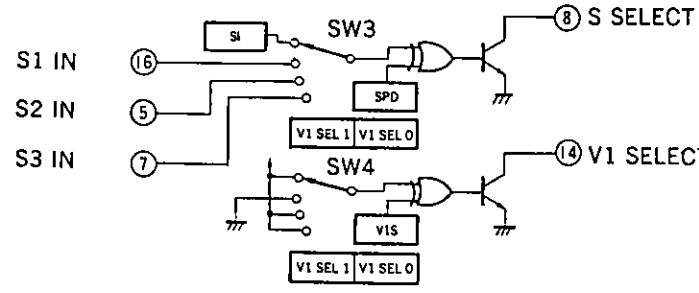
○ CXA1314

V0 SEL 1	V0 SEL 0	S pin select input signal
0	0	SI
0	1	S 1 IN
1	0	S 2 IN
1	1	S 3 IN



○ CXA1414

V1 SEL 1	V1 SEL 0	S pin select input signal
0	0	SI
0	1	S 1 IN
1	0	S 2 IN
1	1	S 3 IN



SPD: Defines the polarity of the control signal output (S SELECT) for the S signal/composite video signal select switch.

S1 to S3/SI	SPD	S SELECT
0	0	1
0	1	0
1	0	0
1	1	1

VIS : When information indicating that video input 1 (VIDEO 1 IN) has been selected at the video output source of Pin 11 (For CXA1314 VIDEO 0 OUT and for CXA1414 VIDEO 1 OUT), this output polarity is defined.
In CXA1314 SW4 is controlled by V0 SEL1 and V0 SEL0 while in CXA1414 it is controlled by V1 SEL 1 and V1 SEL0.

○ CXA1314

V0 SEL1	V0 SEL0	V1S	V1 SELECT
0	1	0	1
		1	0
0	0	0	0
1	*	1	1

○ CXA1414

V0 SEL1	V0 SEL0	V1S	V1 SELECT
1	1	0	1
		1	0
0	0	0	0
1	*	1	1

* S pin information (S1 to S3), S SELECT and V1 SELECT become positive logic as a I^2C bus data.

3. CXA1314/CXA1414 control example

At application circuit example 2 a control instance is shown where S-VIDEO 1 signal is output to Y/C 1 OUT and S-VIDEO 3 signal to Y/C 2 OUT. S information input polarity is at 0.
If switching at SW1 and 2 is executed by flowing in current, polarity at S SELECT output turns to 0.
In the application circuit example, Pin 14 the video 1 select output pin is open but output polarity is set to 1.

	Video input and polarity	
	CXA1314	CXA1414
Video 0 output	Video 1	Video 1
Video 1 output	Video 3	Video 3
S information input	0	0
S select output	0	0
Video 1 Select output	1	1

When input on the above chart is to be selected.

	CXA1314	CXA1414
Video 0 output	101	101
Video 1 output	111	111
polarity	110	101

As this is the control code, transferring the 3 byte data would do.

CXA1314 X 1 0 1 X X X X X 1 1 1 X X X X X 1 1 0 X X X X
CXA1414 X 1 0 1 X X X X X 1 1 1 X X X X X 1 0 1 X X X X
First byte — Second byte — Third byte

(Since X bit is undefined either 1 or 0) that is,

CXA1314

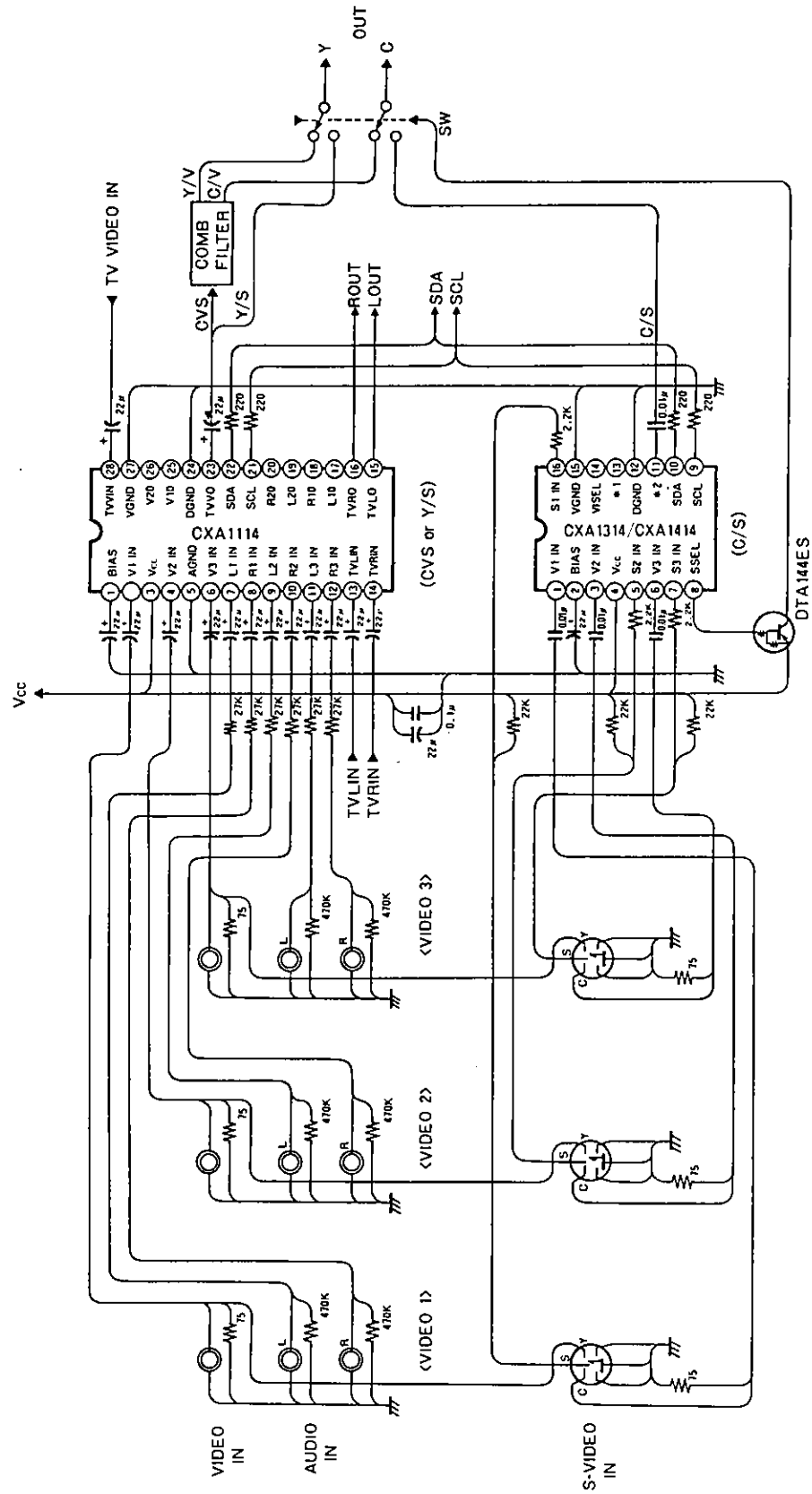
92_H, 50_H, 70_H, 60_H (When X is at 0)
92_H, DF_H, FF_H, EF_H (When X is at 1)

CXA1414

94_H, 50_H, 70_H, 50_H (When X is at 0)
94_H, DF_H, FF_H, DF_H (When X is at 1)

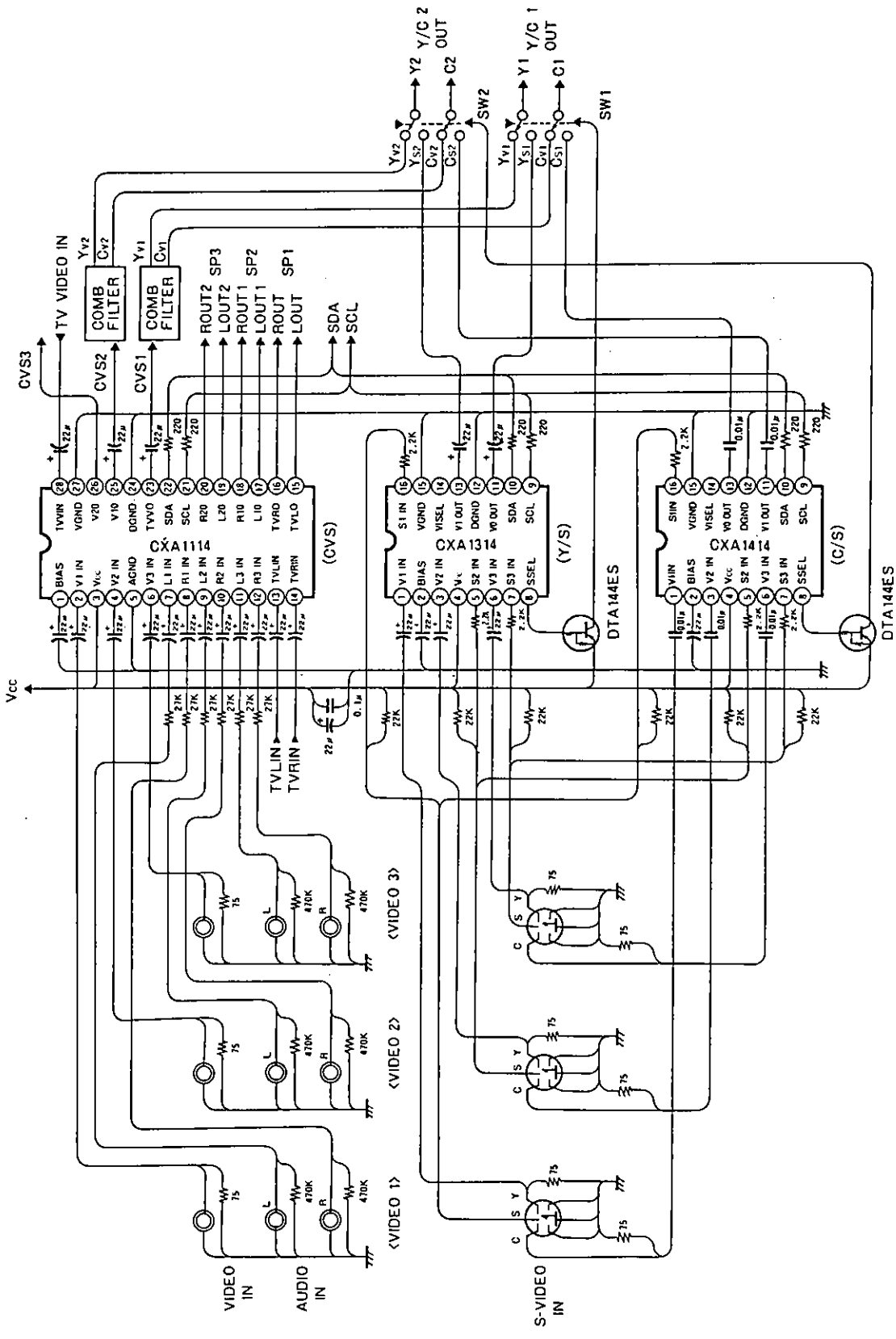
Transferring either data would do.

Application Circuit 1



* 1. CXA1314 : V1 OUT, CXA1414 : V0 OUT
* 2. CXA1314 : V0 OUT, CXA1414 : V1 OUT

Application Circuit 2



Handling Precautions

As CXA1314 and CXA1414 utilize video and digital signals the following points should be taken into consideration.

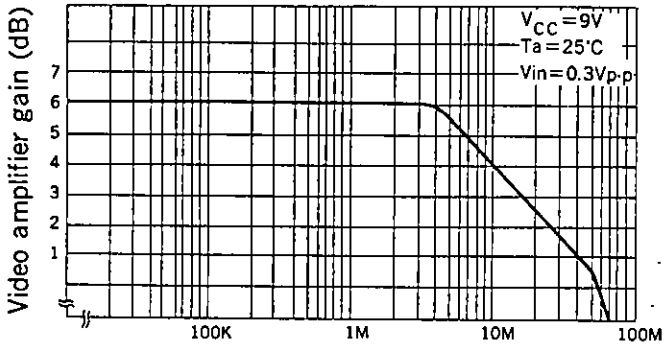
1) On the input side of the video system the wiring may cause crosstalk. An effective measure would be to separate input by utilizing an earth line on the substrate.
2) When control is performed through I²C bus, once it is set on, as long as there is no change in the data (With power off it is called off, however), the condition at which it is set is kept on. To avoid noise caused by SCL, SDA clock, and data transfer, it is recommended to stop the master for a while except during usage.
3) Pin 2 provides bias. By installing a capacitor here effective suppression of supply ripple can be expected. Here the cut off frequency obtained is

$$fo=\frac{1000}{2\pi\times 11\times C(\mu F)}\ [Hz]$$

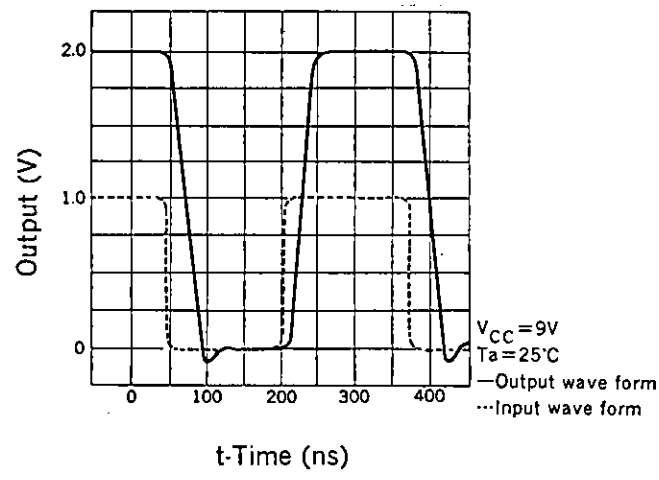
4) Keep the bypass capacitor for the supply near pin 4.

Characteristics Diagram

Video Amplifier vs. Frequency

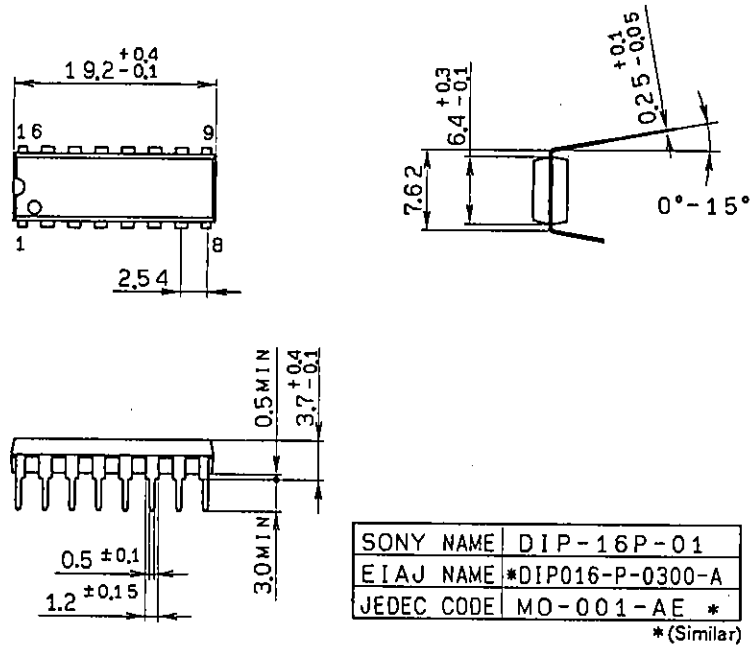


Rectangular wave input vs. Video amplifier output



Package Outline Unit: mm

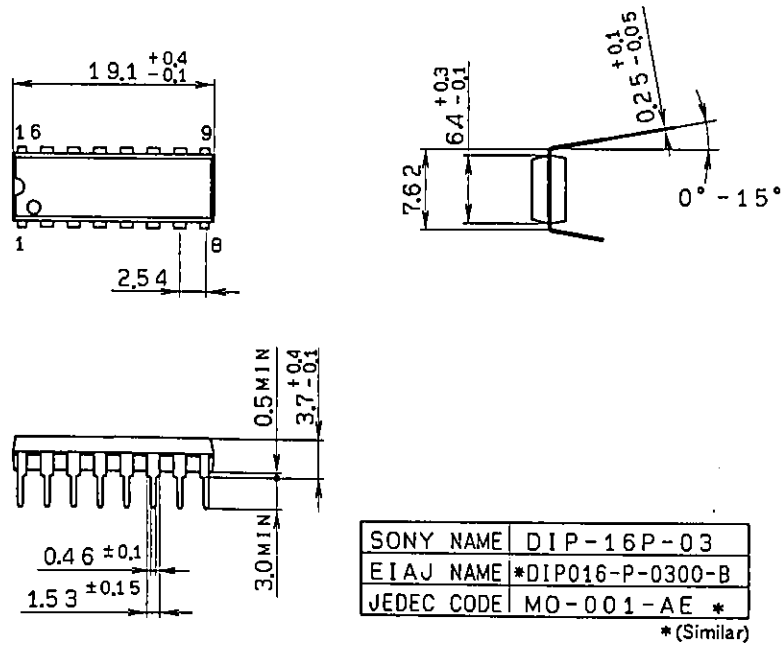
16pin DIP (Plastic) 300mil 1.0g



SONY NAME	DIP-16P-01
EIAJ NAME	*DIP016-P-0300-A
JEDEC CODE	MO-001-AE *

*(Similar)

16pin DIP (Plastic) 300mil



SONY NAME	DIP-16P-03
EIAJ NAME	*DIP016-P-0300-B
JEDEC CODE	MO-001-AE *

*(Similar)