SONY

CXD1179Q

8-bit 35MSPS Video A/D Converter with Clamp Function

Description

The CXD1179Q is an 8-bit CMOS A/D converter for video with synchronizing clamp function. The adoption of 2 step-parallel method achieves ultra-low power consumption and a maximum conversion speed of 35MSPS.

Features

- Resolution: 8-bit ± 1/2LSB (DL)
- Maximum sampling frequency: 35MSPS
- Low power consumption: 80mW (at 35MSPS typ.) (reference current excluded)
- Synchronizing clamp function
- Clamp ON/OFF function
- Reference voltage self bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 5V power supply
- Low input capacitance: 8pF
- Reference impedance: 330Ω (typ.)

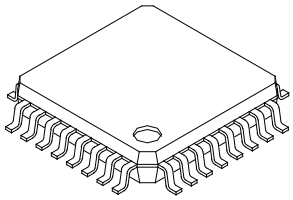
Applications

Wide range of applications that require high-speed A/D conversion such as TV and VCR.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

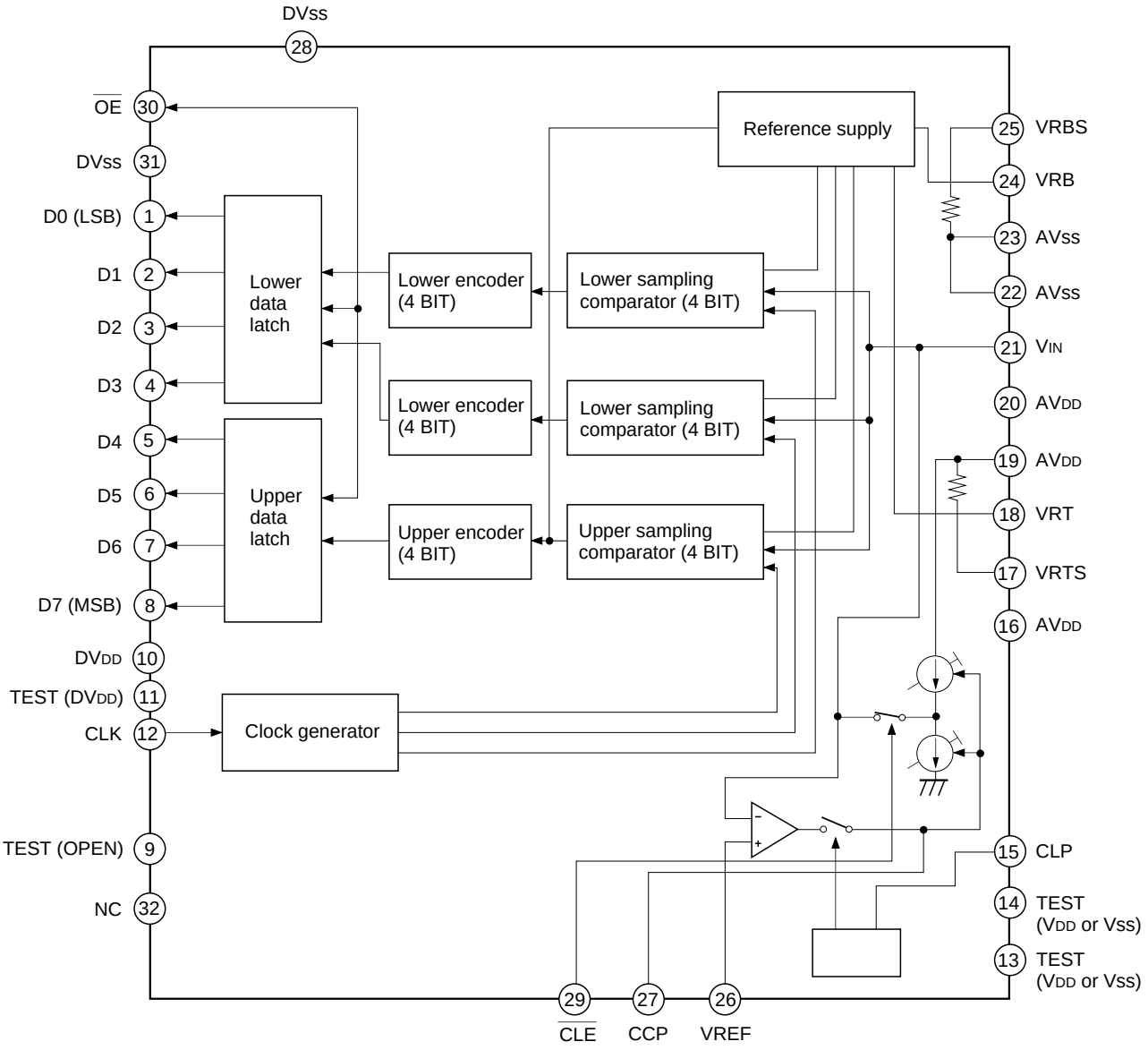
• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (Analog)	V_{IN}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (Digital)	V_I	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Output voltage (Digital)	V_O	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

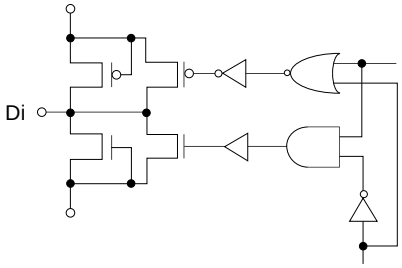
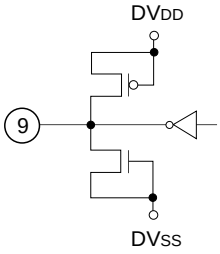
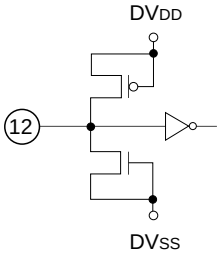
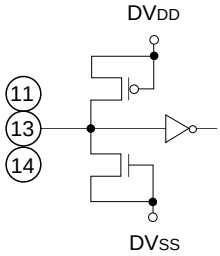
• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}		
	$\lvert DV_{SS} - AV_{SS} \rvert$	0 to 100	mV
• Reference input voltage			
	V_{RB}	0 and above	V
	V_{RT}	2.7 and below	V
• Analog input	V_{IN}	1.8Vp-p above	
• Clock pulse width			
	Tpw_1, Tpw_0	13ns (min) to 1.1µs (max)	
• Operating ambient temperature			
	Topr	–40 to +85	°C

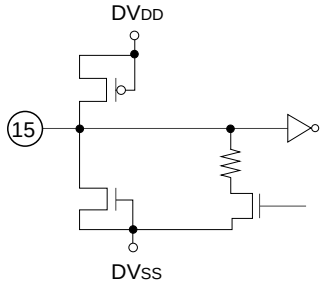
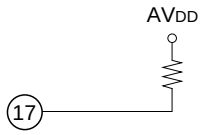
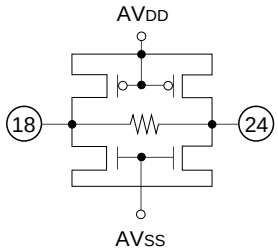
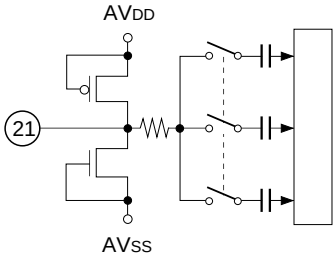
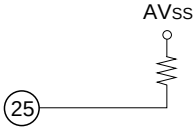
E91Z07F78-PS

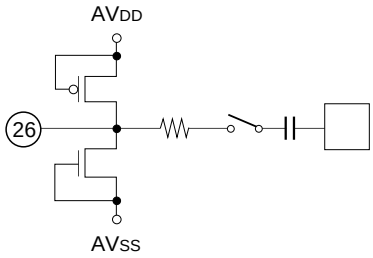
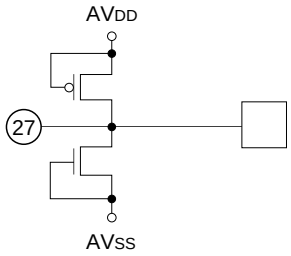
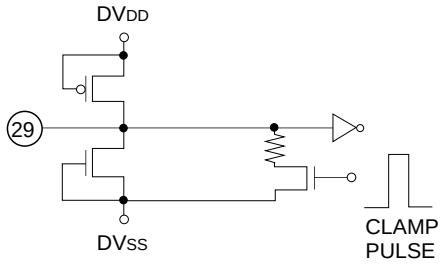
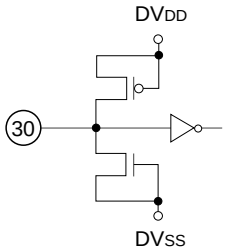
Block Diagram



Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) output
9	TEST		Leave open during normal usage.
10	DVDD		Digital +5V
12	CLK		Clock input
11, 13, 14	TEST		Fix Pin 11 to V_{DD}, Pins 13 and 14 to V_{DD} or V_{SS} during normal usage.

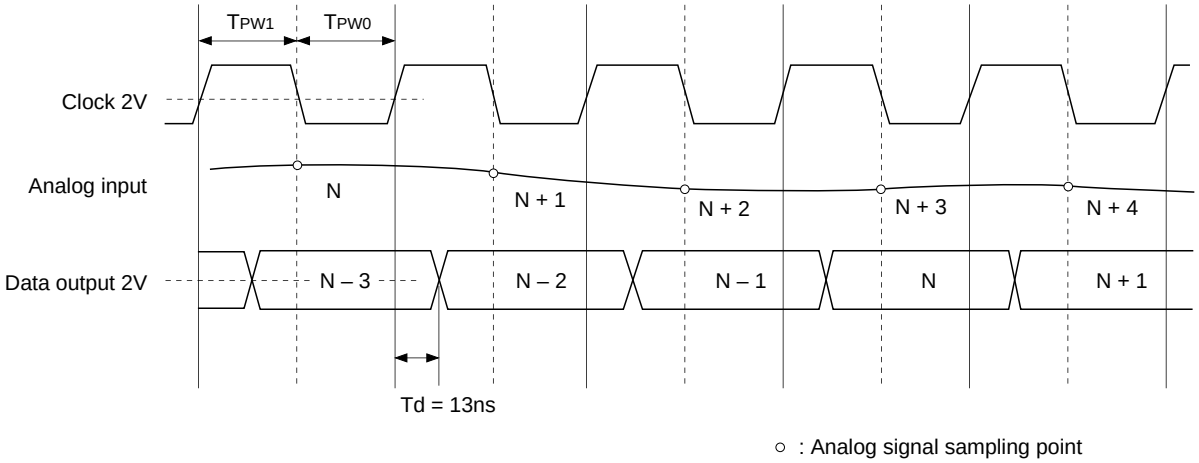
Pin No.	Symbol	Equivalent circuit	Description
15	CLP		Inputs clamp pulse to Pin 15 (CLP). Clamps the signal voltage during Low interval.
16, 19, 20	AVDD		Analog +5V
17	VRTS		Generates approximately +2.6V when shorted with VRT.
18	VRT		Reference voltage (top)
24	VRB		Reference voltage (bottom)
21	VIN		Analog input
22, 23	AVSS		Analog ground
25	VRBS		Generates approximately +0.5V when shorted with VRB.

Pin No.	Symbol	Equivalent circuit	Description
26	VREF		Clamp reference voltage input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in V_{IN} voltage is positive phase.
28, 31	DV_{SS}		Digital ground
29	$\overline{CLE}$		The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is set to off and the converter functions as a normal A/D converter when $\overline{CLE}$ = High. The clamp pulse can be measured by connecting $\overline{CLE}$ to DV_{DD} through a several hundred Ω resistor.
30	$\overline{OE}$		Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High.
32	NC		NC pin

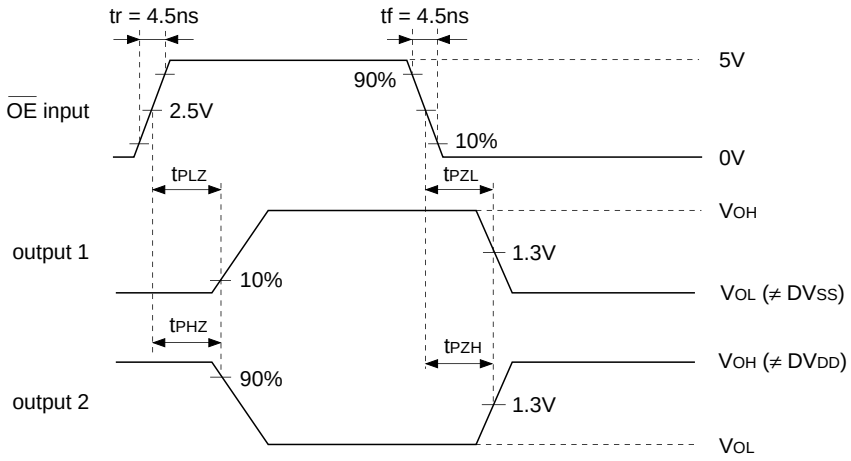
Digital Output

The following table shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
:	:	:
:	127	1 0 0 0 0 0 0 0
:	128	0 1 1 1 1 1 1 1
:	:	:
V_{RB}	255	0 0 0 0 0 0 0 0



Timing Chart I.



Timing Chart II.

Electrical Characteristics

Analog characteristics (Fc = 35MSPS, V_{DD} = 5V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Conversion speed	Fc	V_{DD} = 4.75 to 5.25V Ta = –40 to +85°C V_{IN} = 0.5 to 2.5V f_{IN} = 1kHz ramp		0.5		35	MSPS
Analog input band width (–1dB)	BW	Envelope			25		MHz
Offset voltage*1	E_{OT}	Potential difference to VRT		–60	–40	–20	mV
	E_{OB}	Potential difference to VRB		+55	+75	+95	
Integral non-linearity error	E_L	End point			+0.5	+1.3 –1.0	LSB
Differential non-linearity error	E_D				±0.3	±0.5	
Differential gain error	DG	NTSC 40 IRE mod ramp Fc = 14.3MSPS			1		%
Differential phase error	DP				0.5		deg
Aperture jitter	taj				30		ps
Sampling delay	tsd				2		ns
Clamp offset voltage*2	Eoc	V_{IN} = DC, PWS = 3µs	V_{REF} = 0.5V	–20	0	+20	mV
			V_{REF} = 2.5V	–30	–10	+10	
Clamp pulse delay	tcpd				25		ns

*1 The offset voltage EOB is a potential difference between VRB and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from “00000000” to “00000001”. EOT is a potential difference between VRT and a potential of point where the voltage rises equivalent to 1/2LSB of the voltage when the output data changes from “11111111” to “11111110”.

*2 Clamp offset voltage varies individually. When using with R, G, B 3 channels, color sliding may be generated.

DC characteristics (Fc = 35MSPS, V_{DD} = 5V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current	I_{DD}	Fc = 35MSPS NTSC ramp wave input			16	22	mA
Reference pin current	I_{REF}			4.5	6.1	8.7	mA
Analog input capacitance	C_{IN}	V_{IN} = 1.5V + 0.07Vrms			8		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self-bias I	VRB_1	Shorts VRB and VRBS Shorts VRT and VRTS		0.52	0.56	0.60	V
	$VRT_1 – VRB_1$			1.96	2.10	2.24	
Self-bias II	VRT_2	VRB = AGND Shorts VRT and VRTS		2.13	2.33	2.53	V
Digital input voltage	V_{IH}	V_{DD} = 4.75 to 5.25V Ta = –40 to +85°C		3.5			V
	V_{IL}					0.5	
Digital input current	I_{IH}	V_{DD} = max	$V_{IH} = V_{DD}$			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	$\overline{OE} = V_{SS}$ V_{DD} = min	$V_{OH} = V_{DD} – 0.5V$	–1.1	–2.5		mA
	I_{OL}		V_{OL} = 0.4V	3.7	6.5		
	I_{OZH}	$\overline{OE} = V_{DD}$ V_{DD} = max	$V_{OH} = V_{DD}$			16	µA
	I_{OZL}		V_{OL} = 0V			16	

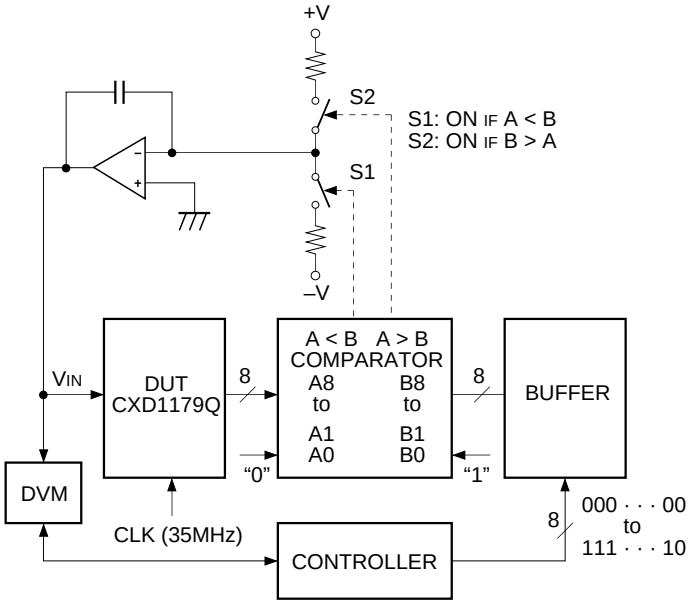
Timing (Fc = 35MSPS, V_{DD} = 5V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output data delay	T_{DL}	With TTL 1 gate and 10pF load V_{DD} = 4.75 to 5.25V Ta = –40 to +85°C	7	13	18	ns
Tri-state output enable time	t_{PZH} t_{PZL}	R_L = 1kΩ, C_L = 15pF $\overline{OE}$ = 5V → 0V V_{DD} = 4.75 to 5.25V Ta = –40 to +85°C	5	8	14	ns
Tri-state output disable time	t_{PHZ} t_{PLZ}	R_L = 1kΩ, C_L = 15pF $\overline{OE}$ = 0V → 5V V_{DD} = 4.75 to 5.25V Ta = –40 to +85°C	4	6.5	11	ns
Clamp pulse width*1	tcpw	Fc = 14MSPS, C_{IN} = 10µF for NTSC wave	1.75	2.75	3.75	µs

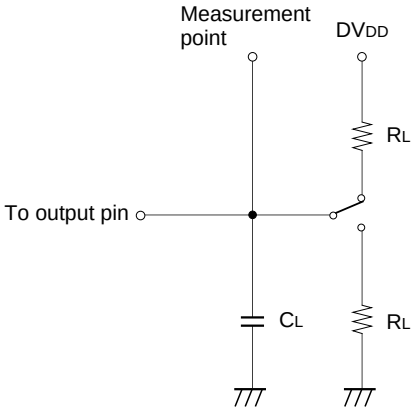
*1 The clamp pulse width is for NTSC as an example. Adjust the rate to the clamp pulse cycle (1/15.75kHz for NTSC) for other processing systems to equal the values for NTSC.

Electrical Characteristics Measurement Circuit

Integral non-linearity error
Differential non-linearity error } **measurement circuit**
Offset voltage

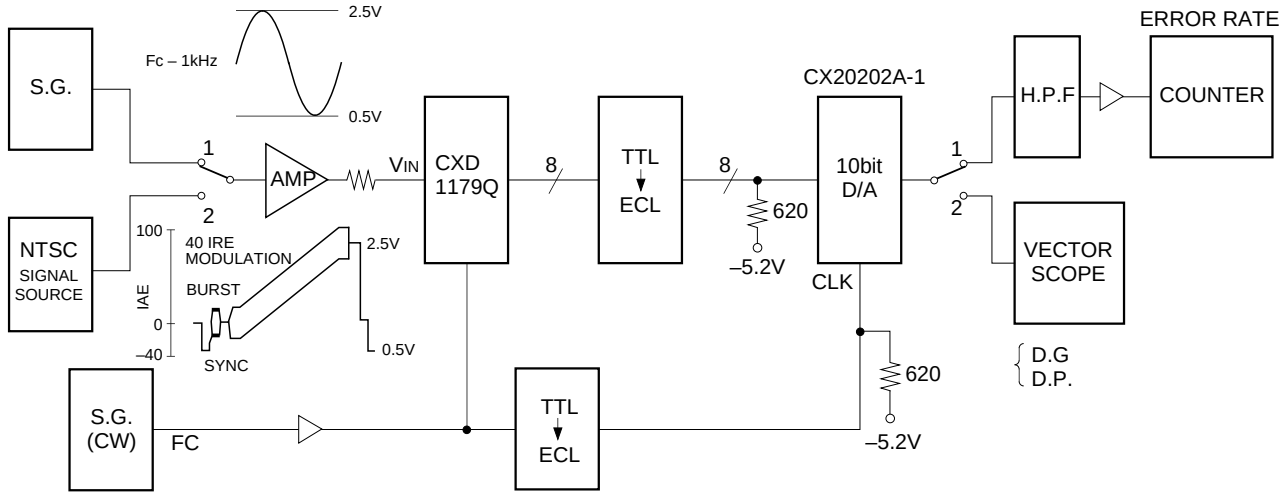


Tri-state output measurement circuit

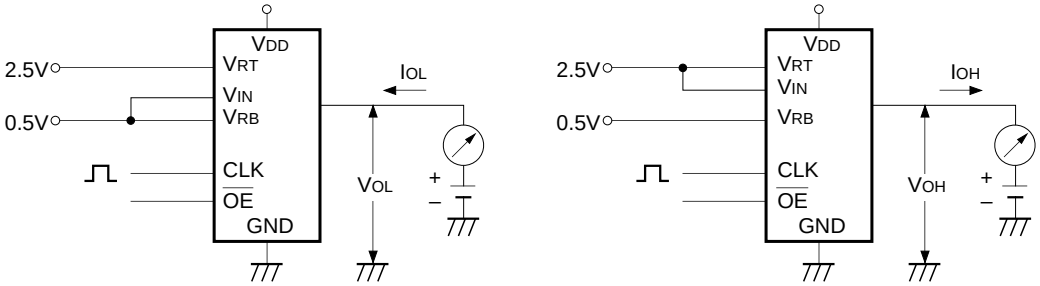


Note) CL includes capacitance of the probe and others.

Maximum operational speed
Differential gain error } **measurement circuit**
Differential phase error

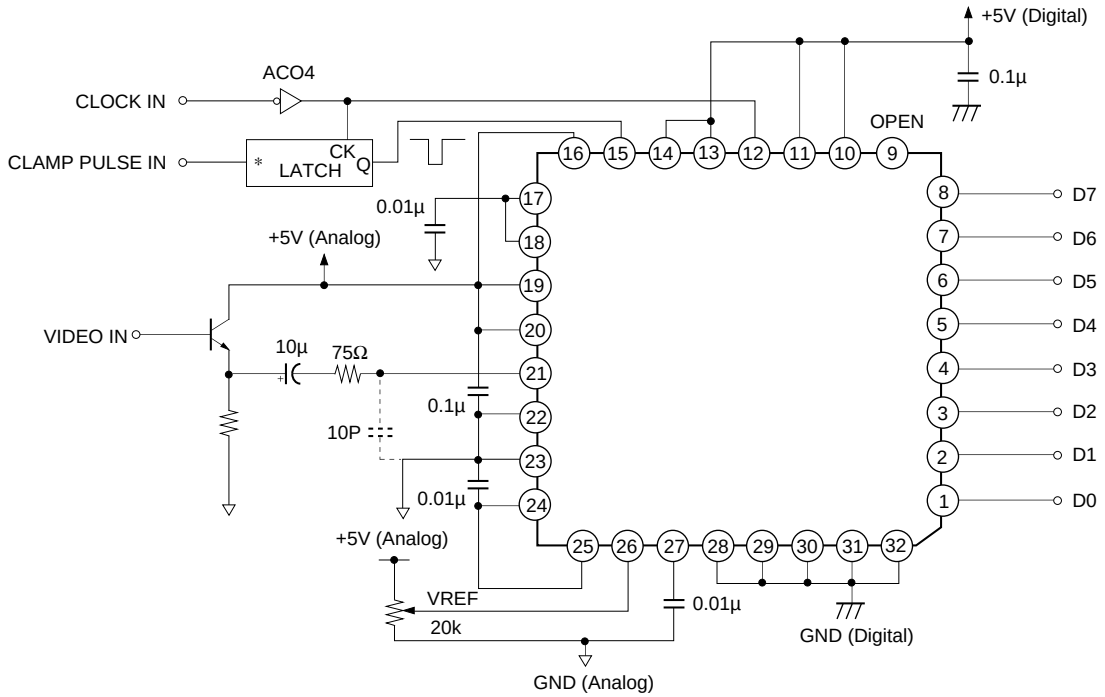


Digital output current measurement circuit



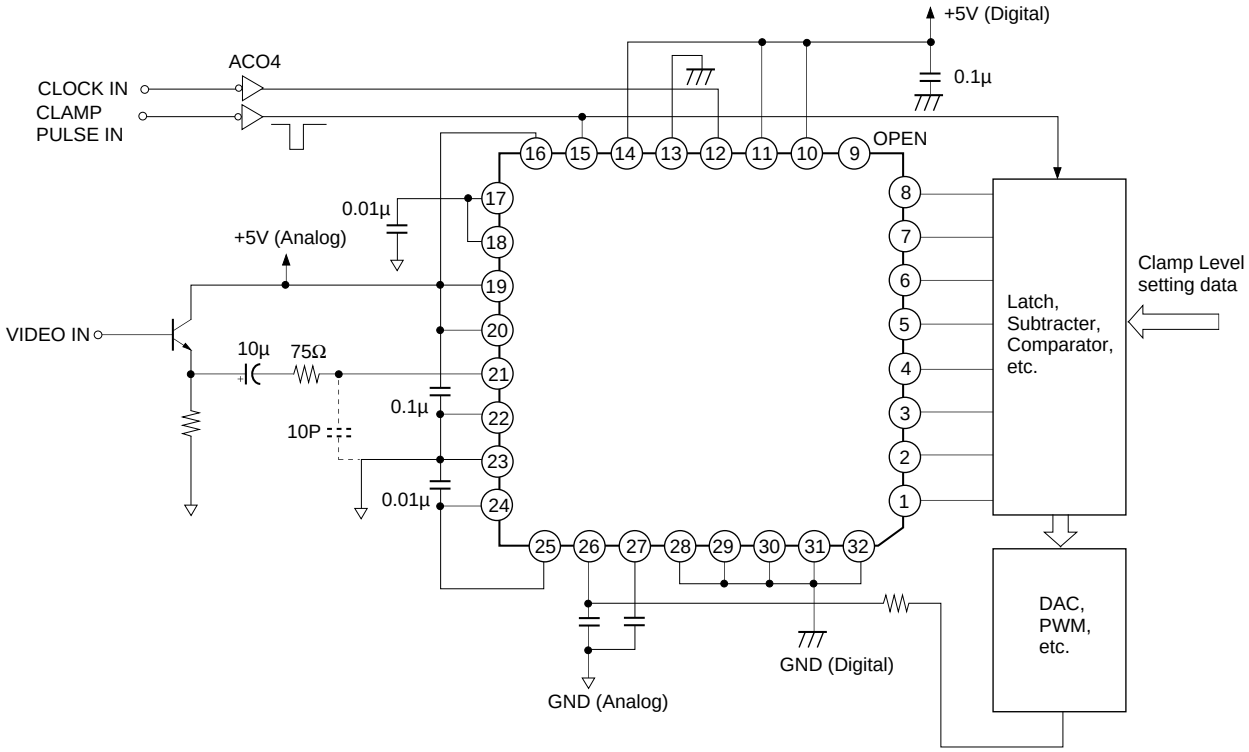
Application Circuit

(1) When clamp is used (self bias used)

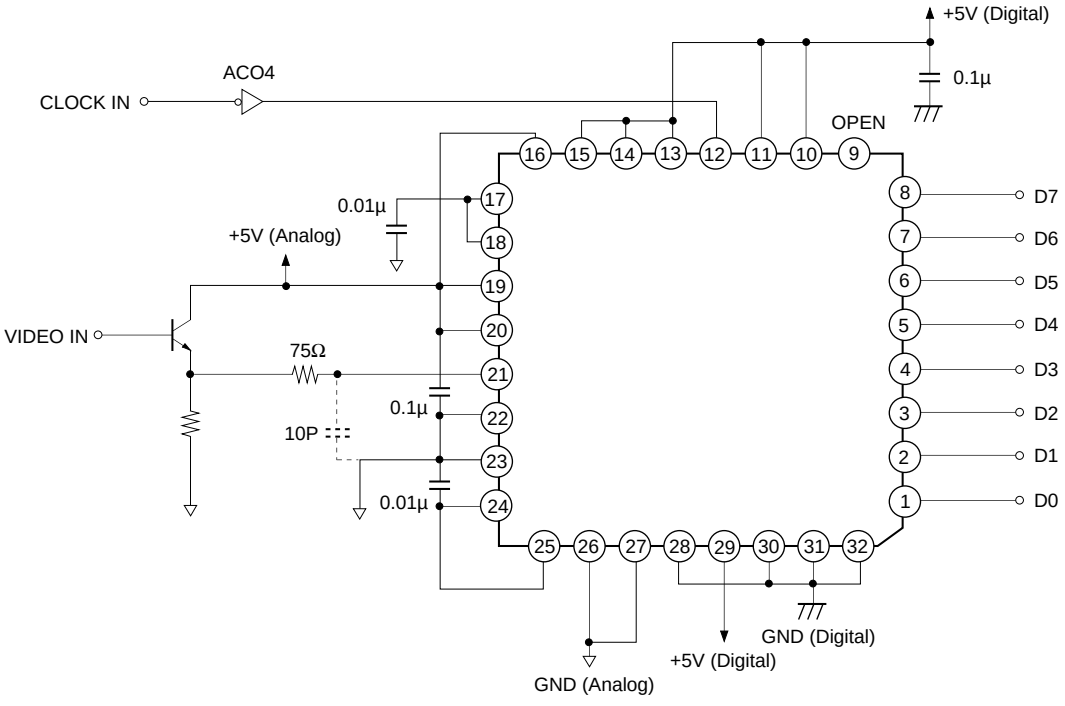


* The clamp pulse is latched by the sampling clock of ADC, but that is not necessary for basic clamp operation. However, slight small beat may be generated as vertical sag according to the relationship between the sampling frequency and the clamp pulse frequency. At such time, the latch circuit is effective in this case.

(2) Digital clamp (self bias used)

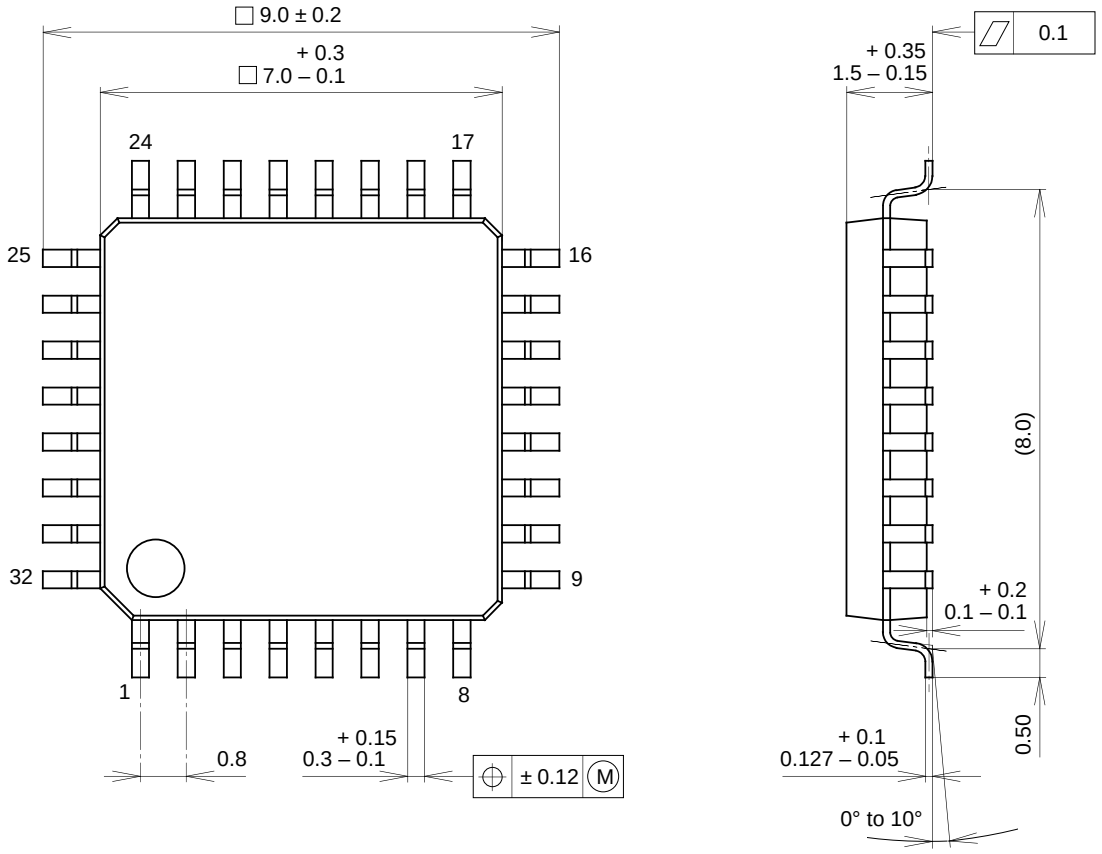


(3) When clamp is not used (self bias used)



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	∗QFP032-P-0707-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g