SONY

CXD2306Q

10-bit 80MSPS 1ch D/A Converter

Description

The CXD2306Q is a 1-ch 10-bit 80MSPS D/A converter for fine monitor and video, and is ideal for high definition TVs and high resolution displays.

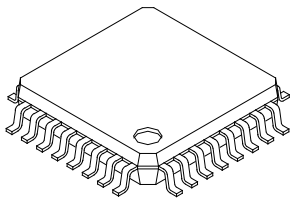
Features

- 10-bit resolution
- Maximum conversion rate 80MSPS
- Differential linearity error ±0.5LSB
- Low power consumption 150mW
  (When 80MSPS 200Ω load, 2Vp-p is output)
- Single 5V power supply
- Built-in independent constant-voltage source

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	5.0 ± 0.25	V
	DV_{DD}, DV_{SS}	5.0 ± 0.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	t_{pw1}	6.25 (min.)	ns
	t_{pw0}	6.25 (min.)	ns
• Operating temperature	topr	–20 to +75	°C

32 pin QFP (PIastic)



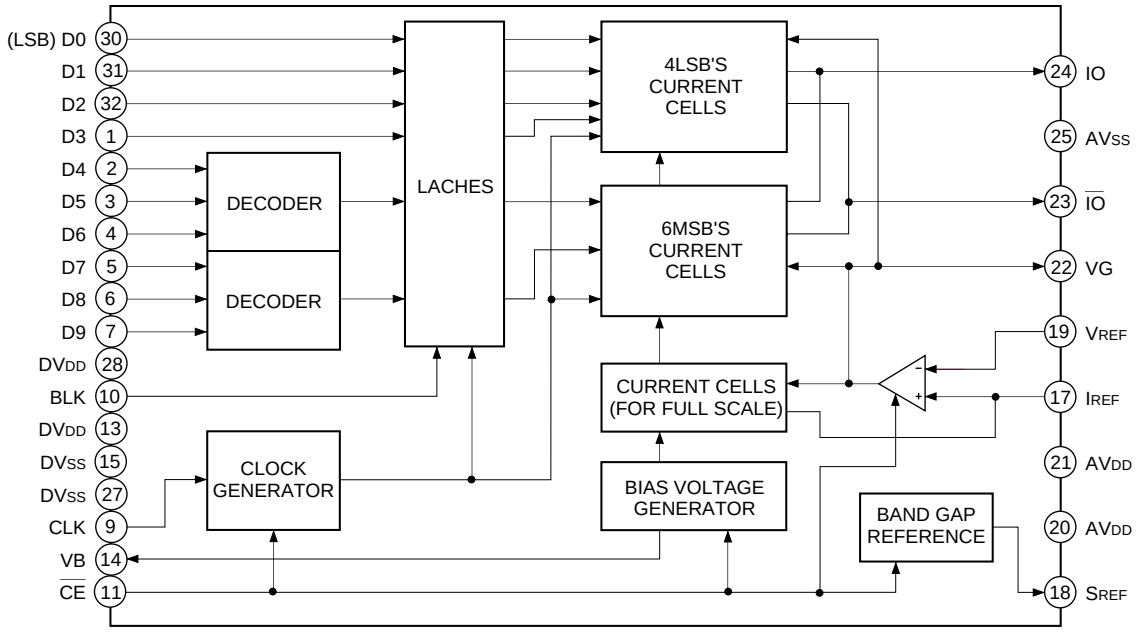
Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

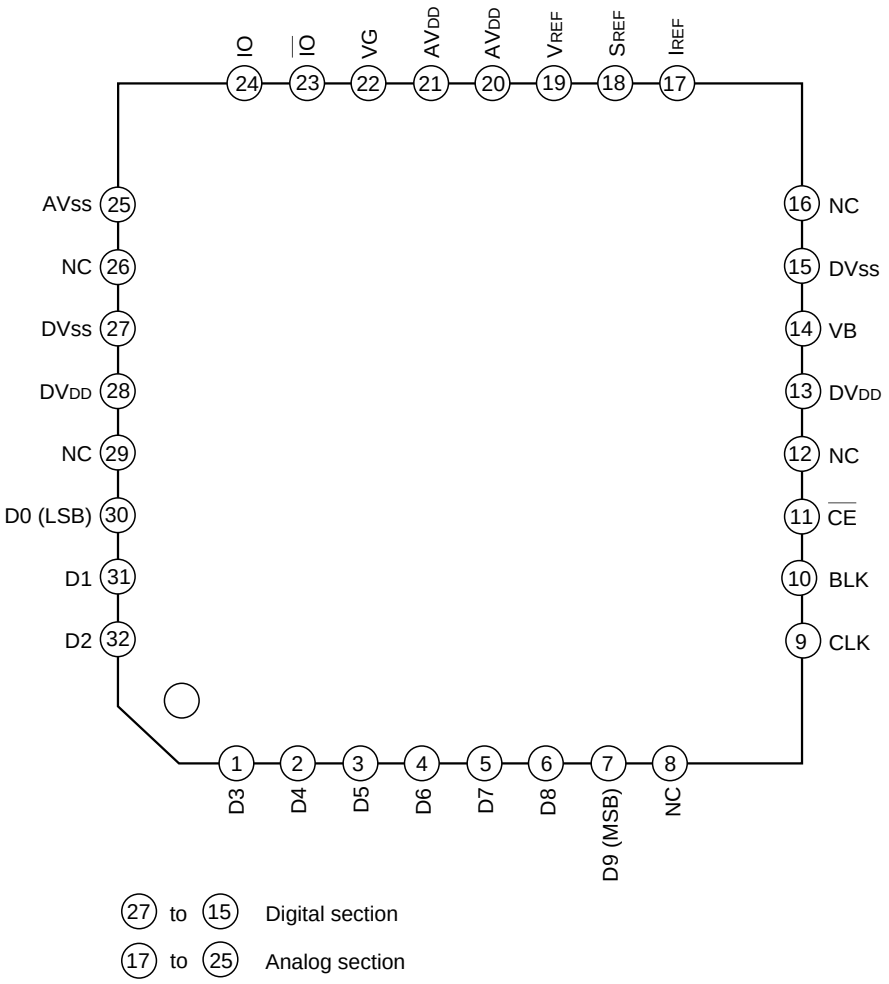
• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

Block Diagram

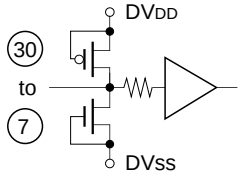
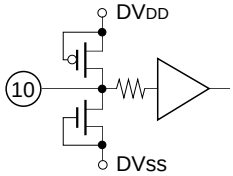
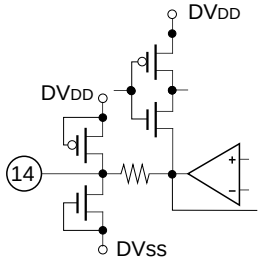
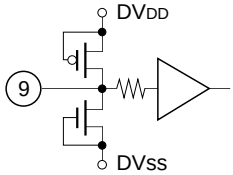
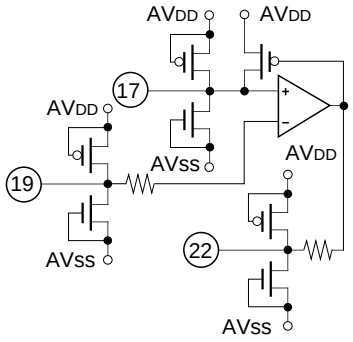


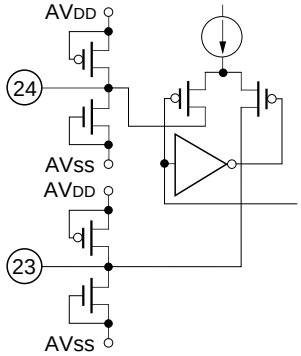
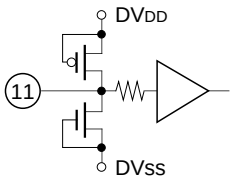
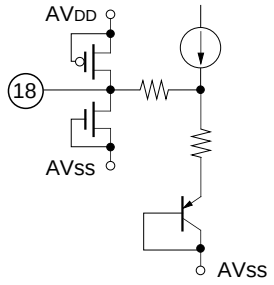
E92X12B7Y

Pin Configuration



Pin Description and Equivalent Circuit

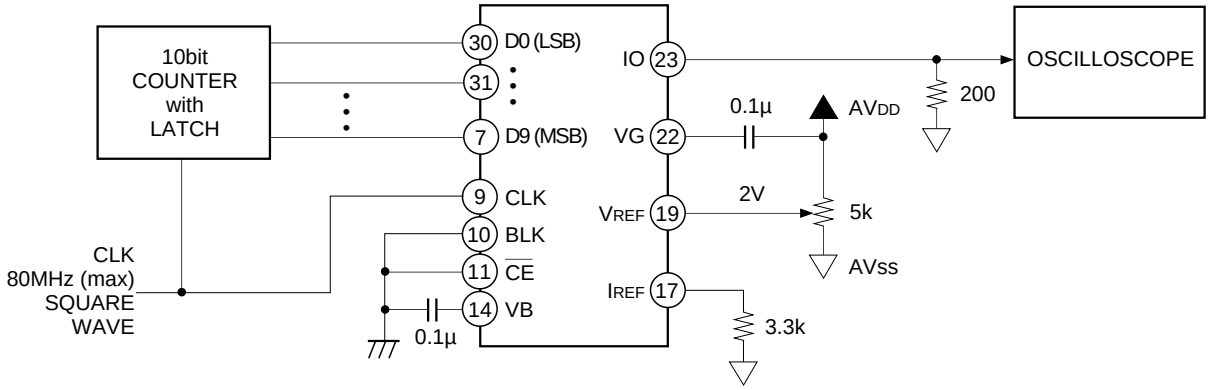
Pin No.	Symbol	Equivalent circuit	Description
30 to 32 1 to 7	D0 to D9		Digital input
10	BLK		Blanking pin. No signal (0V output) at high and output state at low.
14	VB		Connect a capacitor of approximately 0.1µF.
9	CLK		Clock pin
15, 27	DVSS		Digital GND
25	AVSS		Analog GND
17	IREF		Connect resistance “16R” which is 16 times output resistance “R”.
19	VREF		Sets output full scale value.
22	VG		Connect a capacitor of approximately 0.1µF.

Pin No.	Symbol	Equivalent circuit	Description
20, 21	AV_{DD}		Analog V_{DD}
24	IO		Current output pin. Output can be retrieved by connecting resistance. The standard is 200Ω.
23	$\overline{IO}$		Inverted current output pin. Connect to GND normally.
13, 28	DV_{DD}		Digital V_{DD}
11	$\overline{CE}$		Chip enable pin. No signal (0V output) at high makes power consumption minimum.
18	S_{REF}		Independent constant-voltage source output pin using band gap reference. Stable voltage independent of the fluctuation for supply voltage can be get by connecting to V_{REF}. See Application Circuit 2 for details

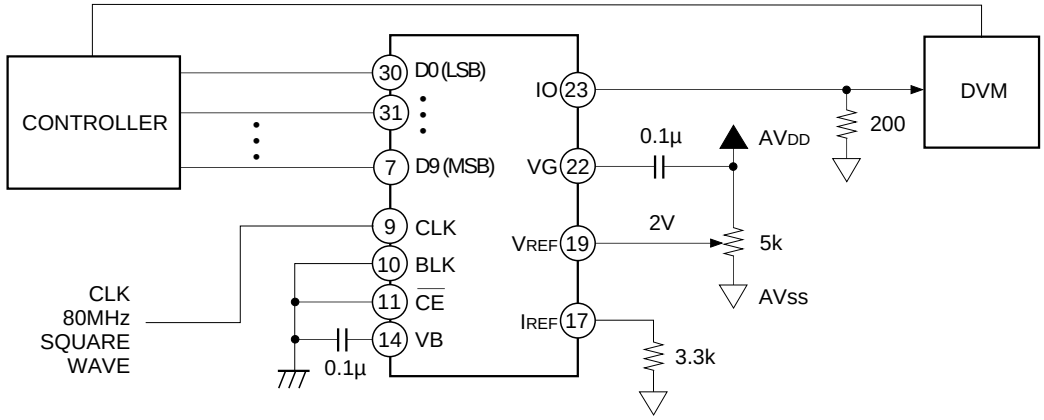
Electrical Characteristics (f_{CLK} = 80MHz, V_{DD} = 5V, R = 200Ω, V_{REF} = 2.0V, 16R = 3.3kΩ, Ta = 25°C)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution		n			10		bit
Maximum conversion rate		f_{MAX}		80			MSPS
Linearity error		EL		–2.0		2.0	LSB
Differential linearity error		ED		–0.5		0.5	LSB
Output full-scale voltage		V_{FS}		1.8	1.92	2.0	V
Output full-scale current		I_{FS}		9.0	9.6	10	mA
Output off-set voltage		V_{OS}				1	mV
Supply current		I_{DD}				30	mA
Digital Input current	High level	I_{IH}				5	µA
	Low level	I_{IL}		–5			µA
Digital Input voltage	High level	V_{IH}		2.15			V
	Low level	V_{IL}				0.85	V
Accuracy guarantee output voltage range		V_{OC}		1.8	1.92	2.0	V
Setup time		ts		5.0			ns
Hold time		th		1.0			ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE	Rout = 100Ω,1Vp-p		50		pV-s
Differential gain		DG			2.5		%
Differential phase		DP			1.3		deg
S_{REF} output voltage		S_{REF}	Ta = 25°C	1.0		1.3	V

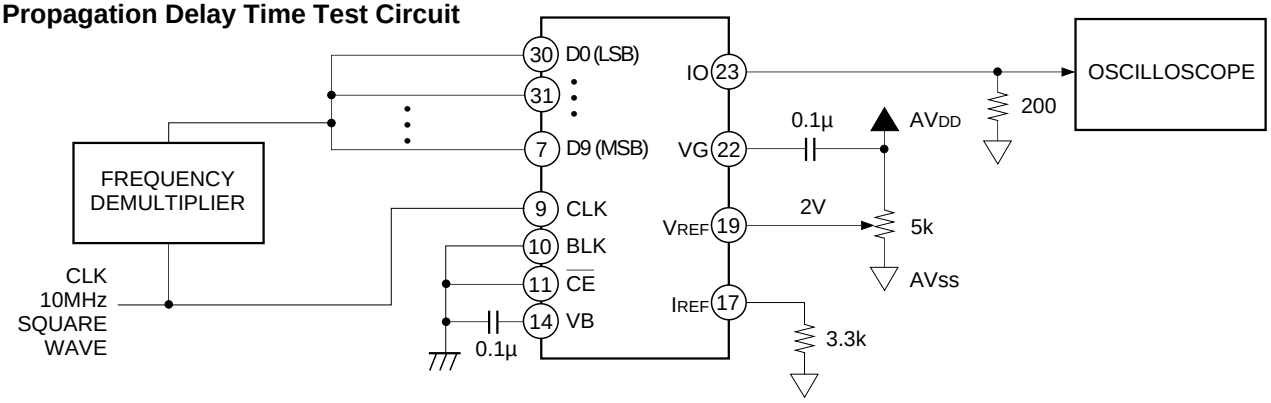
Maximum Conversion Rate Test Circuit



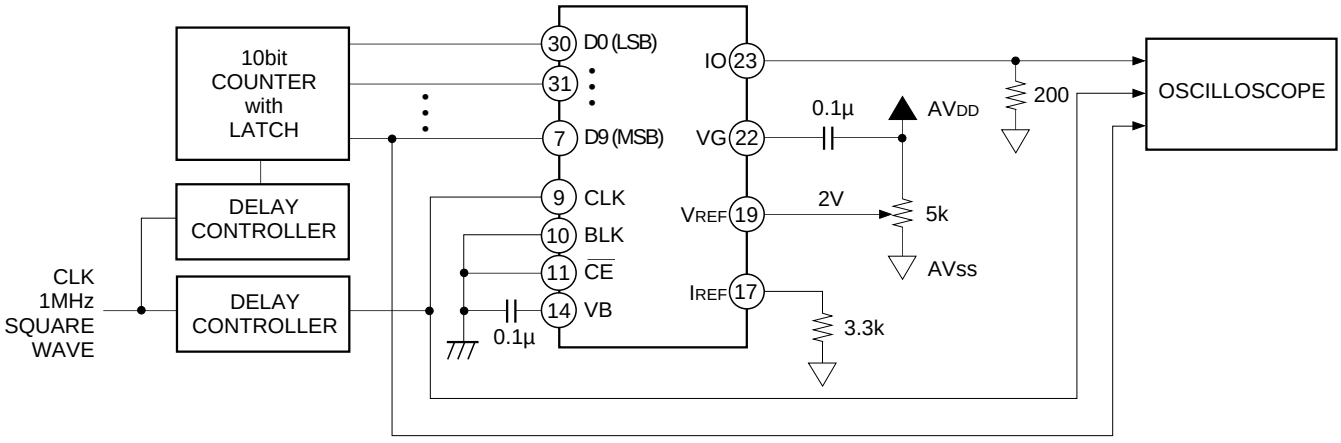
DC Characteristics Test Circuit



Propagation Delay Time Test Circuit

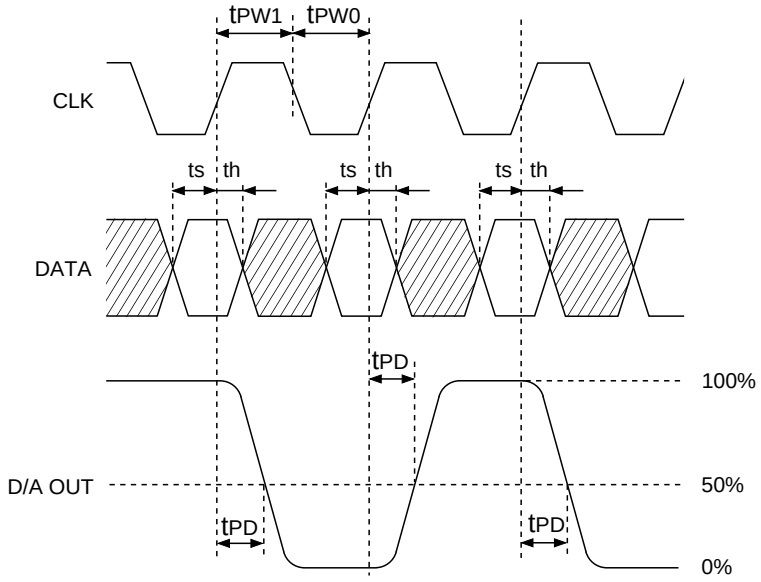


Setup Hold Time and Glitch Energy Test Circuit



Description of Operation

Timing Chart

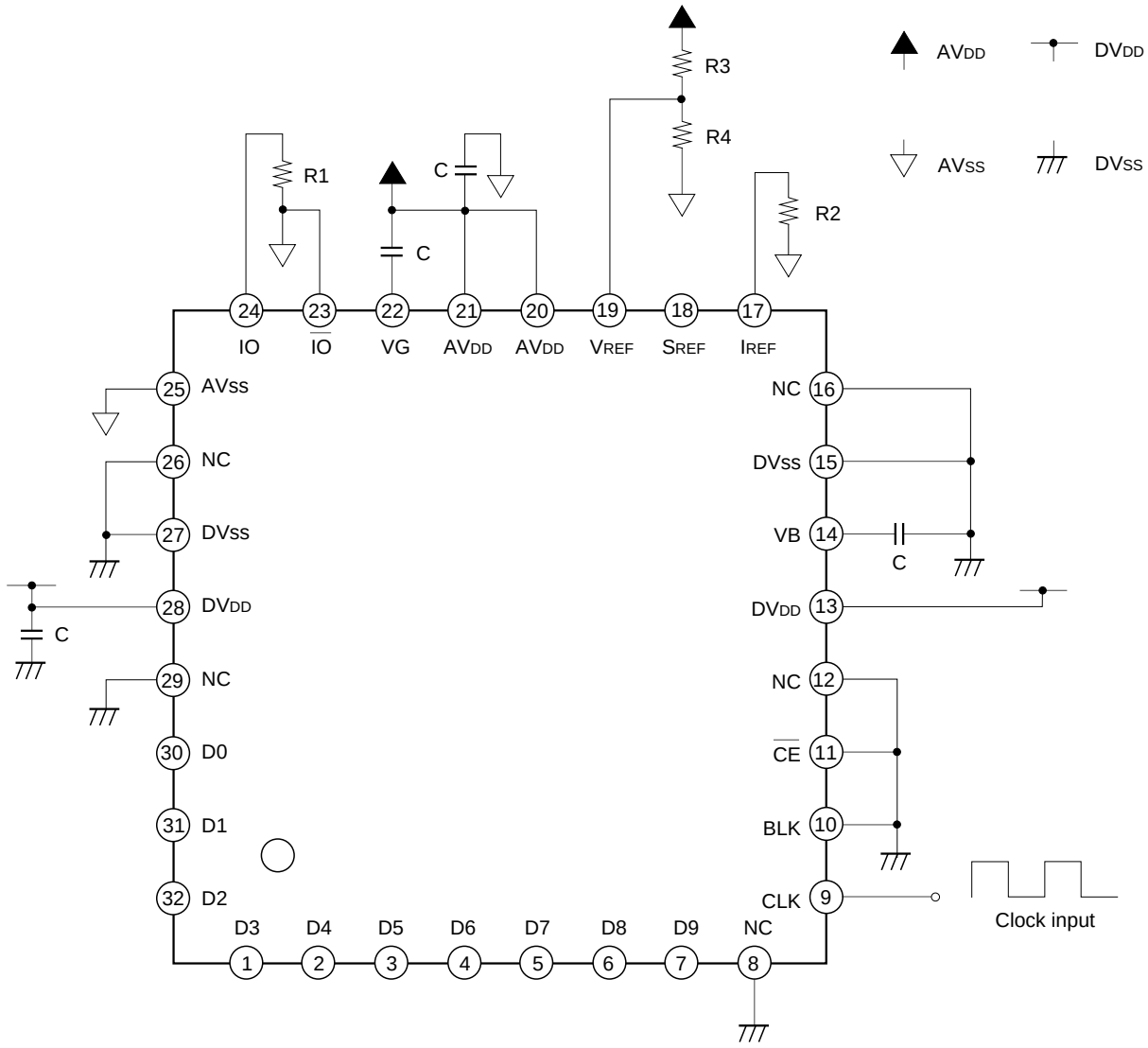


I/O Correspondence Table

(When 2.00V output full-scale voltage)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1 1 1	2.0V
:	
1 0 0 0 0 0 0 0 0 0	1.0V
:	
0 0 0 0 0 0 0 0 0 0	0V

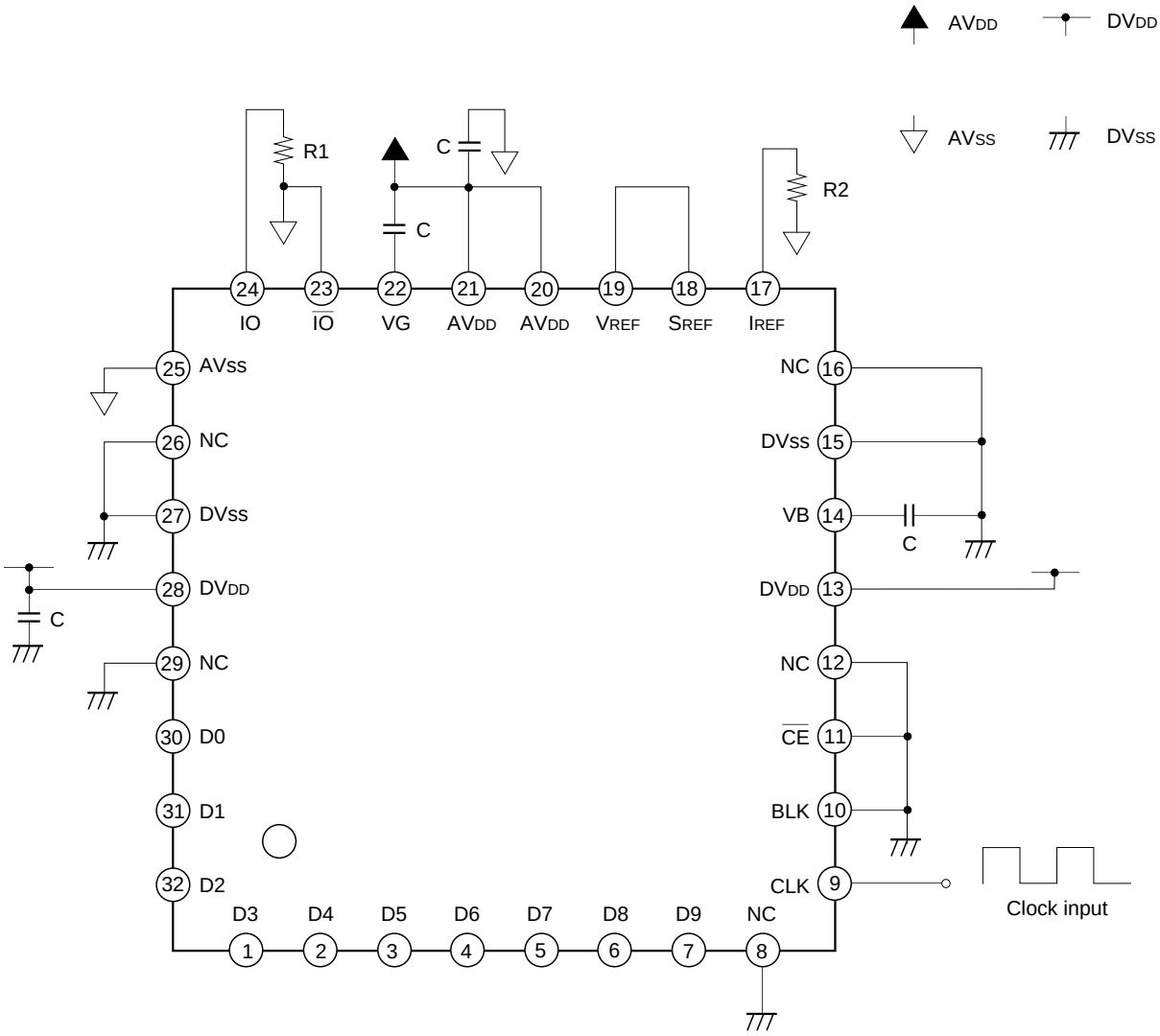
Application Circuit 1



- When 5.0V supply voltage (DV_{DD} and AV_{DD})
- Digital input from Pins 30 to 32 and Pins 1 to 7
- Pin 18 is left open when using normally
- R1 = 200Ω
- R2 = 3.3kΩ (resistance 16 times R1)
- R3 = 3.0kΩ
- R4 = 2.0kΩ
- C = 0.1µF

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2



- When 5.0V supply voltage (DV_{DD} and AV_{DD})
- Digital input from Pins 30 to 32 and Pins 1 to 7
- R1 = 200Ω
- R2 = 2.0kΩ
- C = 0.1µF

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Fig. 1. Output fullscale voltage vs. reference voltage

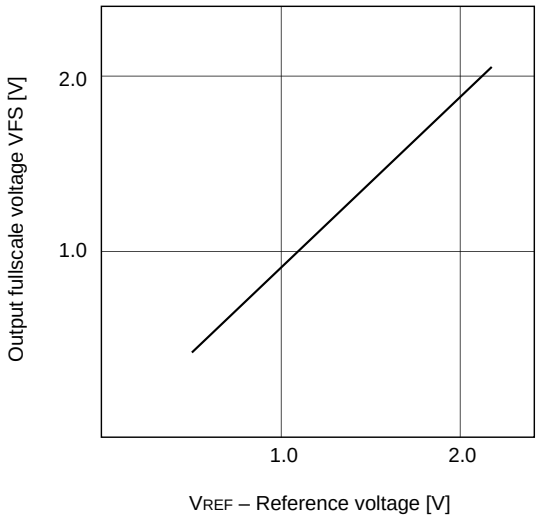


Fig. 2. Output resistance vs. Glitch energy

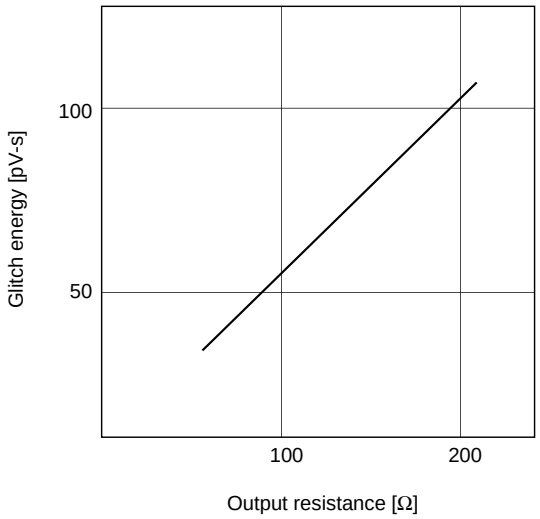


Fig. 3. Output fullscale voltage vs. Ta

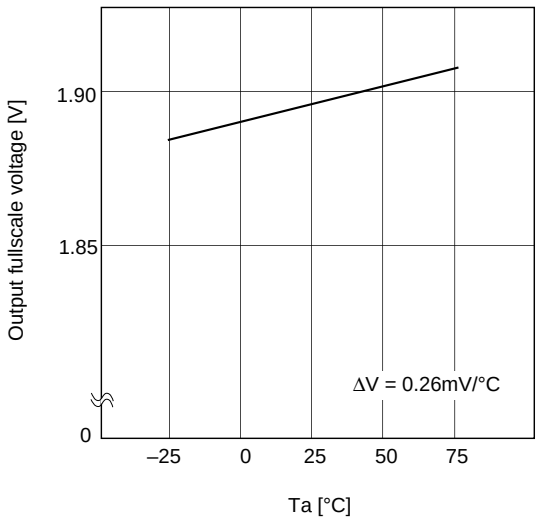


Fig. 4. Output frequency vs. current consumption

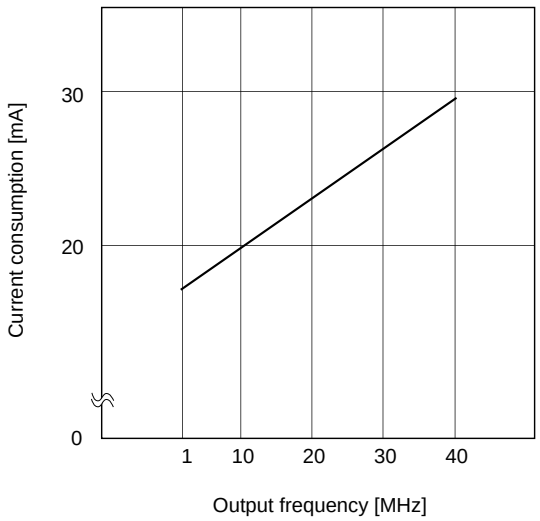
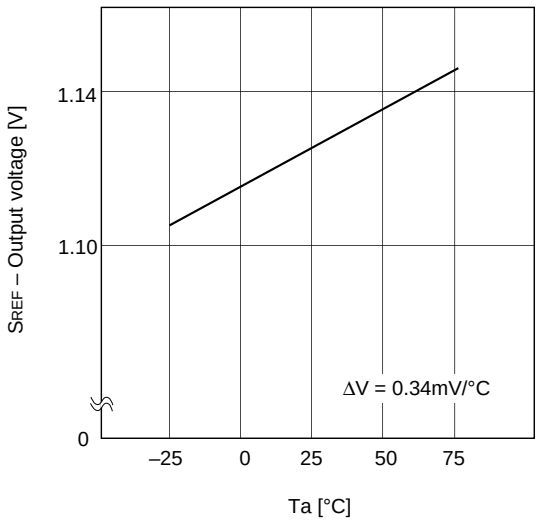


Fig. 5. SREF vs. Ta



Standard masurement conditions and description
- V_{DD} = 5.0V
- V_{REF} = 2.0V
- R1 = 200Ω
- R2 = 3.3kΩ
- Ta = 25°C
- Input data in Fig. 4 = all 0, rectangular wave of all 1, clock freq. = 80MHz.

Notes on Operation

- Selecting the Output Resistance

  CXD2306Q is a current output type D/A converter. To create the output voltage, connect the resistor to the current output terminal.

  Specifications: Output full-scale voltage V_{FS} max = 2.0 [V]
  Output full-scale current I_{FS} max = 10 [mA]

  Calculate the output resistance from $V_{FS} = I_{FS} \times R$. Connect a resistance sixteen times the output resistance to the reference current terminal I_{REF}. In some cases, as this value may not exist, a similar value can be used instead.

  Note that the V_{FS} will be the following.

  $V_{FS} = V_{REF} \times 16\ R/R'$

  R is the resistor to be connected to the IO and R' is the resistor to be connected to the I_{REF}. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the gritty energy and data settling time. Set the best values according to the purpose of use.

- Correlation between Data and Clock

  For CXD2306Q to display the desired performance as a D/A converter, the data transmitted from outside and the clock must be synchronized properly. Adjust the setup time (ts) and hold time (th) as specified in "Electrical Characteristics".

- V_{DD}, V_{SS}

  Separate the analog and digital signals around the device to reduce noise effects. Bypass the V_{DD} terminal to each GND with a 0.1µF ceramics capacitor as near as possible to the terminal for both the digital and analog signals.

- Latch up

  The AV_{DD} and DV_{DD} terminals must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two terminals when the power is turned on.

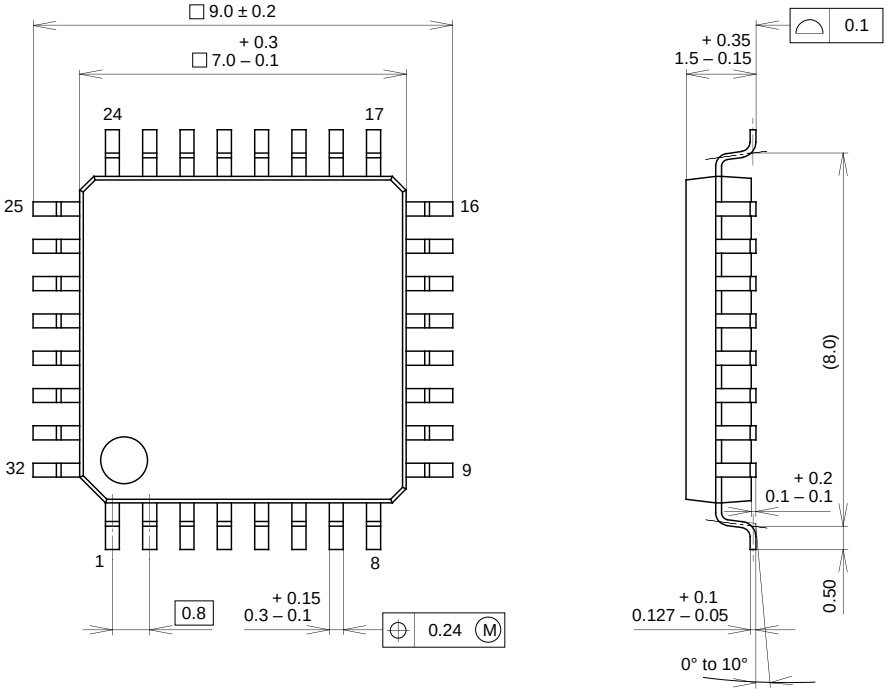
- S_{REF}

  The S_{REF} is an independent regulated current source. By connecting it to the V_{REF}, stable output amplitudes that do not depend on fluctuations in the power supply can be obtained.

  In this case, as $V_{FS} = S_{REF} \times 16R/R'$, set the V_{FS} according to R'.

Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g