SONY

CXD8302Q

PLL for CCD Cameras

Description

The CXD8302Q has the functions needs to configure a PLL circuit with a timing generator and external sync signals for a CCD of 480K pixels (EIA, effective pixels) and 570K pixels (CCIR, effective pixels).

Features

- EIA and CCIR compatible
- Compatible with component digital and composite digital recording format
- Both SYNC and VD/HD signals can be used for external sync signals

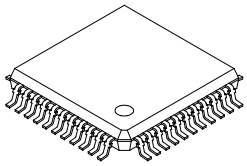
Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.3 to +7	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	0 to 70	°C

44 pin QFP (Plastic)



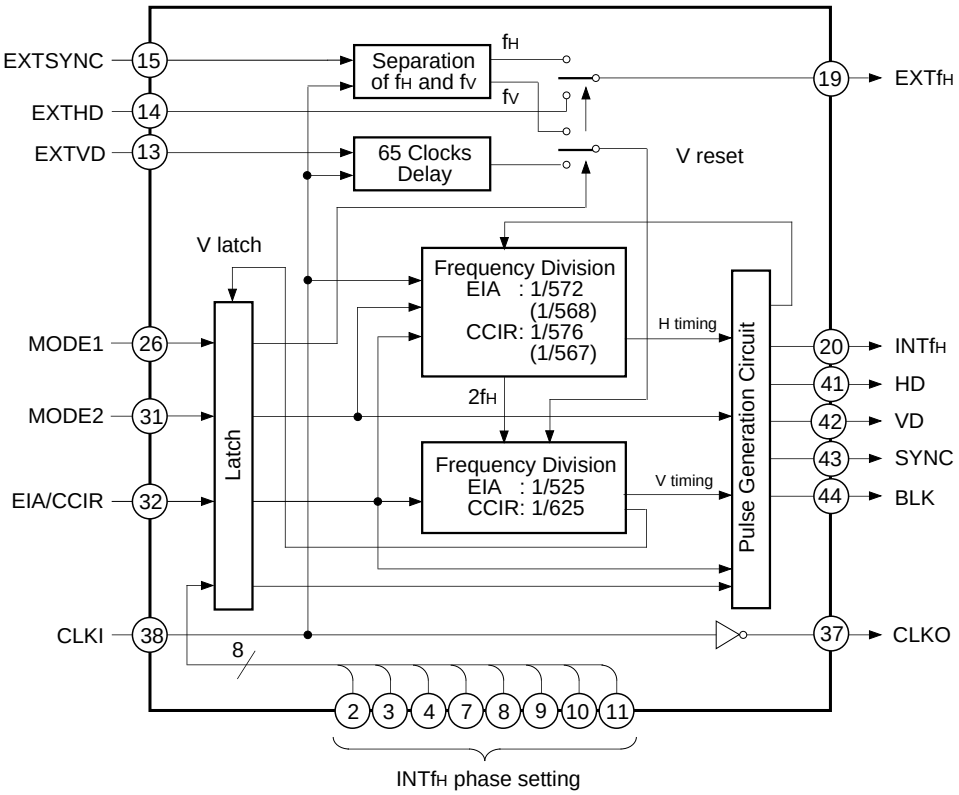
Applications

CCD cameras

Structure

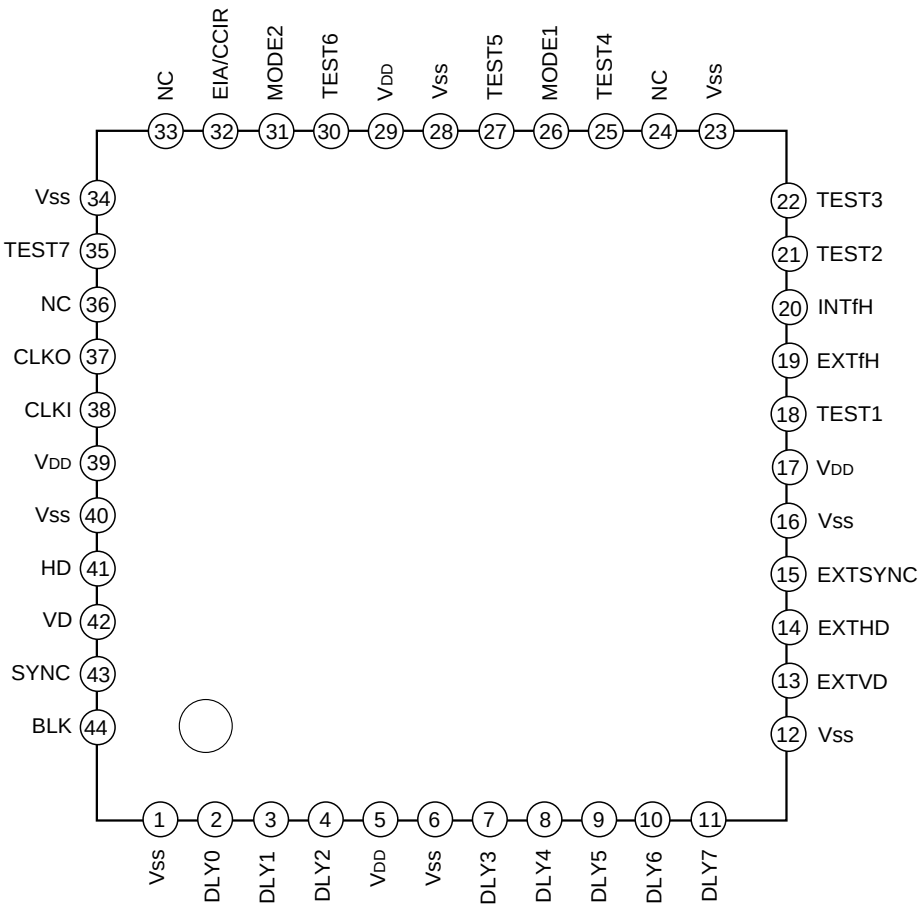
Silicon gate CMOS IC

Block Diagram



E94320A52-PP

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	
1	V_{SS}	—		
2	DLY0	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
3	DLY1	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
4	DLY2	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
5	V_{DD}	—		
6	V_{SS}	—		
7	DLY3	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
8	DLY4	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
9	DLY5	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
10	DLY6	I	Pin 20 (INTf_H) phase setting.	(With pull-up resistor)
11	DLY7	I	Pin 20 (INTf_H) phase setting (MSB).	(With pull-up resistor)
12	V_{SS}	—		
13	EXTVD	I	External VD input.	(With pull-up resistor)
14	EXTHD	I	External HD input.	(With pull-up resistor)
15	EXTSYNC	I	External SYNC input.	(With pull-up resistor)
16	V_{SS}	—		
17	V_{DD}	—		
18	TEST1	O	Test output (normally OPEN).	
19	EXTf_H	O	External f_H output.	
20	INTf_H	O	Internal f_H output.	
21	TEST2	O	Test output (normally OPEN).	
22	TEST3	O	Test output (normally OPEN).	
23	V_{SS}	—		
24	NC	—		
25	TEST4	I	Test input (normally High).	(With pull-up resistor)
26	MODE	I	High: SYNC sync mode, Low: VD/HD sync mode.	(With pull-up resistor)
27	TEST5	I	Test input (normally Low).	(With pull-down resistor)
28	V_{SS}	—		
29	V_{DD}	—		
30	TEST6	I	Test input (normally High).	(With pull-up resistor)
31	MODE2	I	High: Component digital mode, Low: Composite digital mode.	(With pull-up resistor)
32	EIA/CCIR	I	High: EIA mode, Low: CCIR mode.	(With pull-up resistor)
33	NC	—		
34	V_{SS}	—		
35	TEST7	O	Test output (normally OPEN).	
36	NC	—		
37	CLKO	O	Inversed output of CLKI.	

Pin No.	Symbol	I/O	Description
38	CLKI	I	Clock input (from timing generator).
39	V_{DD}	—	
40	V_{SS}	—	
41	HD	O	Horizontal sync signal output.
42	VD	O	Vertical sync signal output.
43	SYNC	O	Sync signal output.
44	BLK	O	Blanking pulse output.

Electrical Characteristics

1) DC characteristics (V_{DD} = 5V ± 0.25V, Topr = 0 to 70°C, V_{SS} = 0V)

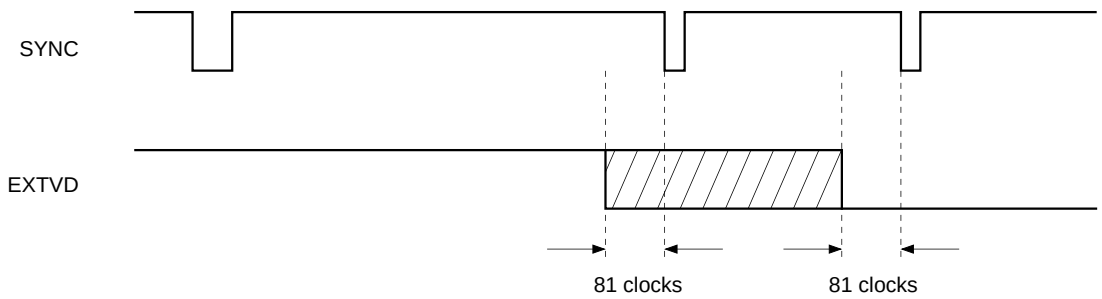
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	High	V_{IH}		0.7V_{DD}			V
	Low	V_{IL}				0.3V_{DD}	V
Input current 1 (Input pins other than those below)		$I_{IN}1$		–10	±1	10	µA
Input current 2 (Input pins with pull-up resistor)		$I_{IN}2$	$V_I = V_{DD}$	10	35	120	µA
Input current 3 (Input pins with pull-down resistor)		$I_{IN}3$	$V_I = V_{SS}$	–8	–30	–100	µA
Output voltage	High	V_{OH}	I_{OH} = –2mA	2.4	4.5		V
	Low	V_{OL}	I_{OL} = 4mA		0.2	0.4	V

2) AC characteristics

Vertical reset in VD/HD sync mode

The phase of EXTVD should be input as shown in the diagram below against the first equivalent pulse during vertical blanking period.

(Take care as the following conditions might not be satisfied depending on the phase setting of INTf_H if the phases are locked when the falling phase shifts a lot between EXTf_H and INTf_H.)



The EXTVD should fall at the timing shown with the slashes.

3) I/O pin capacitance (V_{DD} = 5V ± 0.25V, Topr = 0 to 70°C, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}		2.0		pF
Output pin capacitance	C_{OUT}		4.0		pF

Description of Operation

1) Operation overview

• Functions as sync signal generator
Each of f_H (INTf_H), VD, HD, SYNC, and BLK pulses is generated from clocks input by the timing generator. These pulses are generated by free running if external sync signals are not input.

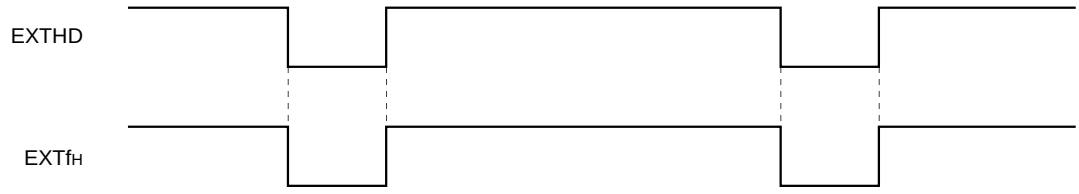
• External synchronization function (PLL)
When the SYNC (EXTSYNC) or VD/HD (EXTVD/EXTHD) external sync signal is input, the vertical reset is compulsorily triggered on each of the f_H (INTf_H), VD, HD, SYNC, and BLK pulses, and f_H (EXTf_H) is simultaneously generated according to the external sync signal. Phase comparison is done externally between INTf_H and EXTf_H and a PLL circuit is configured, then the timing generator is synchronized with an external sync signal.

2) Mode setting

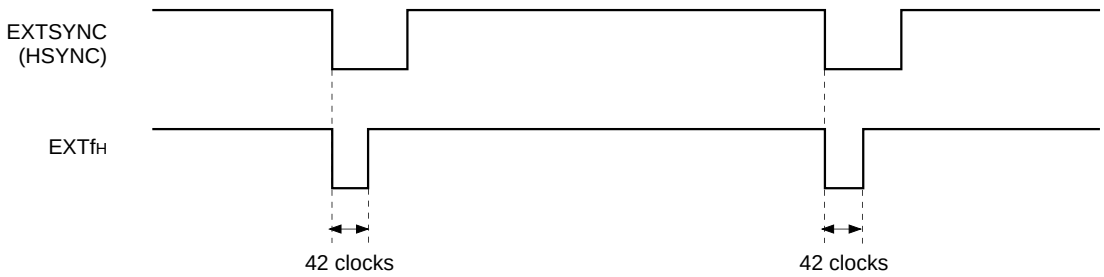
Symbol	Pin No.	L	H
EIA/CCIR	32	CCIR	EIA
MODE1	26	VD/HD sync mode: EXTVD/EXTHD is used as the external sync signal, and the EXTHD signal becomes EXTf_H.	SYNC sync mode: EXTSYNC is used as the external sync signal, and the EXTf_H is obtained by separating it from EXTSYNC
MODE2	31	Composite digital mode; Clock frequency input by timing generator EIA 17.897725MHz (1137.5f_H = 5fsc) CCIR 17.734475MHz (1135 + 4/625f_H = 4fsc)	Component digital mode: Clock frequency input by timing generator EIA 18MHz (1144f_H) CCIR 18MHz (1152f_H)

The phase relationship between external sync and EXTf_H in each sync mode is shown below.

• VD/HD sync mode
The rise and fall timings of EXTHD signal are directly reflected on EXTf_H.



• SYNC synchronous mode
The fall timing of EXTSYNC is the fall timing EXTf_H, but the rise timing of EXTf_H is generated by counting the number of clocks input by the timing generator. Therefore, make sure to compare phases of fall timing of between EXTf_H and INTf_H for PLL configuration in the SYNC synchronous mode.

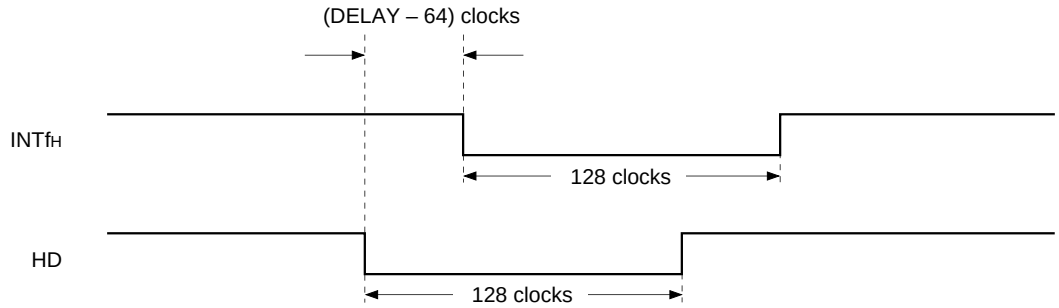


3) INTf$_H$ phase setting

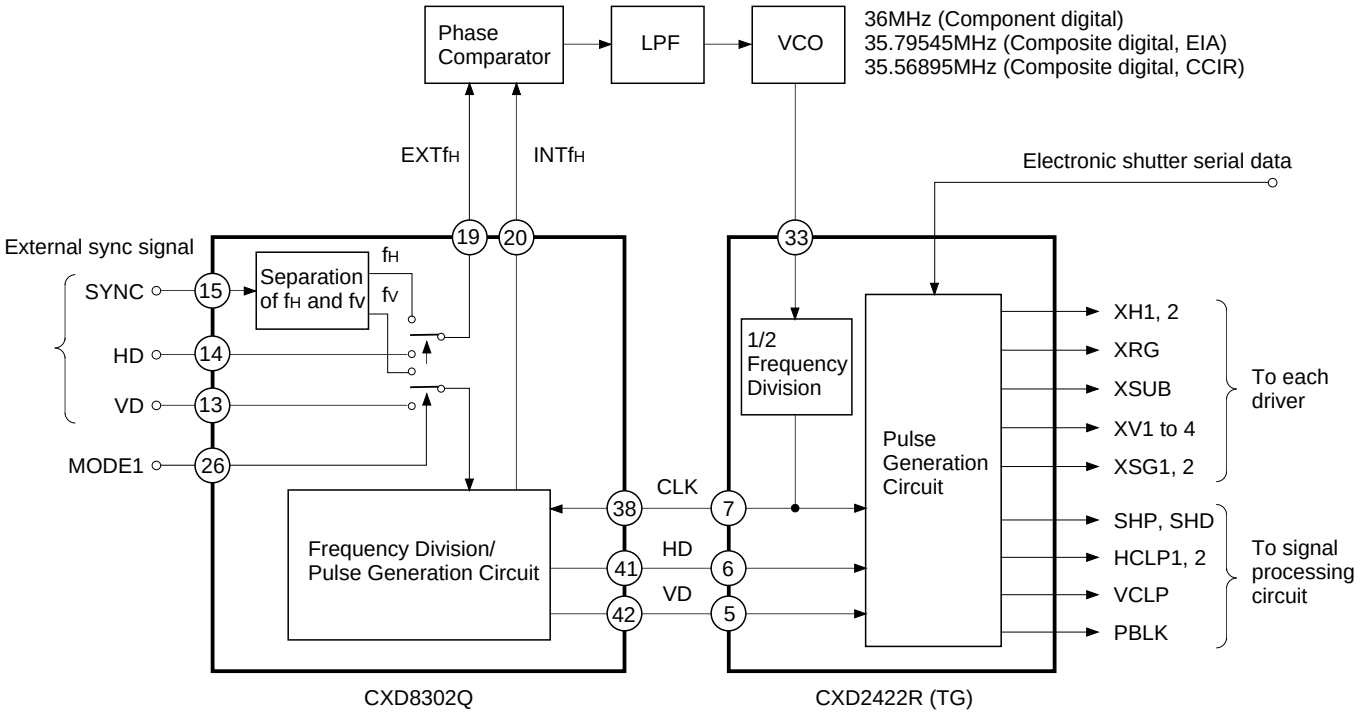
In either VD/HD or SYNC sync mode, the INTf$_H$ phase should be adjusted in line with the phase variance of EXTf$_H$, which forms the reference for phase comparison. The INTf$_H$ phase may be adjusted against VD, HD, SYNC and BLK pulses using DLY0 to DLY7, respectively. (The state of INTf$_H$ and EXTf$_H$ phases fixed by PLL leads to phase adjustment of VD, HD, SYNC, and BLK pulse against the external sync signal.)

The INTf$_H$ is set to the phase being delayed (DELAY-64) clocks from that of HD.

DELAY = 0 to 255: to be set in 8-bit binary with DLY7 as MSB. High: 1, low: 0.



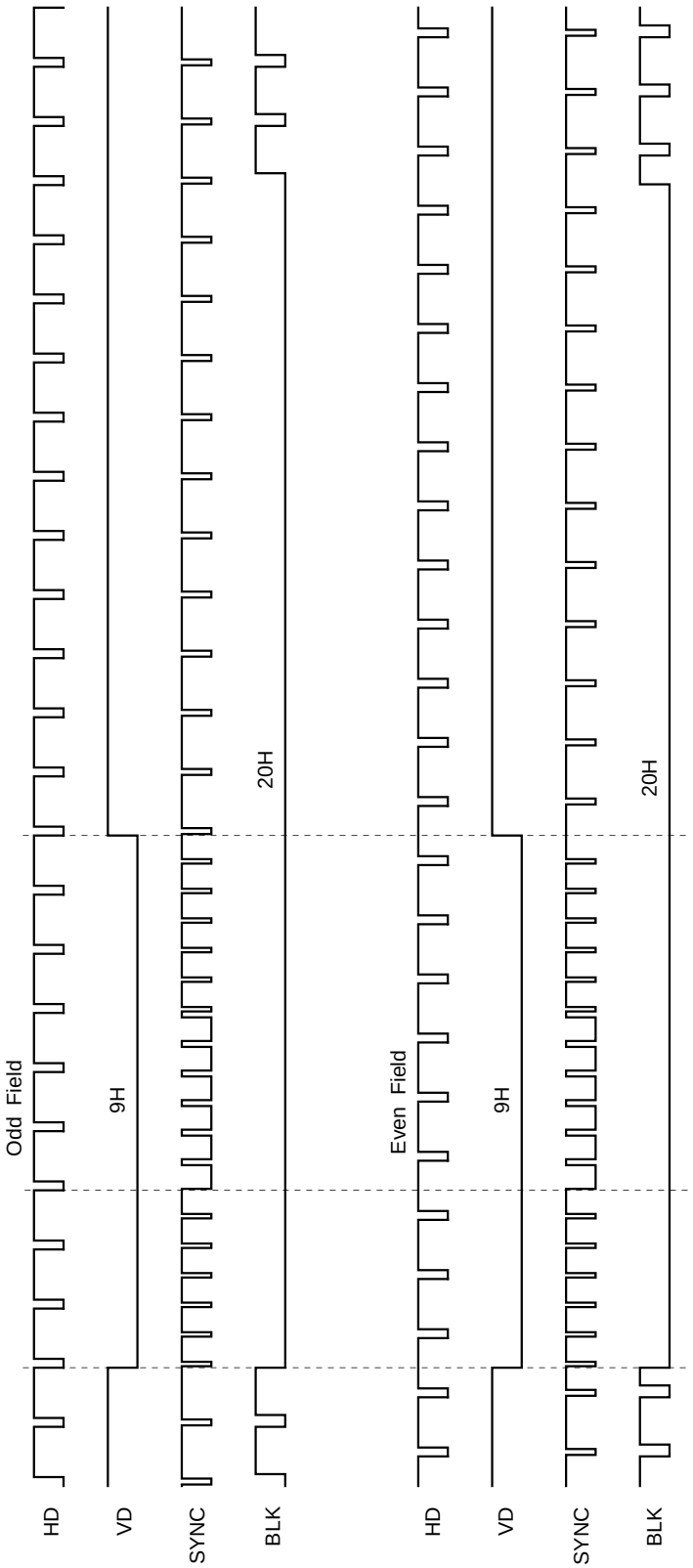
Example of System Configuration



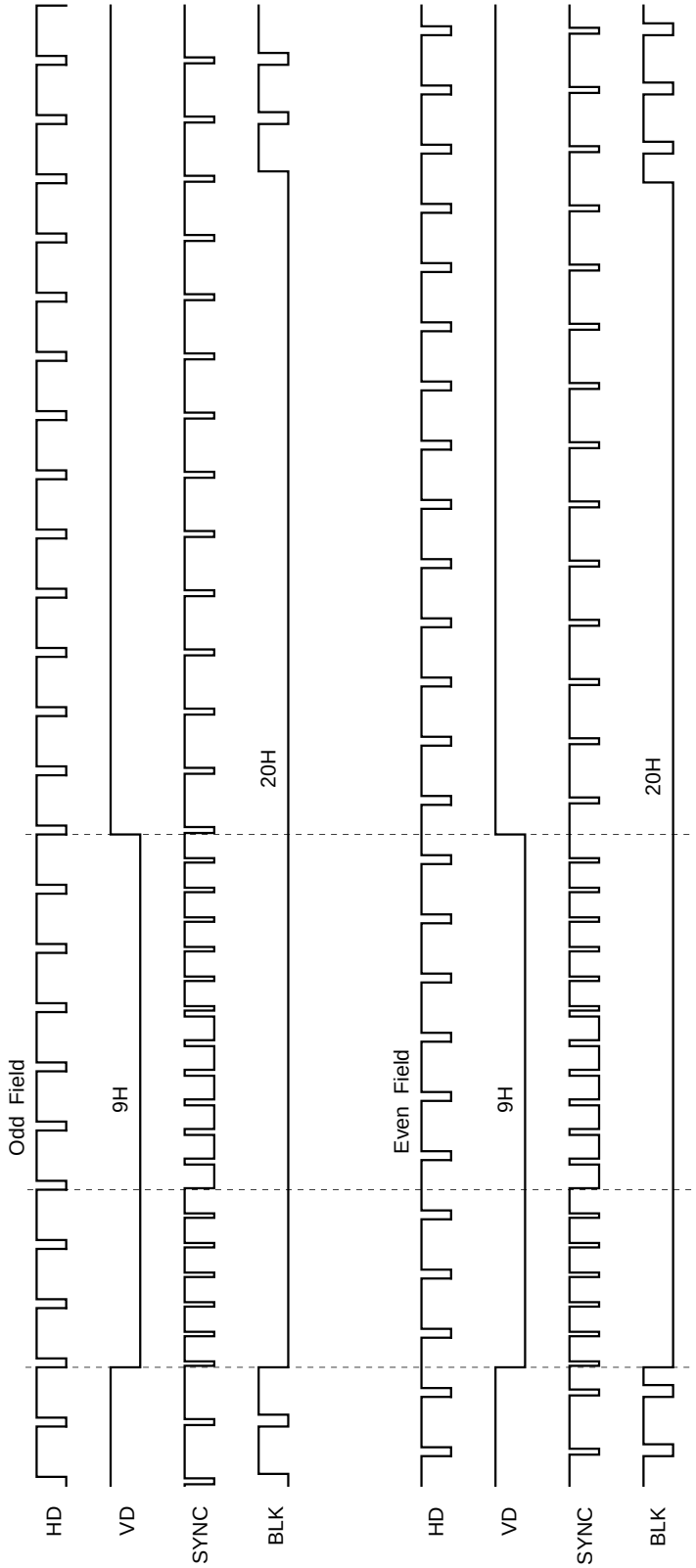
Note) 1. Either SYNC or VD/HD is used as the external sync signal. When SYNC is used (SYNC synchronous mode), fix MODE1 to High; when VD/HD is used (VD/HD synchronous mode), fix MODE1 to Low.

2. Be sure to do phase comparison of the falling edge of EXTf$_H$ and INTf$_H$ for SYNC synchronous mode.

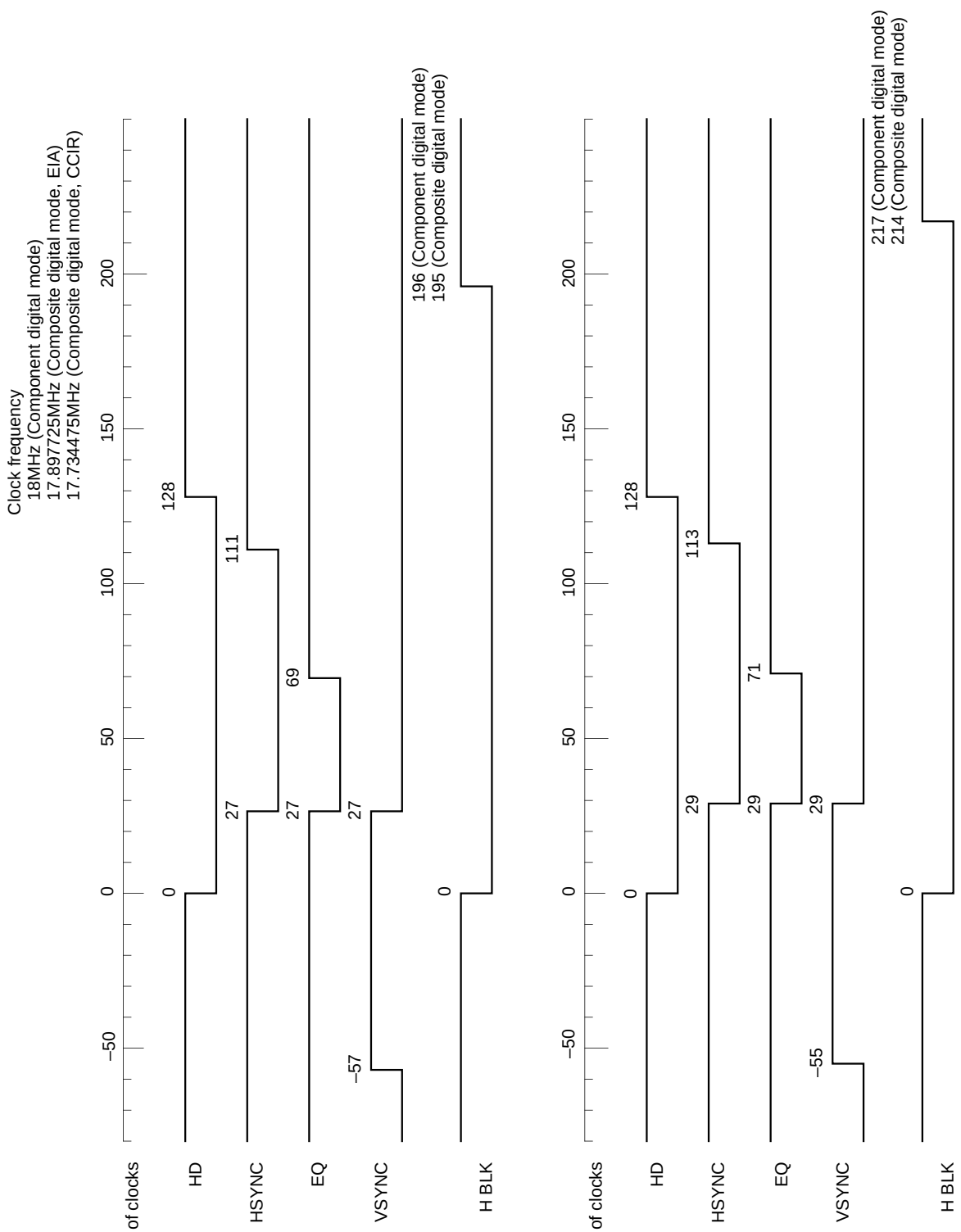
Timing Chart (1) EIA vertical direction



Timing Chart (1) EIA vertical direction

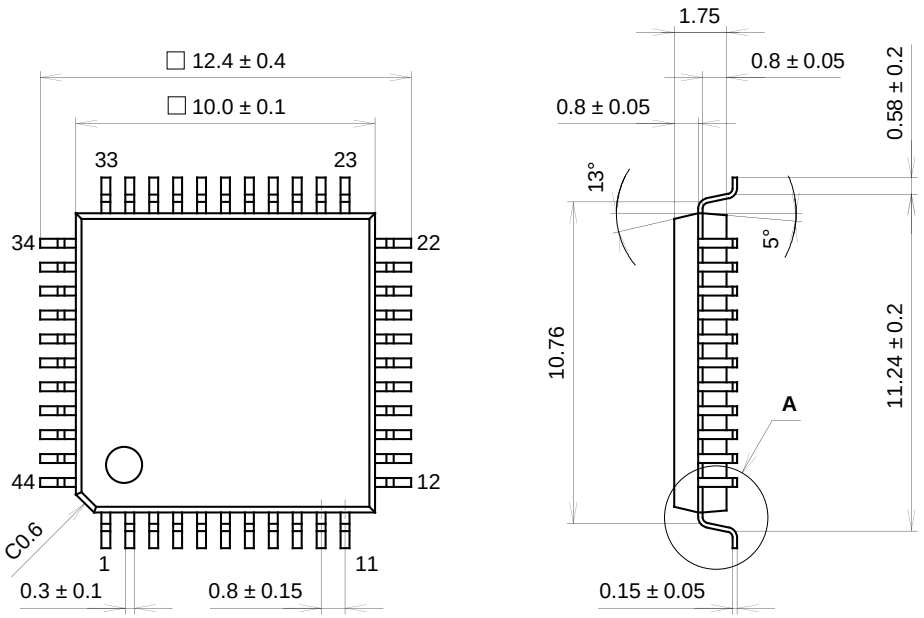


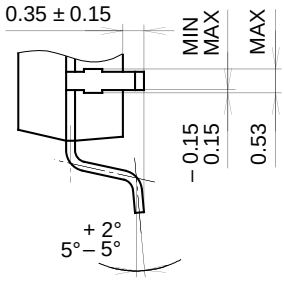
Timing Chart (2) CCIR vertical direction



Package Outline Unit: mm

44PIN QFP (PLASTIC)





DETAIL **A**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.4g

SONY CODE	QFP-44P-L221
EIAJ CODE	∗QFP044-P-1010-B
JEDEC CODE	————————