SONY

CXG1017N

High-Frequency DPDT Antenna Switch

Description

The CXG1017N is a high power antenna switch MMIC. This IC is designed using the Sony's GaAs J-FET process and operates at a single positive power supply.

Features

- Single positive power supply operation
- Insertion loss 0.5dB (Typ.) at 1.5GHz
- High power switching

P1dB (Typ.)	33dBm	at 2.0GHz
		V_{CTL} (H) = 2.0V
	36dBm	at 2.0GHz
		V_{CTL} (H) = 4.0V

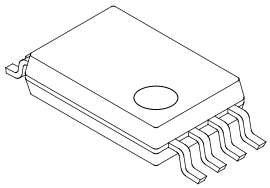
Application

Antenna switch for digital cellular telephones

Structure

GaAs J-FET MMIC

8 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Control voltage	Vctl	7	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Operating Condition

Control voltage	0/4	V

E95Z32-ST

Electrical Characteristics

V_{CTL} (L) = 0V, V_{CTL} (H) = 4V, P_{IN} = 32dBm, R_{RF} = 75kΩ (Ta = 25°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL1	f = 1.0GHz		0.4	0.7	dB
Isolation	ISO1		19	21		dB
Insertion Loss	IL1.5	f = 1.5GHz		0.5	0.8	dB
Isolation	ISO1.5		16	18		dB
Insertion Loss	IL2	f = 2.0GHz		0.7	1.0	dB
Isolation	ISO2		13	15		dB
VSWR	VSWR				1.5	
Switching Time	TSW			100		ns

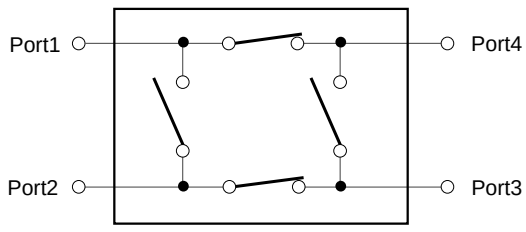
V_{CTL} (L) = 0V, f = 2GHz (Ta = 25°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
1dB Compression Point	P1dB (3)	V_{CTL} (H) = 3V	31	33		dBm
1dB Compression Point	P1dB (4)	V_{CTL} (H) = 4V	34	36		dBm

V_{CTL} (L) = 0V, R_{RF} = 75kΩ (Ta = 25°C)

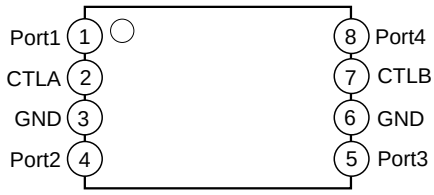
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Control Current	I_{CTL} (3)	V_{CTL} (H) = 3V		130	160	µA
Control Current	I_{CTL} (4)	V_{CTL} (H) = 4V		190	220	µA

Block Diagram



V_{CTLA}	V_{CTLB}	
Hgh	Low	Port1-Port2, Port3-Port4 ON Port2-Port3, Port4-Port1 OFF
Low	High	Port2-Port3, Port4-Port1 ON Port1-Port2, Port3-Port4 OFF

Package Outline/Pin Configulation



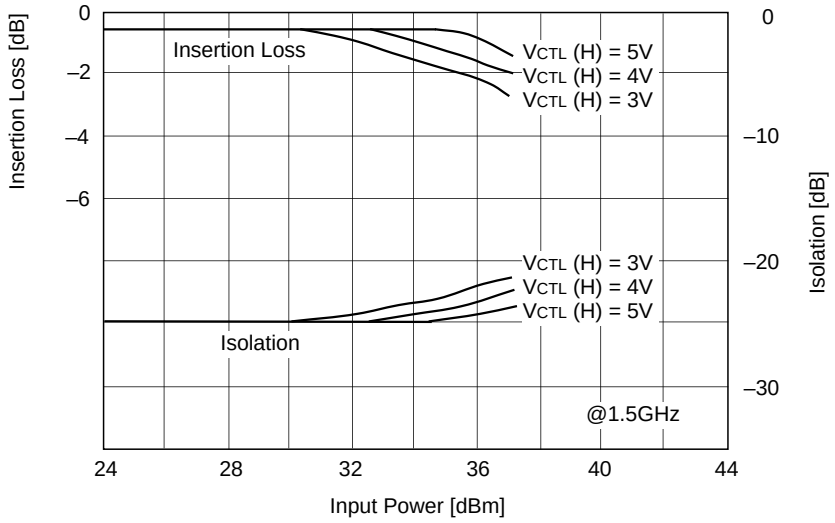
8pin SSOP (PLASTIC)

Recommended Circuit

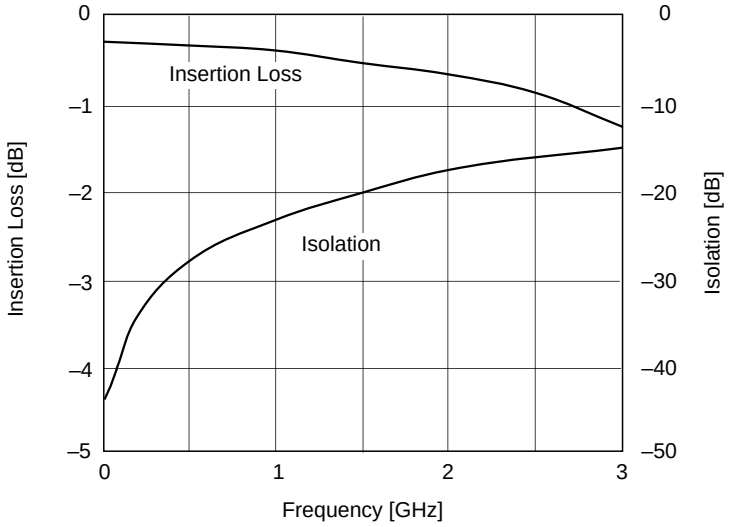
* R_{RF} is used to stabilize the electrical characteristics at high power signal input

Example of Representive Characteristics (Ta = 25°C)

Insertion Loss and Isolation vs. Input Power

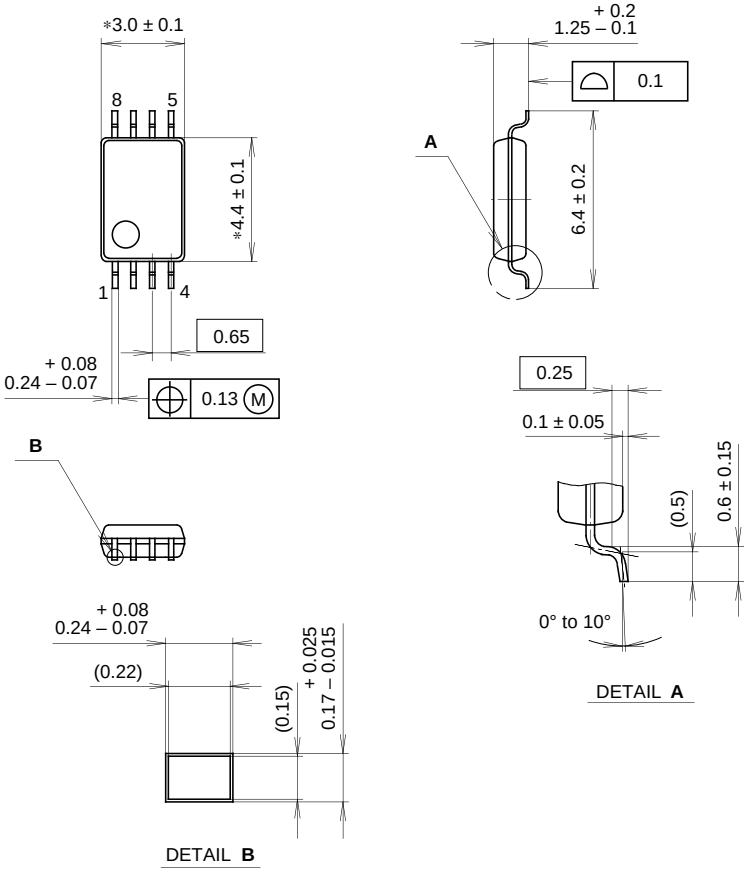


Insertion Loss and Isolation vs. Frequency



Package Outline Unit: mm

8PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-8P-L01
EIAJ CODE	SSOP008-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.04g