

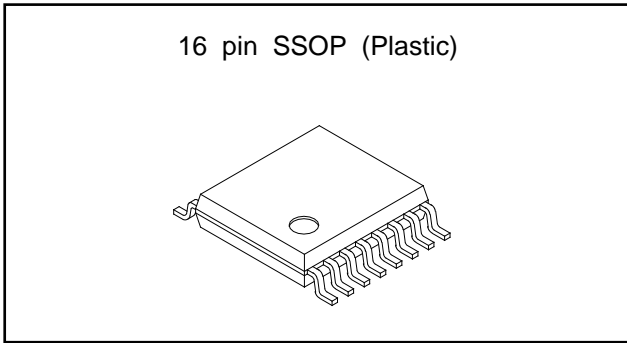
High-Frequency SPDT Antenna Switch

Description

The CXG1024N is a high power antenna switch MMIC to connect Tx/Rx to one of 4 antennas. This IC is designed using the Sony's GaAs J-FET process and operates at a single positive power supply.

Features

- Single positive power supply operation
- Low insertion loss 0.4 dB (Typ.) at 1.0 GHz
 (Tx Port)
- Isolation 21 dB (Typ.) at 1.0 GHz
 (Tx Port)
- High power switching
 P1 dB (Typ.) 32 dBm at 1.5 GHz
 V_{CTL}(H)=3.0 V
 35 dBm at 1.5 GHz
 V_{CTL}(H)=4.0 V



Absolute Maximum Ratings (Ta=25 °C)

- Supply voltage V_{DD} 8 V
- Control voltage V_{ctl} (H)–V_{ctl} (L) 8 V
- Operating temperature T_{opr} –35 to +85 °C
- Storage temperature T_{stg} –65 to +150 °C
- Input Power Pin (RF2, RF3, RF4) 37 dBm
 Pin (RF1, RF5, RF6) 30 dBm

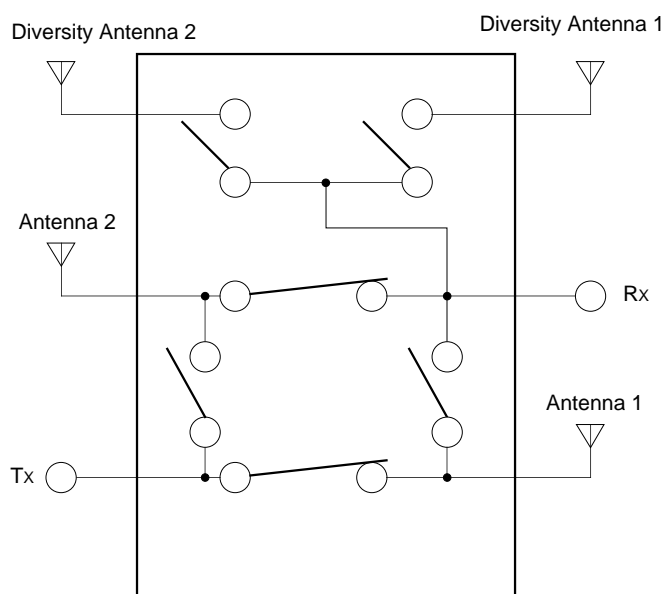
Applications

Antenna switch for digital cellular telephones

Structure

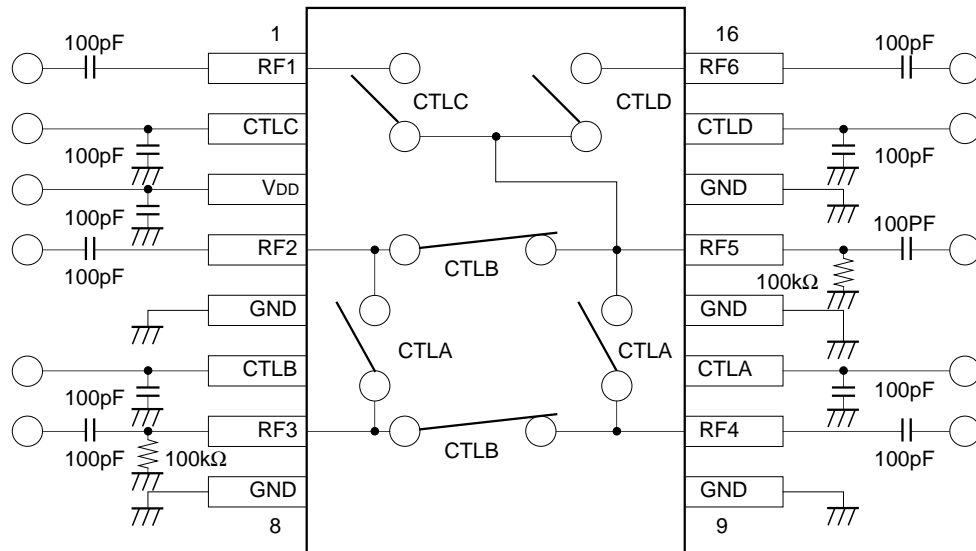
GaAs J-FET MMIC

Function Block Diagram



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Pin Configuration and Recommended Circuit



Logic Table

ON-Port	CTLA	CTLB	CTLC	CTLD
RF3–RF2	H	L	H or L	H or L
RF3–RF4	L	H	H or L	H or L
RF5–RF2	L	H	L	L
RF5–RF4	H	L	L	L
RF5–RF6	L	L	L	H
RF5–RF1	L	L	H	L

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.
Control Voltage (high)	Vctl (H)			6
Control Voltage (low)	Vctl (L)	-6		
Difference of Control Voltage	Vctl (H)–Vctl (L)			6
Supply voltage	VDD	Vctl (H)–0.6	Vctl (H)–0.5	Vctl (H)–0.4

Electrical Characteristics

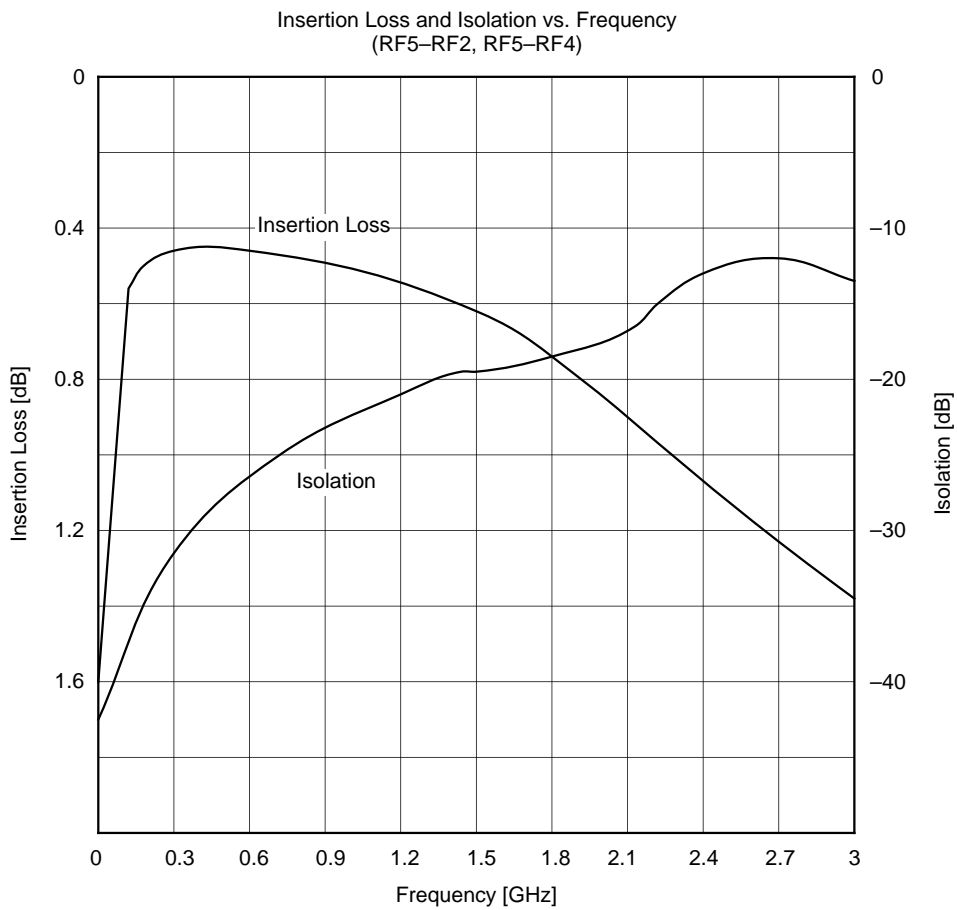
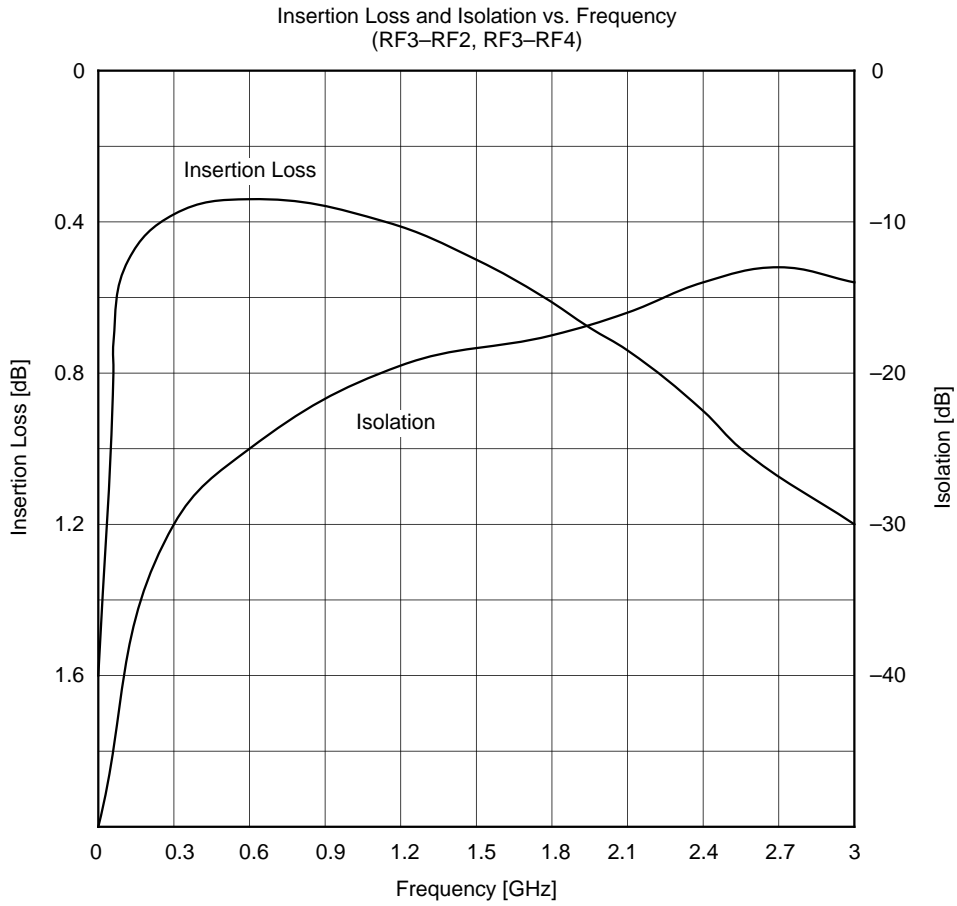
(Ta=25 °C)

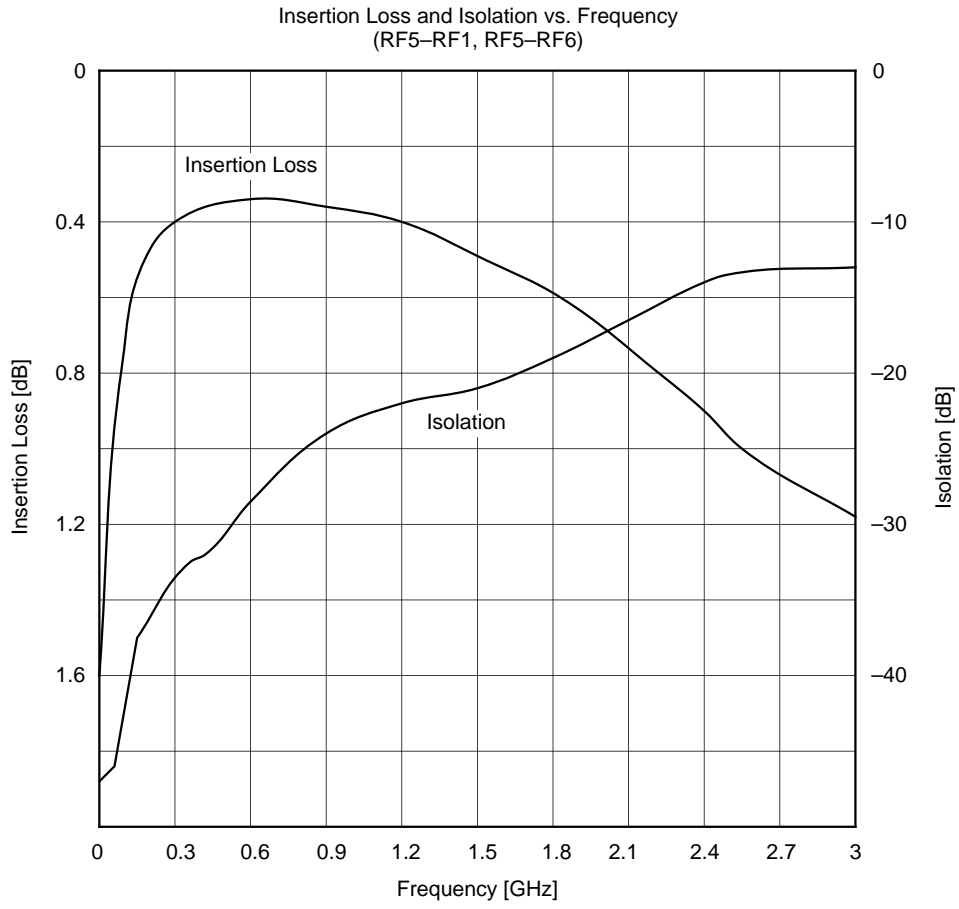
	Symbol	Signal Passes	Test Condition	Frequency	Min.	Typ.	Max.	Unit	
Insertion Loss	IL.	RF3–RF2	*2 Pin=30 dBm	1 GHz		0.4	0.65	dB	
		RF3–RF4		1.5 GHz		0.5	0.8		
				2 GHz		0.7	1.0		
		RF5–RF2	*2 Pin=20 dBm	1 GHz		0.5	0.8		
	1.5 GHz			0.65	0.95				
	2 GHz			0.9	1.2				
	RF5–RF4	*2 Pin=20 dBm	1 GHz		0.6	0.9	dB		
	1.5 GHz			0.75	1.05				
	2 GHz			1.2	1.5				
	RF5–RF1 RF5–RF6	*2 Pin=20 dBm	1 GHz		0.4	0.7		dB	
			1.5 GHz		0.5	0.8			
			2 GHz		0.7	1.0			
Isolation	ISO.	RF3–RF2	*2 Pin=30 dBm	1 GHz	18	21			dB
		RF3–RF4		1.5 GHz	15	18			
				2 GHz	12	15			
		RF5–RF1 RF5–RF6	*2 Pin=20 dBm	1 GHz	21	24			
	1.5 GHz	17		20					
	2 GHz	15		18					
VSWR	VS.	RF3–RF2 RF3–RF4	*2 Pin=30 dBm	0.1 to 2 GHz		1.3	1.5	dB	
		RF5–RF2 RF5–RF4 RF5–RF1 RF5–RF6		*2 Pin=20 dBm	0.1 to 2 GHz		1.3		1.5
1 dB Compression Power	P1 dB	RF3–RF2	*3		1.5 GHz	30	32		dBm
		RF3–RF4		*2	1.5 GHz	33	35		
			*1		1.5 GHz	35	37		
		RF5–RF2 RF5–RF4 RF5–RF1 RF5–RF6		*3	1.5 GHz	22	24		
			*2		1.5 GHz	25	27		
					*1	1.5 GHz	27	29	
Switching Time	tsw			0.1 to 2 GHz			200	nsec	
Control Current	Ictl						100	μA	
Supply Current	IDD						100	μA	
			*2						

*1 : Vctl (H)=5 V, Vctl (L)=0 V, VDD=4.5 V

*3 : Vctl (H)=3 V, Vctl (L)=0 V, VDD=2.5 V

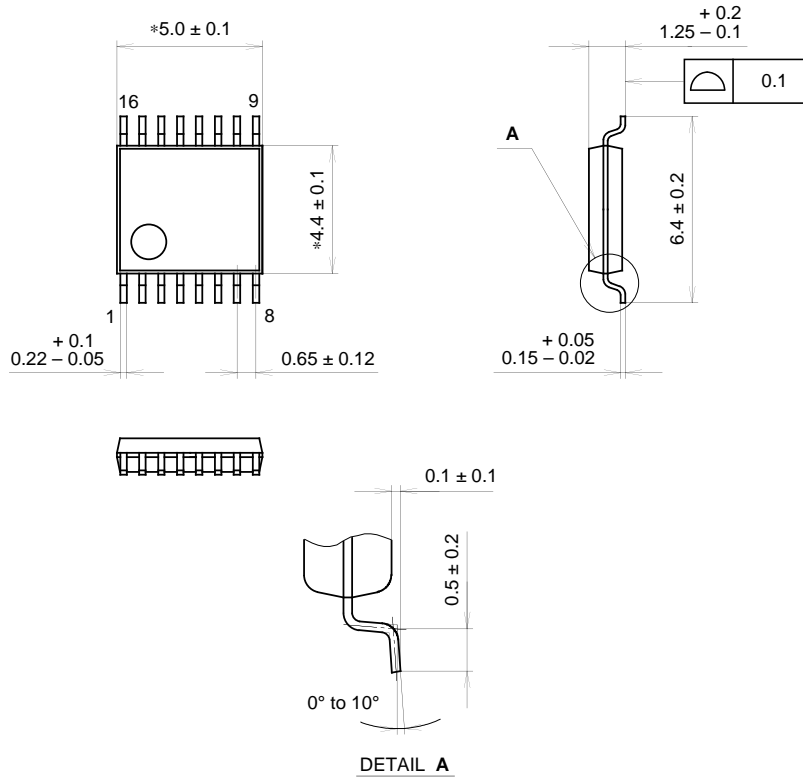
*2 : Vctl (H)=4 V, Vctl (L)=0 V, VDD=3.5 V





Package Outline Unit : mm

16PIN SSOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g