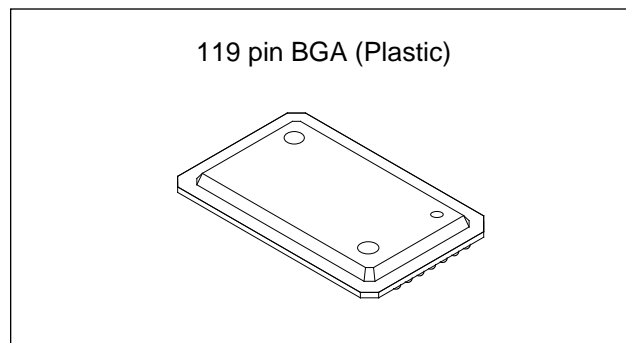


Description

The CXK77B3611AGB-5/6 is a high speed 1M bit Bi-CMOS synchronous static RAM organized as 32768 words by 36 bits. This SRAM integrates input registers, high speed SRAM and write buffer onto a single monolithic IC and features the delayed write system to reduce the dead cycles.

Features

- Fast cycle time (Cycle) (Frequency)
- CXK77B3611AGB-5 5ns 200MHz
- 6 6ns 167MHz
- Inputs and outputs are GTL/HSTL compatible
- Controlled Impedance Driver
- Single 3.3V power supply: 3.3V±0.15V
- Byte-write possible
- \overline{OE} asynchronization
- JTAG test circuit
- Package 119TBGA
- 4 kinds of synchronous operation mode
 - Register-Register mode (R-R mode)
 - Register-Flow Thru mode (R-F mode)
 - Register-Latch mode (R-L mode)
 - Dual clock mode (D-C mode)

**Function**

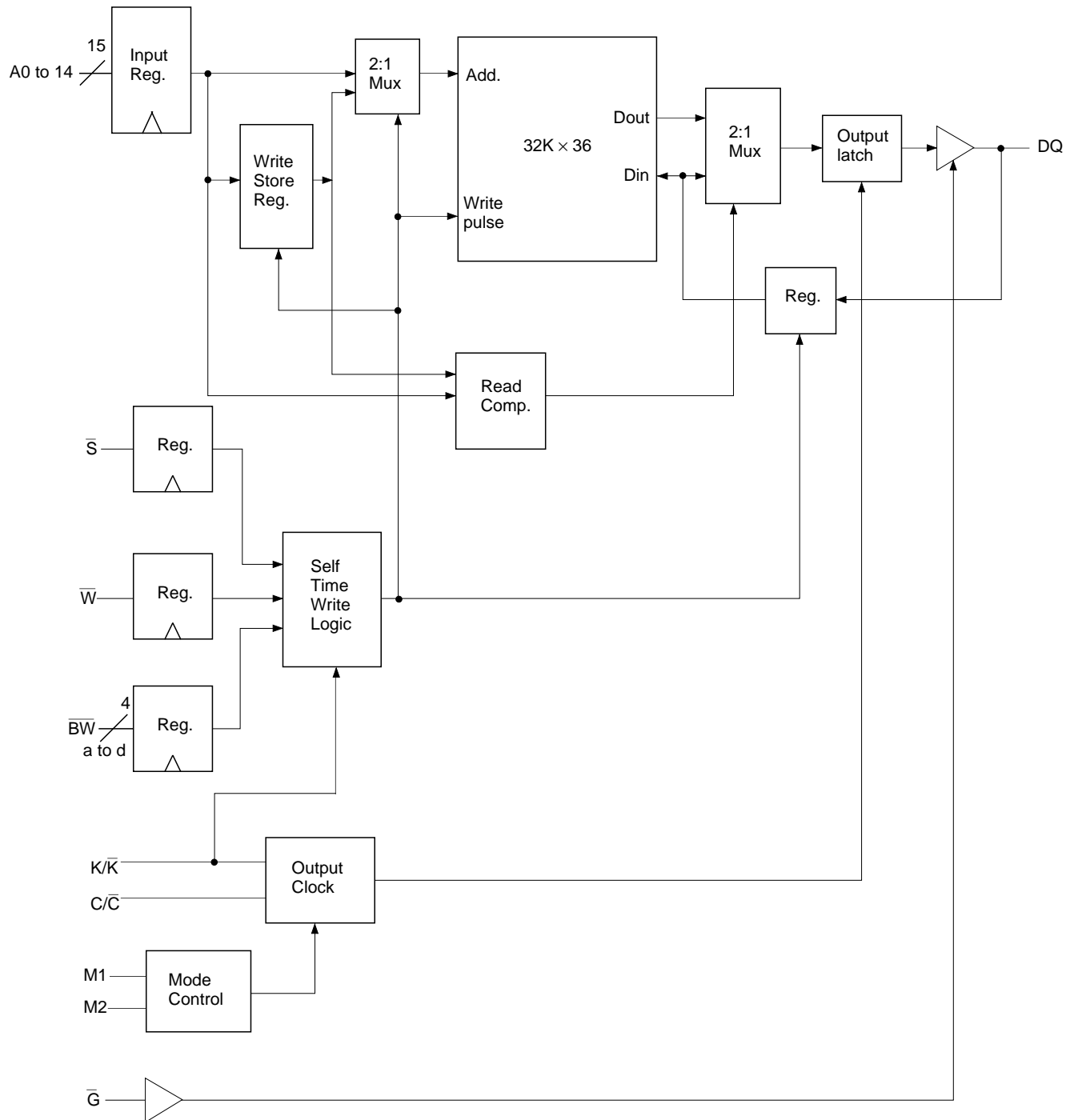
32768 word x 36bit High Speed Bi-CMOS Synchronous SRAM

Structure

Silicon gate Bi-CMOS IC

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Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	NC	A	A	V _{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQ _c	DQ _c	V _{SS}	ZQ	V _{SS}	DQ _b	DQ _b
E	DQ _c	DQ _c	V _{SS}	\overline{S}	V _{SS}	DQ _b	DQ _b
F	V _{DDQ}	DQ _c	V _{SS}	\overline{G}	V _{SS}	DQ _b	V _{DDQ}
G	DQ _c	DQ _c	\overline{BWc}	\overline{C}	\overline{BWb}	DQ _b	DQ _b
H	DQ _c	DQ _c	V _{SS}	C	V _{SS}	DQ _b	DQ _b
J	V _{DDQ}	V _{DD}	VREF	V _{DD}	VREF	V _{DD}	V _{DDQ}
K	DQ _d	DQ _d	V _{SS}	K	V _{SS}	DQ _a	DQ _a
L	DQ _d	DQ _d	\overline{BWd}	\overline{K}	\overline{BWa}	DQ _a	DQ _a
M	V _{DDQ}	DQ _d	V _{SS}	\overline{W}	V _{SS}	DQ _a	V _{DDQ}
N	DQ _d	DQ _d	V _{SS}	A	V _{SS}	DQ _a	DQ _a
P	DQ _d	DQ _d	V _{SS}	A	V _{SS}	DQ _a	DQ _a
R	NC	A	M1	V _{DD}	M2	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

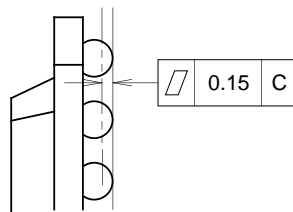
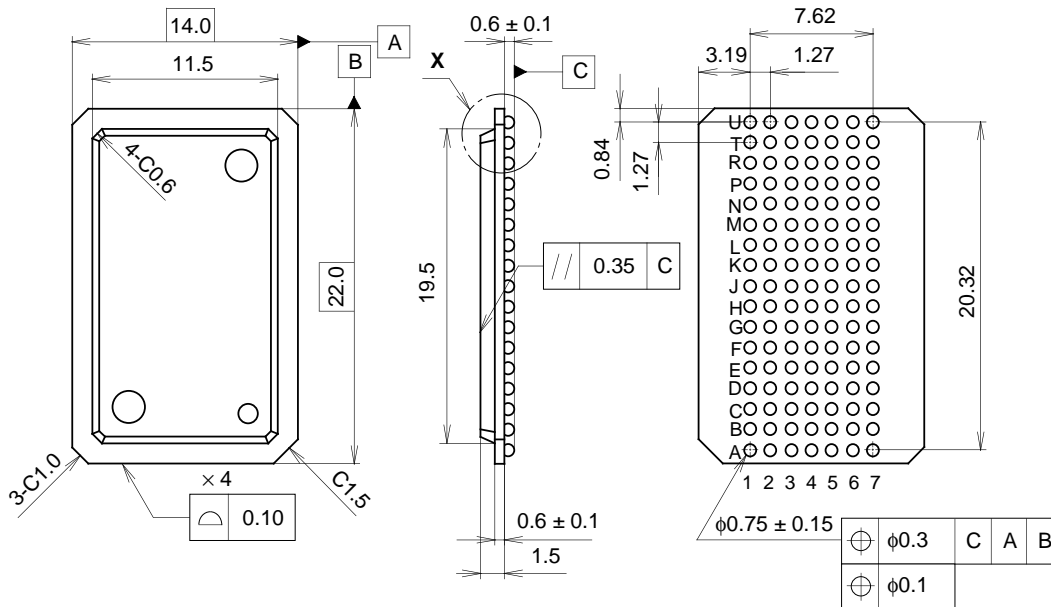
Pin Description

Symbol	Description	Symbol	Description	Symbol	Description
A	Address Input	\overline{BWx}	Byte Write Enable (a to d)	V _{DD}	+3.3V power supply
DQ _x	Data I/O in byte (a to d)	\overline{S}	Chip Select	V _{DDQ}	Output power supply
K	Positive Clock	\overline{G}	Asyn Output Enable	V _{SS}	Ground
\overline{K}	Negative Clock	ZZ	Sleep Mode Select	M1, M2	Mode Select
C	Output Positive Clock(*)	TCK	JTAG Clock	ZQ	Output Impedance Control
\overline{C}	Output Negative Clock(*)	TMS	JTAG Mode Select	NC	No Connect
VREF	Input Reference	TDI	JTAG Data In		
\overline{W}	Write Enable	TDO	JTAG Data Out		

(*) These pins should be tied to V_{DD} or V_{SS} except D-C mode.

Package Outline Unit: mm

119 TERMINAL BGA (PLASTIC)



DETAIL X

PACKAGE STRUCTURE

SONY CODE	BGA-119P-01
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
BOARD MATERIAL	COPPER-CLAD LAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE WEIGHT	0.8g