SONY

# CXL1502M

## CMOS-CCD Signal Processor

### Description

The CXL1502M is a CMOS-CCD signal processor designed for 8-mm video signal processing. In combination with the 8-mm video Y/C signal processing IC CXA1200Q, this IC configures a comb filter for Y/C separation in recording an image, elimination of line crawling and crosstalk in playing back.

### Features

- Single power supply 5V
- Low power consumption
- Built-in peripheral circuits
- Completely adjustment free
- Built-in triple progression PLL circuit
- For PAL signals

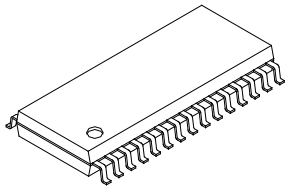
### Functions

- 1H comb filter, 2H comb filter output
- Dropout compensation
- PLL circuit (triple progression)
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit
- Delay time matching through output (THR)

### Structure

CMOS-CCD

30 pin SOP (Plastic)



### Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 6 | V |
| • Operating temperature | Topr | –10 to +60 | °C |
| • Storage temperature | Tstg | –55 to +150 | °C |
| • Allowable power dissipation | $P_D$ | 500 | mW |

### Recommended Operating Conditions (Ta = 25°C)

| | | | |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | 5 ± 5% | V |

### Recommended Clock Conditions (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Input clock amplitude | $V_{CLK}$ | 0.3 to 1.0 (0.4Vp-p Typ.) | Vp-p |
| • Clock frequency | $f_{CLK}$ | 4.433619 | MHz |
| • Input clock waveform | sine wave | | |

### Input Signal Amplitude

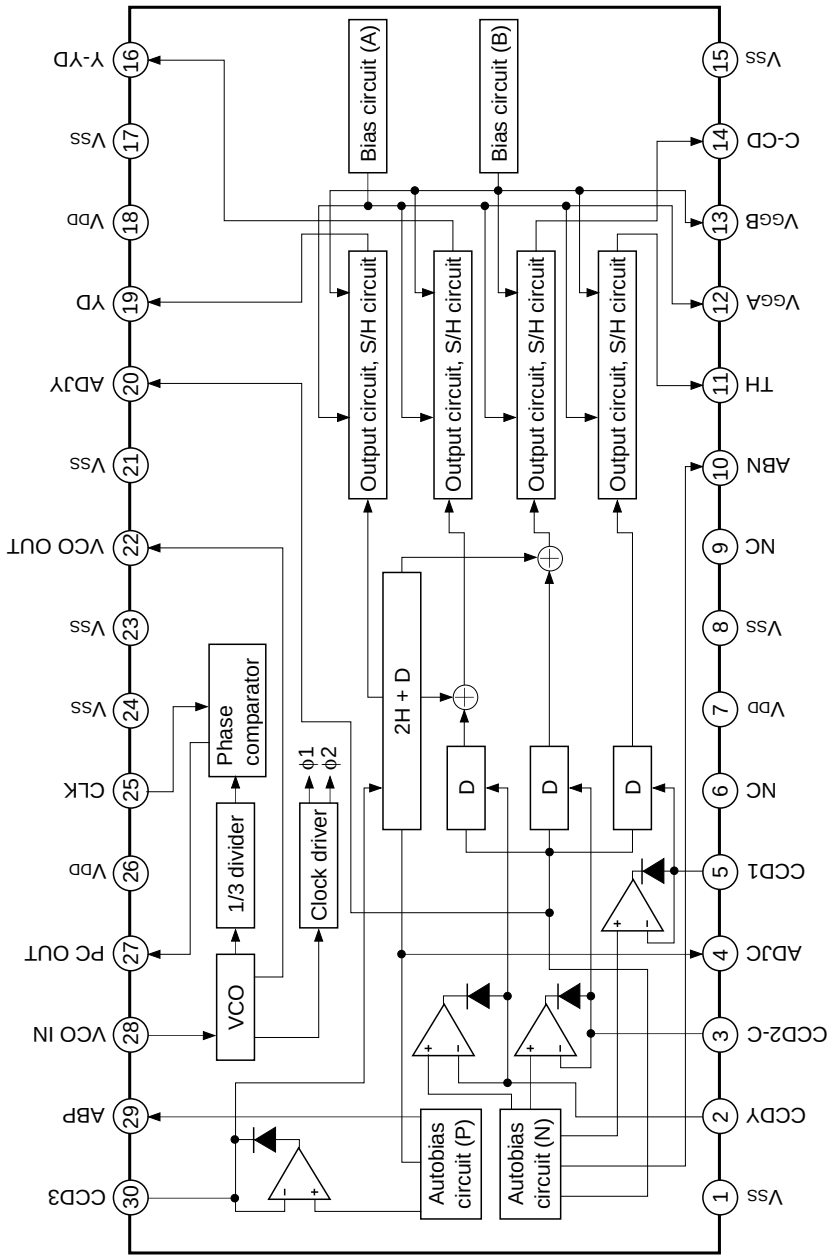
| | | | |
|---|---|---|---|
| | $V_{SIG}$ | 575 (Max.) | mVp-p |





E80334-PS

**Block Diagram**



**Pin Description**

| Pin No. | Symbol | I/O | Description | Impedance (Ω) |
|---|---|---|---|---|
| 1 | $V_{SS}$ | — | GND | |
| 2 | CCDY | I | Signal input 4 (Reverse phase signal) | > 100k (at no clamp) |
| 3 | CCD2-C | I | Signal input 2 (Reverse phase signal) | > 100k (at no clamp) |
| 4 | ADJC | O | Forward CCD bias DC output | 600 to 2k |
| 5 | CCD1 | I | Signal input 1 (Reverse phase signal) | > 100k (at no clamp) |
| 6 | NC | — | | |
| 7 | $V_{DD}$ | — | 5V power supply | |
| 8 | $V_{SS}$ | — | GND | |
| 9 | NC | — | | |
| 10 | ABN | O | Reverse phase autobias DC output | 2k to 200k |
| 11 | TH | O | THR signal output (Forward phase signal) | 40 to 500 |
| 12 | $V_{GG}$A | O | Gate bias (A) DC output | 2k to 10k |
| 13 | $V_{GG}$B | O | Gate bias (B) DC output | 2k to 10k |
| 14 | C-CD | O | 2H comb filter signal output | 40 to 500 |
| 15 | $V_{SS}$ | — | GND | |
| 16 | Y-YD | O | 1H comb filter signal output | 40 to 500 |
| 17 | $V_{SS}$ | — | GND | |
| 18 | $V_{DD}$ | — | 5V power supply | |
| 19 | YD | O | DOC signal output (Reverse phase signal) | 40 to 500 |
| 20 | ADJY | O | Reverse phase CCD bias DC output | 600 to 2k |
| 21 | $V_{SS}$ | — | GND | |
| 22 | VCO OUT | O | VCO output | |
| 23 | $V_{SS}$ | — | GND | |
| 24 | $V_{SS}$ | — | GND | |
| 25 | CLK | I | Clock input | 4k to 40k |
| 26 | $V_{DD}$ | — | 5V power supply | |
| 27 | PC OUT | O | Phase comparator output | 2k to 5k |
| 28 | VCO IN | I | VCO input | > 100k |
| 29 | ABP | O | Forward phase autobias DC output | 2k to 200k |
| 30 | CCD3 | I | Signal input 3 (Forward phase signal) | > 100k (at no clamp) |

## Electrical Characteristics

(Ta = 25°C, $V_{DD}$ = 5V, $f_{CLK}$ = 4.433619MHz, $V_{CLK}$ = 400mVp-p sine wave)

See the Electrical Characteristics Test Circuit.

| Item | Symbol | Test conditions*1 | SW conditions | | | | | | | | | | | Bias conditions*2 (V) | | | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | $V_{BIAS}$ 1 | $V_{BIAS}$ 2 | $V_{BIAS}$ 3 | $V_{BIAS}$ 4 | | | | | |
| Supply current | $I_{DD}$ | — | a | a | a | a | a | a | a | a | a | — | — | — | — | — | — | 50 | 60 | 70 | mA | *3 |
| Low frequency gain | GLC | 203.126kHz 500mVp-p sine wave | a | a | a | a | a | a | a | a | a | c | b | — | — | — | — | –5.0 | –3.0 | –1.0 | dB | *4 |
| | GLY | | a | a | a | a | a | a | a | a | a | b | b | | | | | | | | | |
| | GLD | | a | a | a | a | a | a | a | a | a | a | b | | | | | | | | | |
| | GLT | | a | a | a | a | a | a | a | a | a | d | b | | | | | | | | | |
| High frequency gain | GHC | 4.437525MHz 150mVp-p sine wave | c | a | a | a | a | b | b | b | b | c | b | VID +0.25 | VIY –0.25 | VIC –0.25 | VIT –0.25 | –7.0 | –5.0 | –3.0 | dB | *5 |
| | GHY | | c | a | a | a | a | b | b | b | b | b | b | | | | | | | | | |
| | GHD | | c | a | a | a | a | b | b | b | b | a | b | | | | | | | | | |
| | GHT | | c | a | a | a | a | b | b | b | b | d | b | | | | | | | | | |
| Frequency response | fc | 203.126kHz ↔ 4.437525MHz 150mVp-p sine wave | b↔c | a | a | a | a | b | b | b | b | c | b | VID +0.25 | VIY –0.25 | VIC –0.25 | VIT –0.25 | –3.0 | –2.0 | –1.0 | dB | *6 |
| | fY | | b↔c | a | a | a | a | b | b | b | b | b | b | | | | | | | | | |
| | fD | | b↔c | a | a | a | a | b | b | b | b | a | b | | | | | | | | | |
| | fT | | b↔c | a | a | a | a | b | b | b | b | d | b | | | | | | | | | |
| Differential gain | DGC | 5-staircase wave*7 | h | a | a | a | a | a | a | a | a | c | c | — | — | — | — | 0 | 3 | 7 | deg | *7 |
| | DGY | | h | a | a | a | a | a | a | a | a | b | c | | | | | | | | | |
| | DGD | | h | a | a | a | a | a | a | a | a | a | c | | | | | | | | | |
| | DGT | | h | a | a | a | a | a | a | a | a | d | c | | | | | | | | | |
| Differential phase | DPC | 5-staircase wave*7 | h | a | a | a | a | a | a | a | a | c | c | — | — | — | — | 0 | 3 | 7 | deg | *7 |
| | DPY | | h | a | a | a | a | a | a | a | a | b | c | | | | | | | | | |
| | DPD | | h | a | a | a | a | a | a | a | a | a | c | | | | | | | | | |
| | DPT | | h | a | a | a | a | a | a | a | a | d | c | | | | | | | | | |

| Item | Symbol | Test conditions*1 | SW conditions | | | | | | | | | | | Bias conditions*2 (V) | | | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | $V_{BIAS}$ 1 | $V_{BIAS}$ 2 | $V_{BIAS}$ 3 | $V_{BIAS}$ 4 | | | | | |
| S/N ratio | SNC | No-signal input*8 | — | b | b | b | b | a | a | a | a | c | d | — | — | — | — | — | –56 | –52 | dB | *8 |
| | SNY | | — | b | b | b | b | a | a | a | a | b | d | | | | | | | | | |
| | SND | | — | b | b | b | b | a | a | a | a | a | d | | | | | | | | | |
| | SNT | | — | b | b | b | b | a | a | a | a | d | d | | | | | | | | | |
| S/H pulse coupling | VPC | No-signal input | — | b | b | b | b | b | a | a | a | c | a | VID +0.5 | — | — | — | — | — | 350 | mVp-p | *9 |
| | VPY | | — | b | b | b | b | b | a | a | a | b | a | | | | | | | | | |
| | VPD | | — | b | b | b | b | b | a | a | a | a | a | | | | | | | | | |
| | VPT | | — | b | b | b | b | b | a | a | a | d | a | | | | | | | | | |
| Chroma comb depth min. gain | CCD | 4.437525MHz ↔ 4.441431MHz 200mVp-p sine wave | d↔e | a | a | a | a | b | b | b | b | c | b | VID +0.3 | VIY –0.3 | VIC –0.3 | VIT –0.3 | — | — | –24 | dB | *10 |
| Y-comb depth min. gain | YCD | 2.000011MHz ↔ 1.992198MHz 200mVp-p sine wave | f↔g | a | a | a | a | b | b | b | b | b | b | VID +0.3 | VIY –0.3 | VIC –0.3 | VIT –0.3 | — | — | –15 | dB | *11 |

## Electrical Characteristics Test Circuit

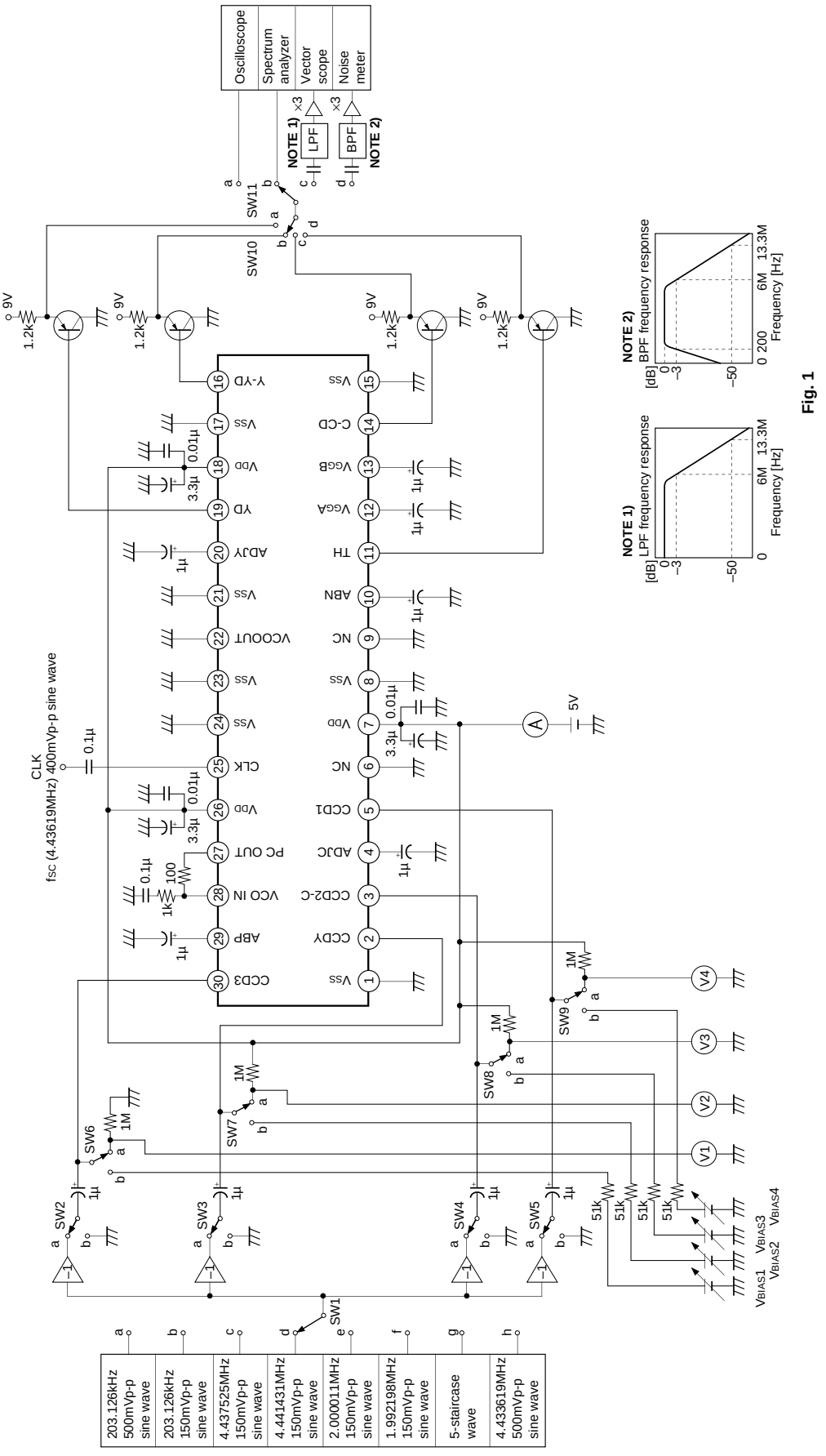
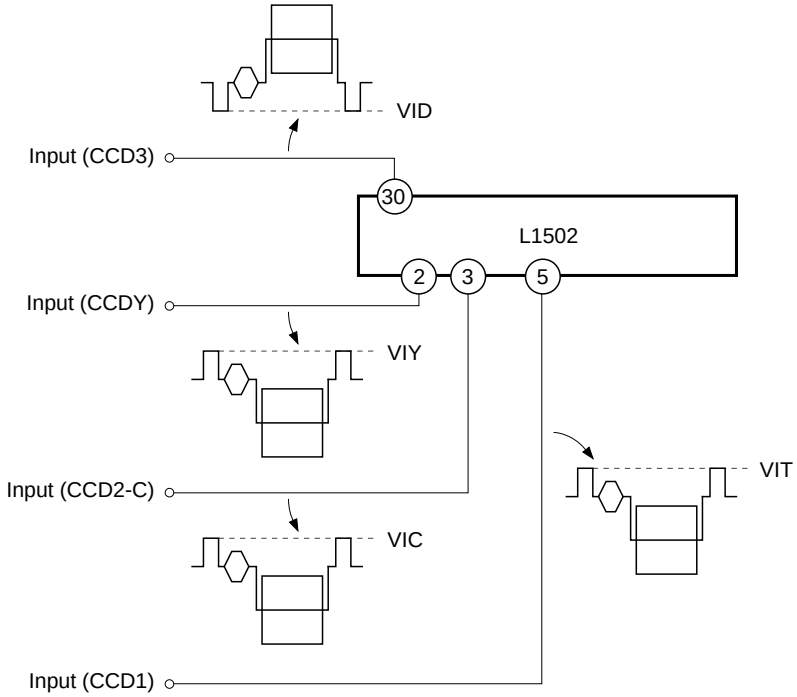



**Fig. 1**

**Notes)**

*1 Adjust the output amplitude of the inversion and the non-inversion amplifiers in the signal input block to an equal value, as well as the phase difference to a precise 180°.
Also set the clock and input signal frequency accurately.

*2 VIC, VIY, VID and VIT are defined as follows:
VIC, VIY, VID and VIT are input signal clamp levels. They clamps the Video signal sync tip level. They are the pin voltages at no-input signal for pins 3, 2, 30 and 5, respectively.




Testing of VIC, VIY, VID and VIT is executed with a voltmeter under the following SW conditions:

| Item | SW conditions | | | | | | | | | | | Test point |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
| VIC | — | b | b | b | b | a | a | a | a | — | — | V3 |
| VIY | — | b | b | b | b | a | a | a | a | — | — | V2 |
| VID | — | b | b | b | b | a | a | a | a | — | — | V1 |
| VIT | — | b | b | b | b | a | a | a | a | — | — | V4 |

*3 This is the IC supply current value during clock and signal input.

*4 GLC, GLY, GLD and GLT are output gains of C-CD, Y-YD, YD and TH pins when a 500mVp-p, 203.126kHz sine wave is simultaneously fed to CCD2-C, CCDY, CCD3 and CCD1 pins, respectively.

(Example of calculation)

$$GLC = 20 \log \frac{\text{C-CD pin output voltage [mVp-p]}}{500\ [\text{mVp-p}]}\ [\text{dB}]$$

*5 GHC, GHY, GHD and GHT are output gains of C-CD, Y-YD, YD and TH pins when a 150mVp-p, 4.437525MHz sine wave is simultaneously fed to CCD2-C, CCDY, CCD3 and CCD1 pins, respectively. Bias at input ($V_{BIAS}1$, $V_{BIAS}2$, $V_{BIAS}3$ and $V_{BIAS}4$) is tested respectively at VID + 0.25V, VIY – 0.25V, VIC – 0.25V and VIT – 0.25V.

(Example of calculation)

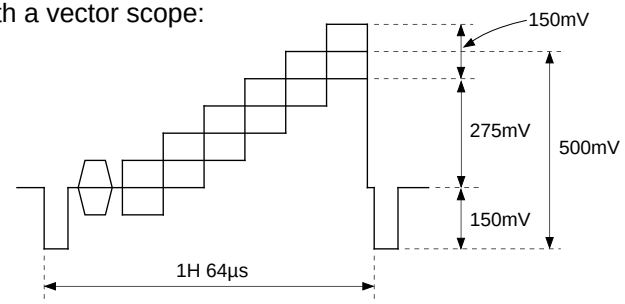
$$GHC = 20 \log \frac{\text{C-CD pin output voltage [mVp-p]}}{150 \text{ [mVp-p]}} \text{ [dB]}$$

*6 Indicates the dissipation at 4.437525MHz in relation to 203.126kHz. From the output voltage at TH, C-CD, Y-YD and YD pins when a 150mVp-p, 203.126kHz sine wave is simultaneously fed to CCD1, CCD2-C, CCDY and CCD3 pins, and from the output voltage at TH, C-CD, Y-YD and YD pins when a 150mVp-p, 4.437525MHz sine wave is simultaneously fed to same, calculation is made according to the following formula. The input block bias for $V_{BIAS}1$, $V_{BIAS}2$, $V_{BIAS}3$ and $V_{BIAS}4$ is tested at VID + 0.25V, VIY – 0.25V, VIC – 0.25V and VIT – 0.25V, respectively.

(Example of calculation)

$$fT = 20 \log \frac{\text{TH pin output voltage (4.437525MHz) [mVp-p]}}{\text{TH pin output voltage (203.126kHz) [mVp-p]}} \text{ [dB]}$$

*7 The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:




CCD3 pin input waveform (the input waveform of CCD1, CCD2-C and CCDY pins is the inverted waveform of the figure above.)

*8 The noise level of output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100kHz to 5MHz. Vn [Vrms]

The signal component is determined either by testing the output voltage (the same test system as that of noise level) at input of 350mVp-p, 203.126kHz, or by performing calculation from the values of GLT, GLC, GLY and GLD in accordance with the following formula. Vs [Vp-p]

(Example of $V_S$ calculation)

$$V_{S\text{-}T} = 0.35 \times 10^{\frac{GLT}{20}} \quad (V_{S\text{-}T}\text{: TH output voltage})$$

(Example of S/N ratio calculation)

$$SNT = 20 \log \frac{V_{N\text{-}T} \text{ (noise component) [Vrms]}}{V_{S\text{-}T} \text{ (signal component) [Vp-p]}} \text{ [dB]}$$

*9 The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input block bias for $V_{BIAS}1$ is tested at VID + 0.5V and VIC – 0.25V.

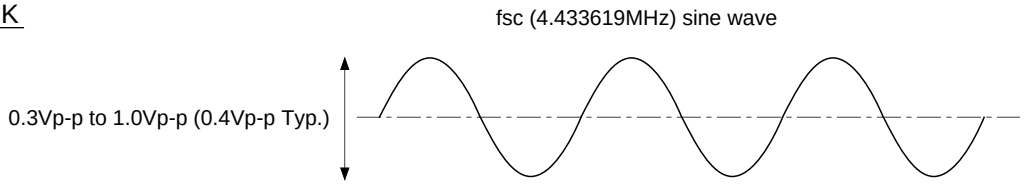

*10 C-CD is calculated in accordance with the following formula from the C-CD pin output voltage when a 200mVp-p, 4.437525MHz sine wave is simultaneously fed to CCD1, CCD2-C, CCDY and CCD3 pins and from the C-CD pin output voltage when a 200mVp-p, 4.441431MHz sine wave is simultaneously fed to same. The input block bias for $V_{BIAS}1$, $V_{BIAS}2$, $V_{BIAS}3$ and $V_{BIAS}4$ is set to VID + 0.3V, VIY – 0.3V, VIC – 0.3V and VIT – 0.3V, respectively.

$$\text{C-CD} = 20 \log \frac{\text{C-CD pin output voltage (4.437525MHz)}}{\text{C-CD pin output voltage (4.441431MHz)}} \text{ [dB]}$$

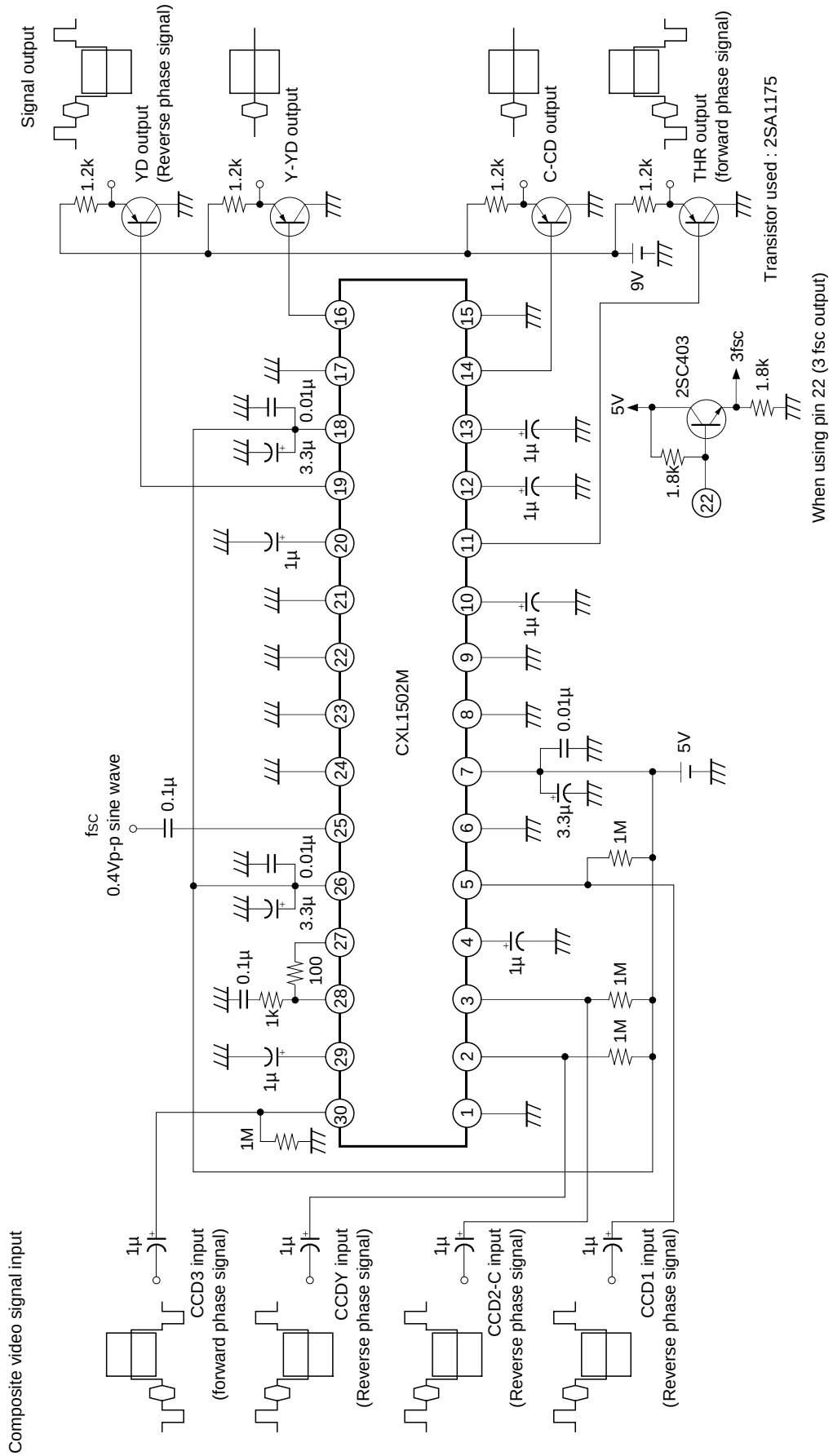
*11 Y-CD is calculated in accordance with the following formula from the Y-YD pin output voltage when a 200mVp-p, 2.000011MHz sine wave is simultaneously fed to CCD1, CCD2-C, CCDY and CCD3 pins and from the Y-YD pin output voltage when a 200mVp-p, 1.992198MHz sine wave is simultaneously fed to same. The input block bias is set to the same conditions as in testing CCD.

$$\text{Y-CD} = 20 \log \frac{\text{Y-YD pin output voltage (1.992198MHz)}}{\text{Y-YD pin output voltage (2.000011MHz)}} \text{ [dB]}$$

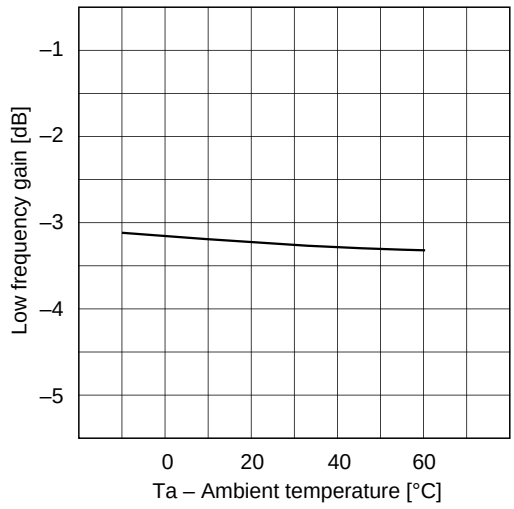
CLOCK



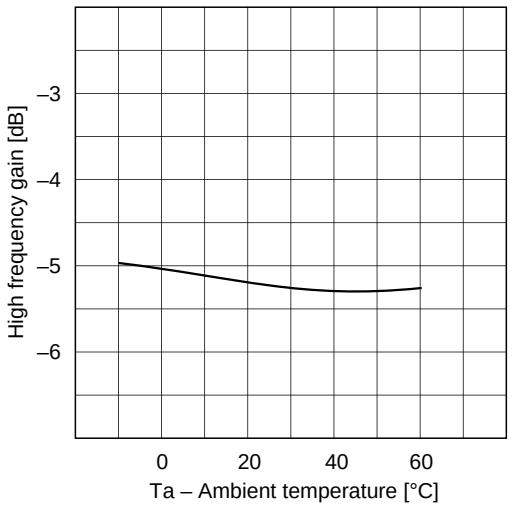
## Application Circuit



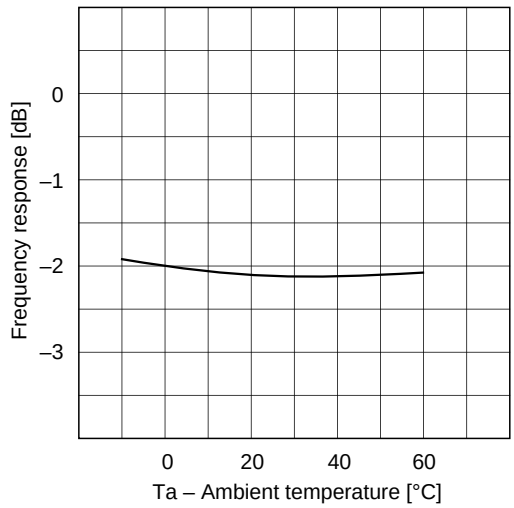
**Low frequency gain vs. Ambient temperature**



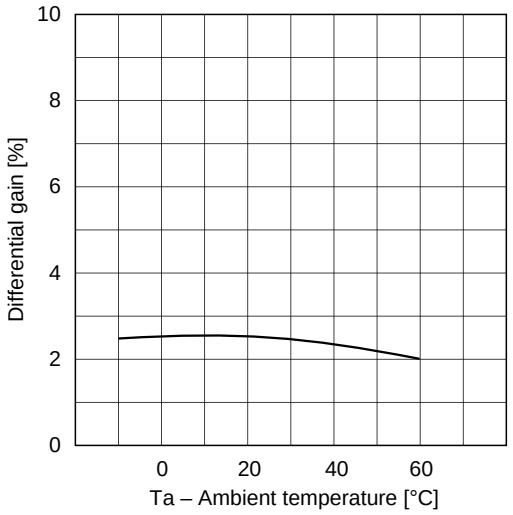

**High frequency gain vs. Ambient temperature**



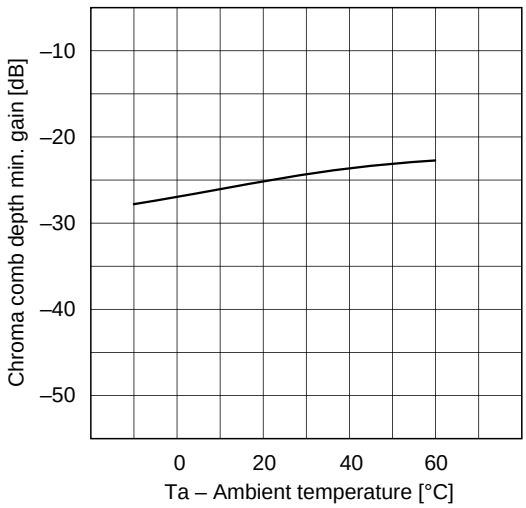

**Frequency response vs. Ambient temperature**



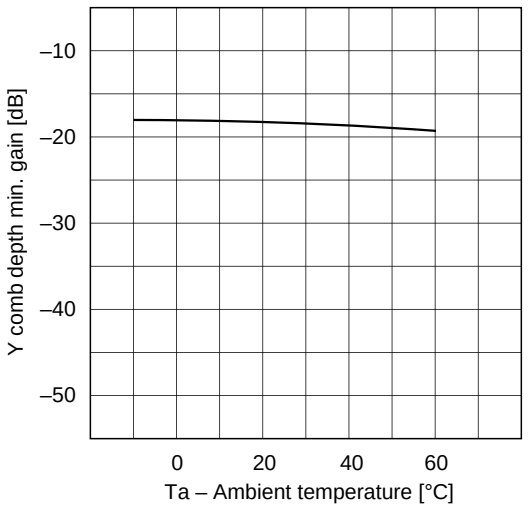

**Differential gain vs. Ambient temperature**



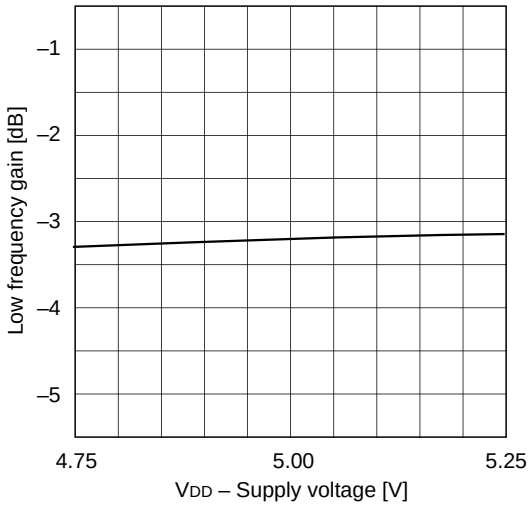

**Chroma comb depth min. gain vs. Ambient temperature**



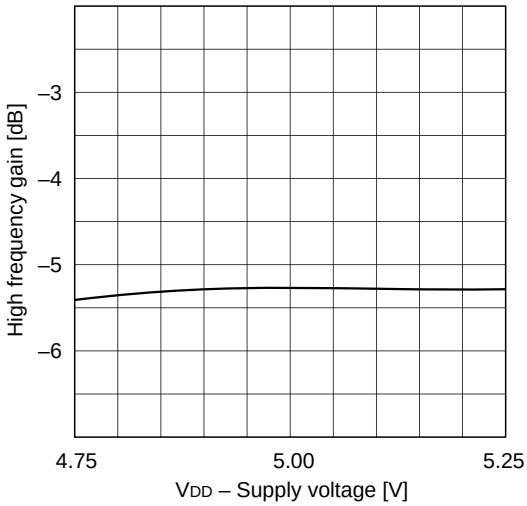

**Y comb depth min. gain vs. Ambient temperature**



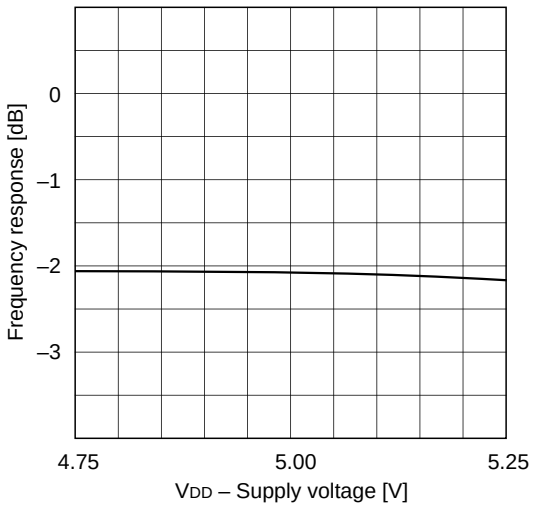
**Low frequency gain vs. Supply voltage**



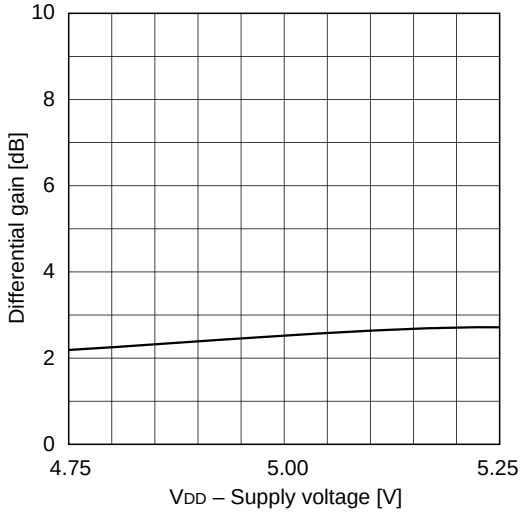

**High frequency gain vs. Supply voltage**



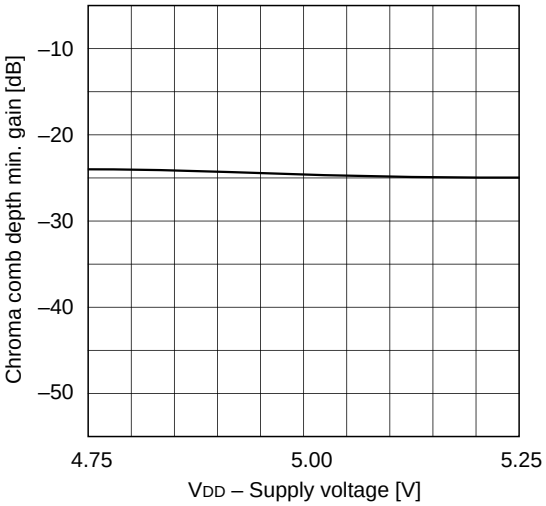

**Frequency response vs. Supply voltage**



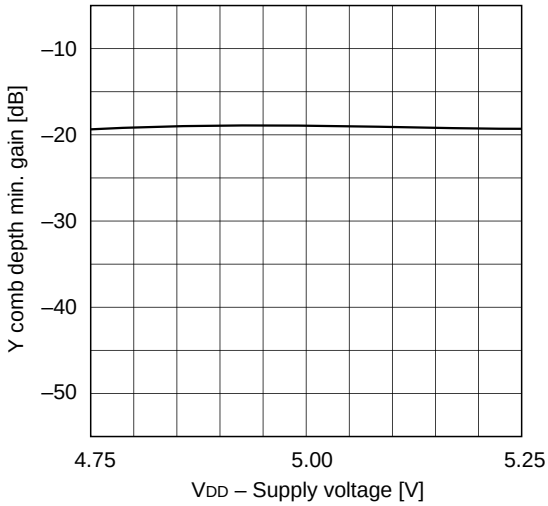

**Differential gain vs. Supply voltage**



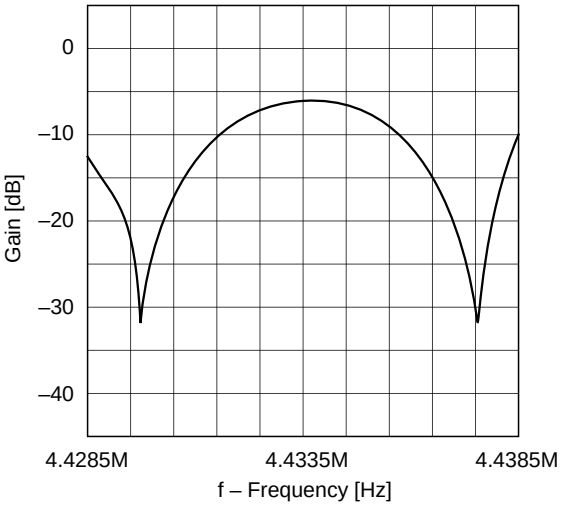

**Chroma comb depth min. gain vs. Supply voltage**



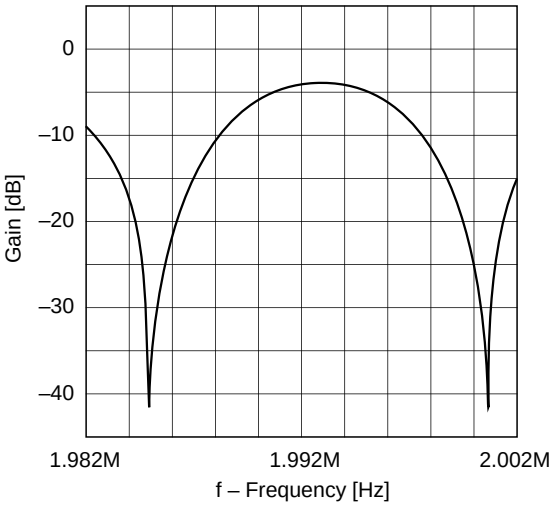

**Y comb depth min. gain vs. Supply voltage**



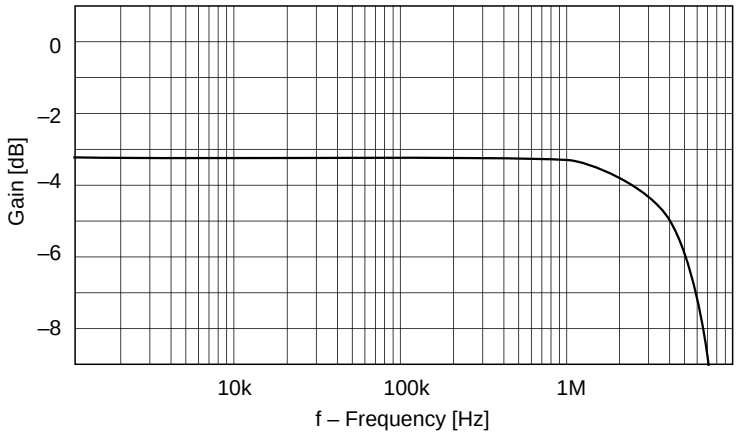
**Chroma comb response (C-CD output)**




**Y comb response (Y-YD output)**

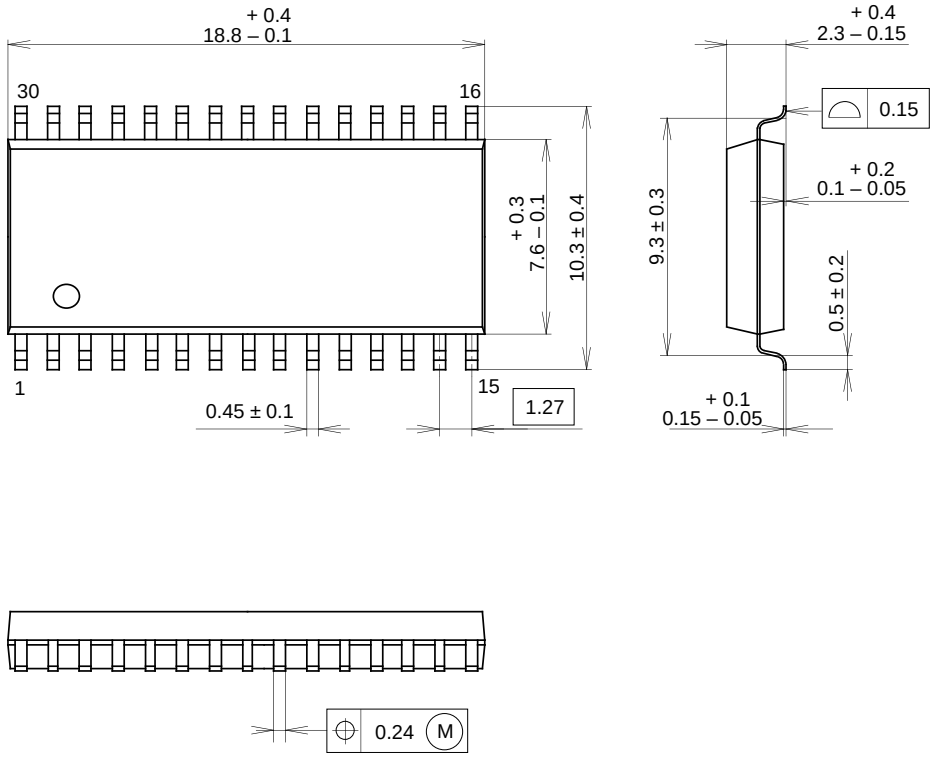



**Frequency response (TH, YD output)**



**Package Outline** Unit: mm

30PIN SOP (PLASTIC)




| | |
|---|---|
| SONY CODE | SOP-30P-L01 |
| EIAJ CODE | SOP030-P-0375 |
| JEDEC CODE | ———————— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE MASS | 0.7g |