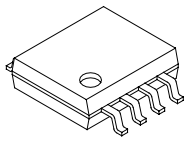
SONY

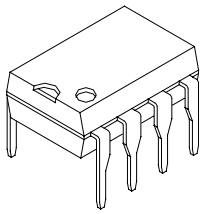
CXL5003M/P

CMOS-CCD 1H Delay Line for PAL

CXL5003M
8 pin SOP (Plastic)



CXL5003P
8 pin DIP (Plastic)



Description

The CXL5003M/P are general-purpose CMOS-CCD delay line ICs that provide 1H delay time for PAL.

Features

- Low power consumption 110mW (Typ.)
- Small size package (8-pin SOP, DIP)
- Low differential gain DG = 3% (Typ.)
- Input signal amplitude 180 IRE (= 1.28Vp-p, Max.)
- Low input clock amplitude operation 150mVp-p (Min.)
- Built-in peripheral circuits (clock driver, timing generator, autobias, and output circuits)

Functions

- 848-bit CCD register
- Clock drivers
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	11	V
• Supply voltage	V_{CL}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5003M	350	mW
	CXL5003P	480	mW

Recommended Operating Conditions

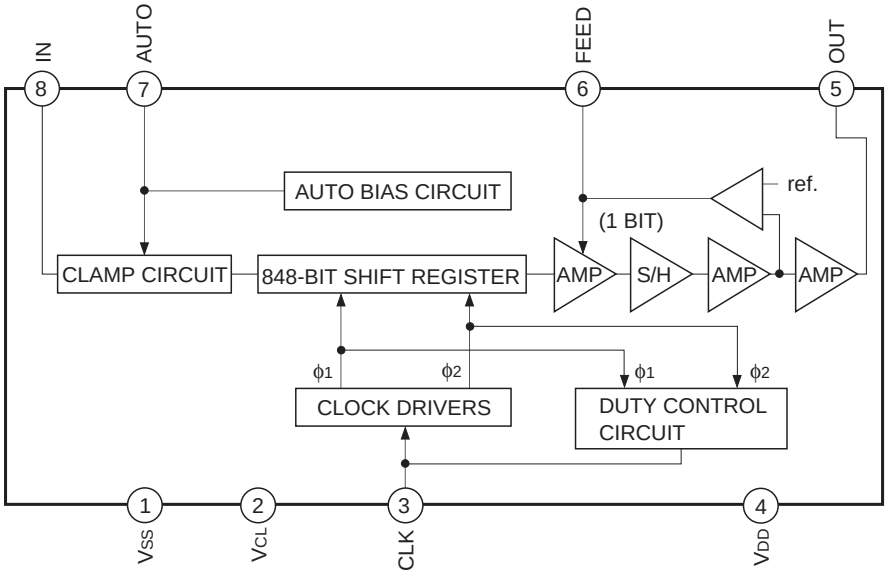
Supply voltage	V_{DD}	9 ± 5%	V
	V_{CL}	5 ± 5%	V

Recommended Clock Conditions

• Input clock amplitude	V_{CLK}	150mVp-p to 1.0Vp-p (250mVp-p typ.)
• Clock frequency	f_{CLK}	13.300856MHz

E51215B79-PS

Blook Diagram



Pin Description

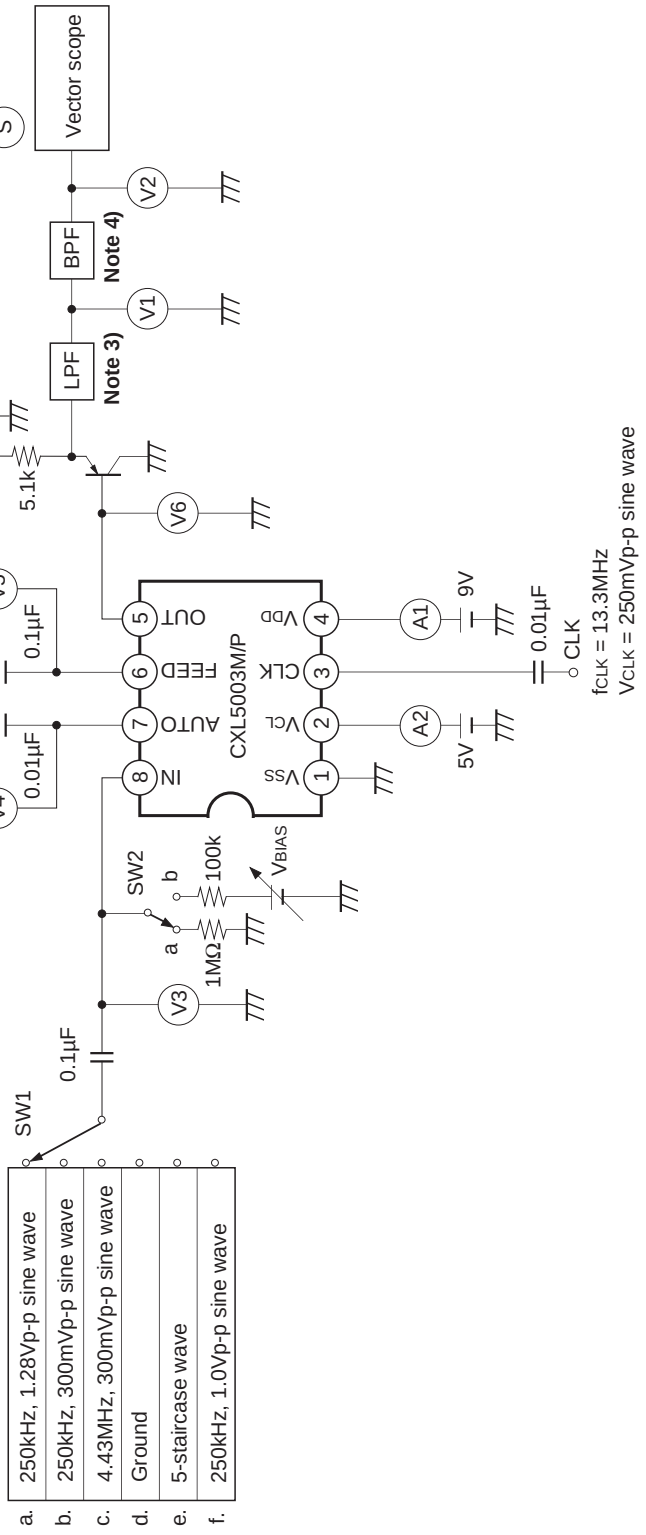
Pin No.	Symbol	Description	Impedance [Ω]	Pin No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	> 100k
3	CLK	Clock input	> 100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	> 100k

Electrical Characteristics

(Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, f_{CLK} = 13.3MHz, V_{CLK} = 250mVp-p sine wave, See "Electrical characteristics test circuit")

Item	Symbol	Measuring condition	SW conditions 1	SW conditions 2	Measuring point	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	250kHz, 1.28Vp-p, sine wave input	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	14	16	mA
Insertion gain	IG	250kHz, 1.28Vp-p, sine wave input IG = 20 log (Output voltage [Vp-p] / 1.28 [Vp-p])	a	a	V1	–3	0	3	dB
Frequency response	fG	Dissipation at 4.43MHz in relation to 250kHz fG = 20 log ($V_{4.43MHz}$/ V_{250kHz}) **(Note 1)**	b, c	b	V1	–3.0	–2.1	—	dB
Differential gain	DG	5-staircase wave input Y = 140 IRE (= 1.0Vp-p) Measure S point with vector scope **(Note 2)**	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: Input = 250kHz, 1.0Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: Input = DC ground output (mVrms)	d	a	V2				
Output DC voltage	V_{IN-AC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	250kHz, 1.28Vp-p, sine wave input	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

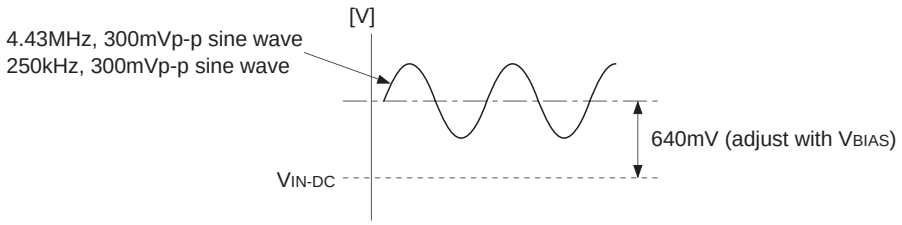
Electrical Characteristics Test Circuit



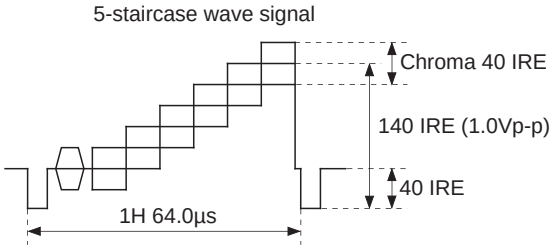
Note 1) Frequency response measuring condition

$V_{4.43MHz}$ (Output signal voltage [Vp-p] at 4.43MHz input)
V_{250kHz} (Output signal voltage [Vp-p] at 250kHz input)

Set Pin 8 (IN) voltage [V] = V_{IN-DC} + 640mV.

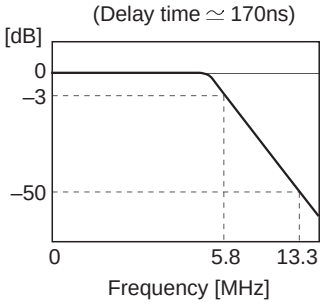


Note 2) Differential gain and differential phase measuring condition

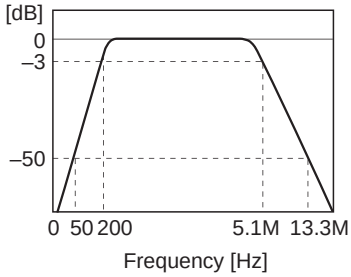


DG and DP are measured at output S point by vector scope.

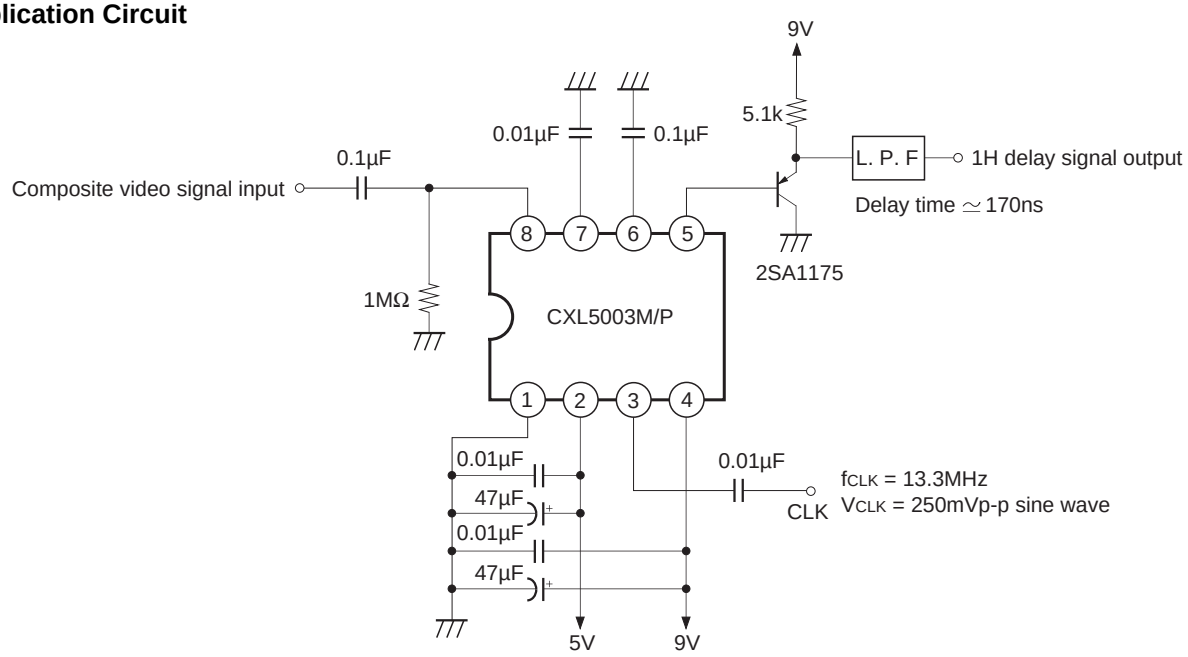
Note 3) LPF frequency response



Note 4) BPF frequency response

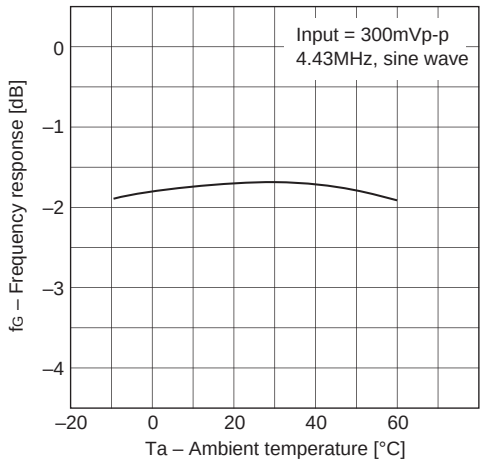


Application Circuit

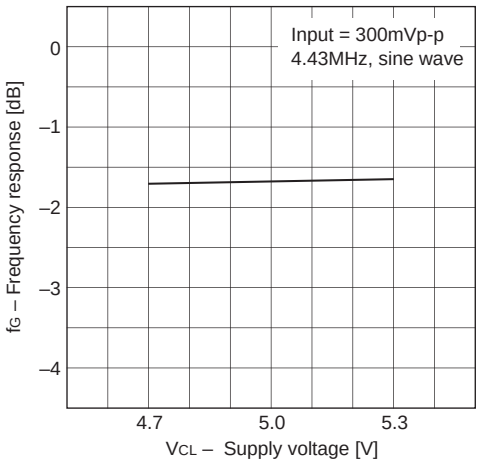


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

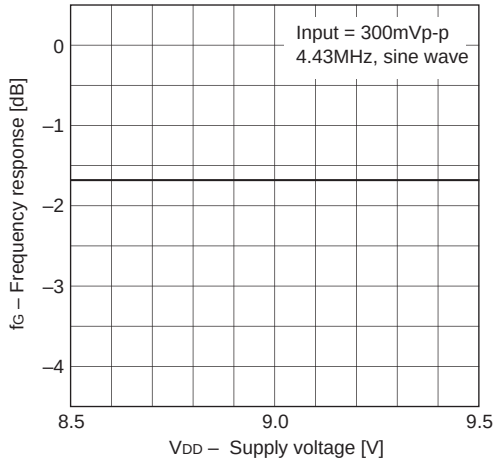
Frequency response vs. Ambient temperature



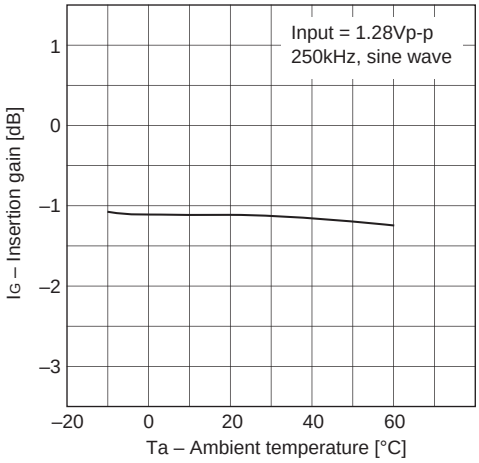
Frequency response vs. Supply voltage



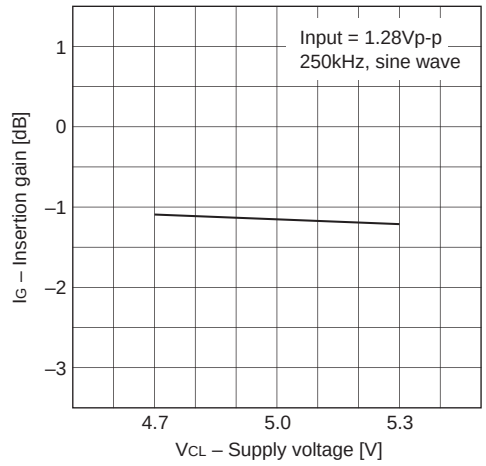
Frequency response vs. Supply voltage



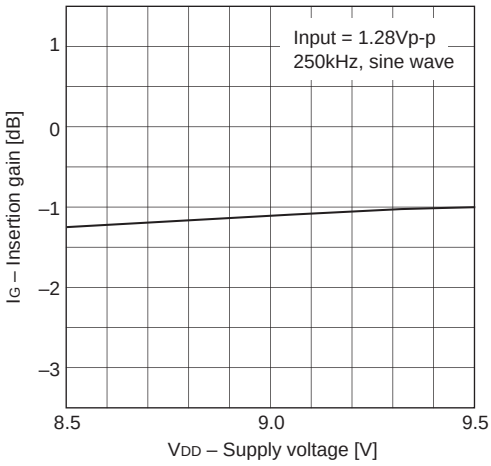
Insertion gain vs. Ambient temperature



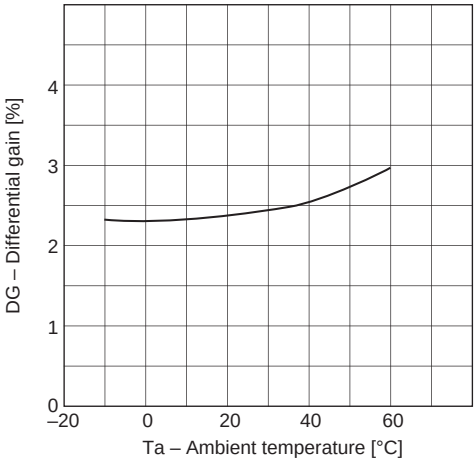
Insertion gain vs. Supply voltage



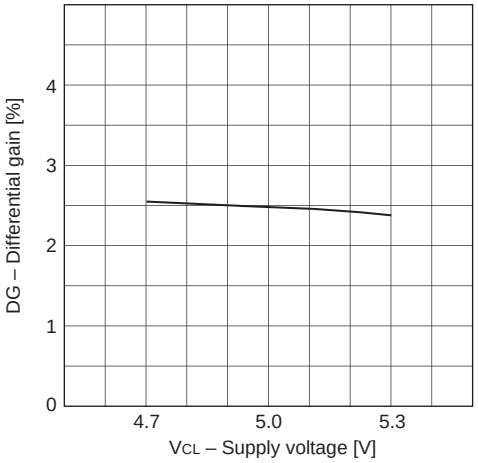
Insertion gain vs. Supply voltage



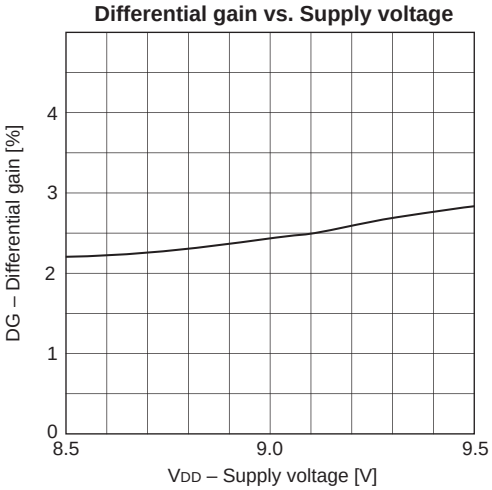
Differential gain vs. Ambient temperature



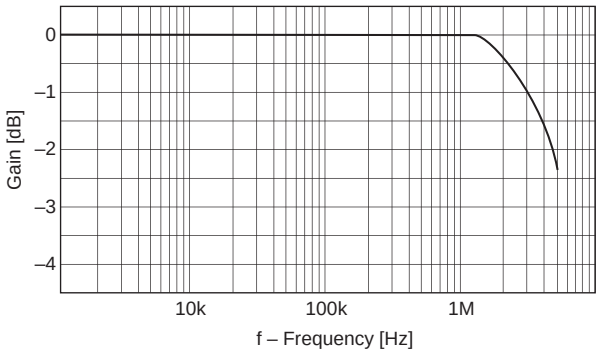
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage

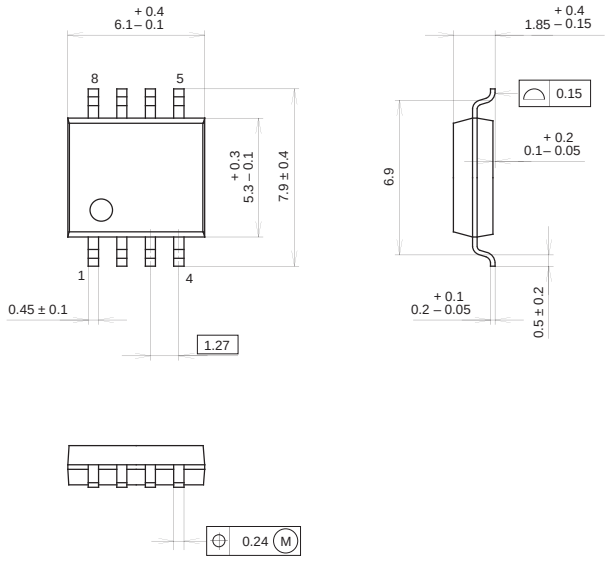


Frequency response



Package Outline Unit: mm

CXL5003M 8PIN SOP (PLASTIC)

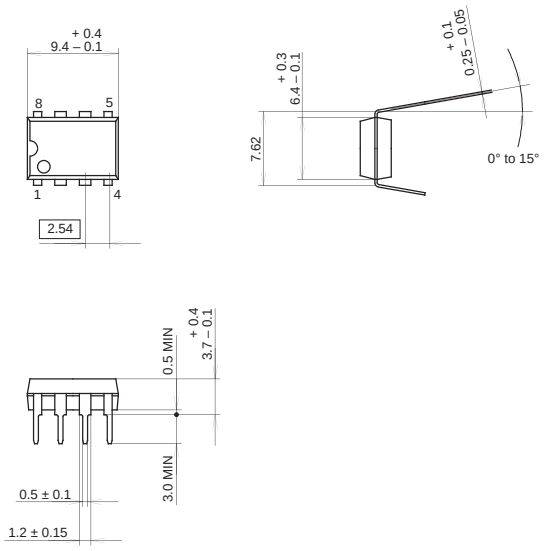


PACKAGE STRUCTURE

SONY CODE	SOP-8P-L01
EIAJ CODE	SOP008-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

CXL5003P 8PIN DIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	DIP-8P-01
EIAJ CODE	DIP008-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g