SONY

CXL5508M/P

CMOS-CCD 1H Delay Line for PAL

Description

The CXL5508M/P are CMOS-CCD delay line ICs that provide 1H delay time for PAL signals, including the external low-pass filter.

Features

- Single 5V power supply
- Low power consumption 60mW (Typ.)
- Built-in peripheral circuits

Functions

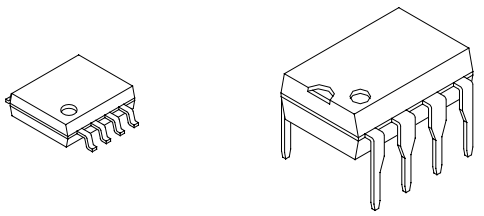
- 565-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample-and-hold circuit

Structure

CMOS-CCD

CXL5508M
8 pin SOP (Plastic)

CXL5508P
8 pin DIP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5508M	350	mW
	CXL5508P	480	mW

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

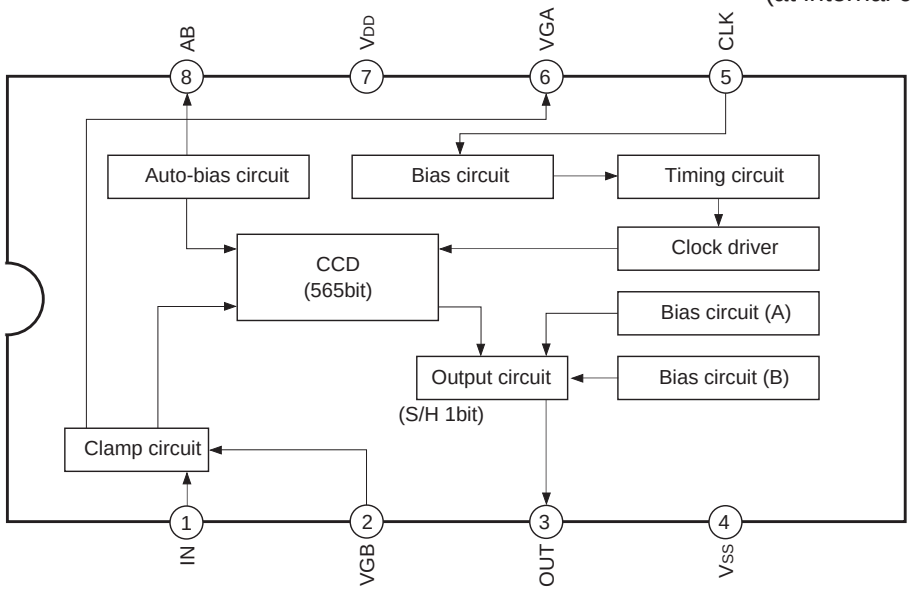
Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0 (0.5Vp-p typ.)	Vp-p
• Clock frequency	f_{CLK}	8.867238	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 527mVp-p (Max.)
(at internal clamp condition)

Blook Diagram and Pin Configuration (Top View)



E91101A7X-PS

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	VGB	I	Gate control B	
3	OUT	O	Signal output	40 to 500Ω
4	V_{SS}	—	GND	
5	CLK	I	Clock input	> 100kΩ
6	VGA	O	Gate control A	
7	V_{DD}	—	Power supply (5V)	
8	AB	O	Auto-bias DC output	600 to 200kΩ

Description of I/O Signals

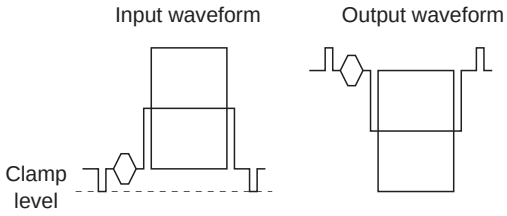
Input signals are low level clamped and output signals are inverted in relation to the input signals. Also, the clamp condition of input signals are controlled by VGB (Pin 2) conditions.

0V ..... Internal clamp condition

5V ..... Non internal clamp condition

Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).

In this mode, the input signal is limited to APL 50% and the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 8.867238MHz, V_{CLK} = 500mVp-p, sine wave)

See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition					Bias condition V1 (V)	Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5						
Supply current	I_{DD}	—	a	a	b	a	—		7	12	17	mA	1
Low frequency gain	GL	200kHz, 500mVp-p, sine wave	a	a	b	a	b		–2	0	2	dB	2
Frequency response	fg	200kHz ⟷ 2MHz, 150mVp-p, sine wave	b c	a	a	b	b	2.1	–1.8	–1.8	0	dB	3
S/H pulse coupling	CP	No signal input	—	b	a	b	a	2.1	—	—	350	mVp-p	4
S/N ratio	SN	No signal input	—	b	a	b	c		54	56	—	dB	5
Linearity	LIS	5-staircase wave (For luminance signals only)	b	a	b	a	a	—	37	40	43	%	6
	LIL		b	a	b	a	a		18	20	22		
	LIC		b	a	b	a	a		56	60	64		

Notes

(1) This is the IC supply current value during clock and signal input.

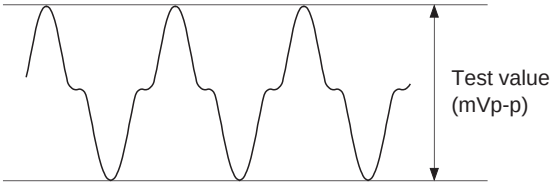
(2) GL is the output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500\ \text{[mVp-p]}}\ \text{[dB]}$$

(3) Indicates the dissipation at 2MHz in relation to 200kHz.
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 2MHz sine wave is fed to same, cal culation is made according to the following formula. Input bias is tested at 2.1V.

$$fg = 20 \log \frac{\text{OUT pin otuput voltage (2MHz) [mVp-p]}}{\text{OUT pin output voltage (200kHz) [mVp-p]}}\text{[dB]}$$

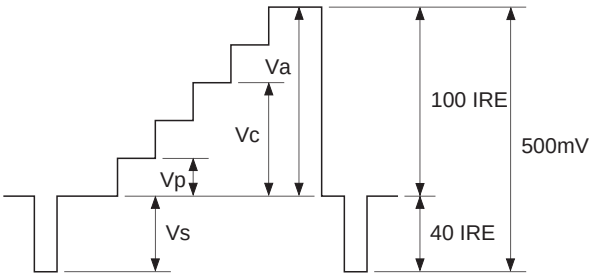
(4) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. Input bias is tested at 2.1V.



(5) Input no signal noise components are tested with the video noise meter at BPF 10kHz to 3MHz. This is calculated from the output gain (GL), at the input of 200kHz, 500mVp-p and according to the following formula.

$$S/N = -20 \cdot \log \frac{\text{Noise (mVrms)}}{0.5 \cdot 10^{GL/20}}\ \text{[dB]}$$

(6) Respective outputs are tested at the input of the 5-staircase waves seen in the figure below (Iuminance signals only) and calculated according to the formula below.
(However, output signals become inverted with regards to input.)



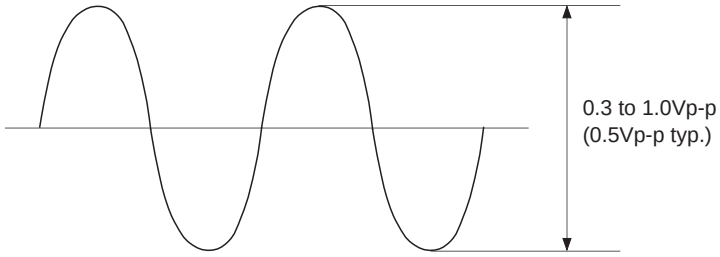
$$LIS = \frac{Vs}{Va} \times 100\ [\%]$$

$$LIL = \frac{Vp}{Va} \times 100\ [\%]$$

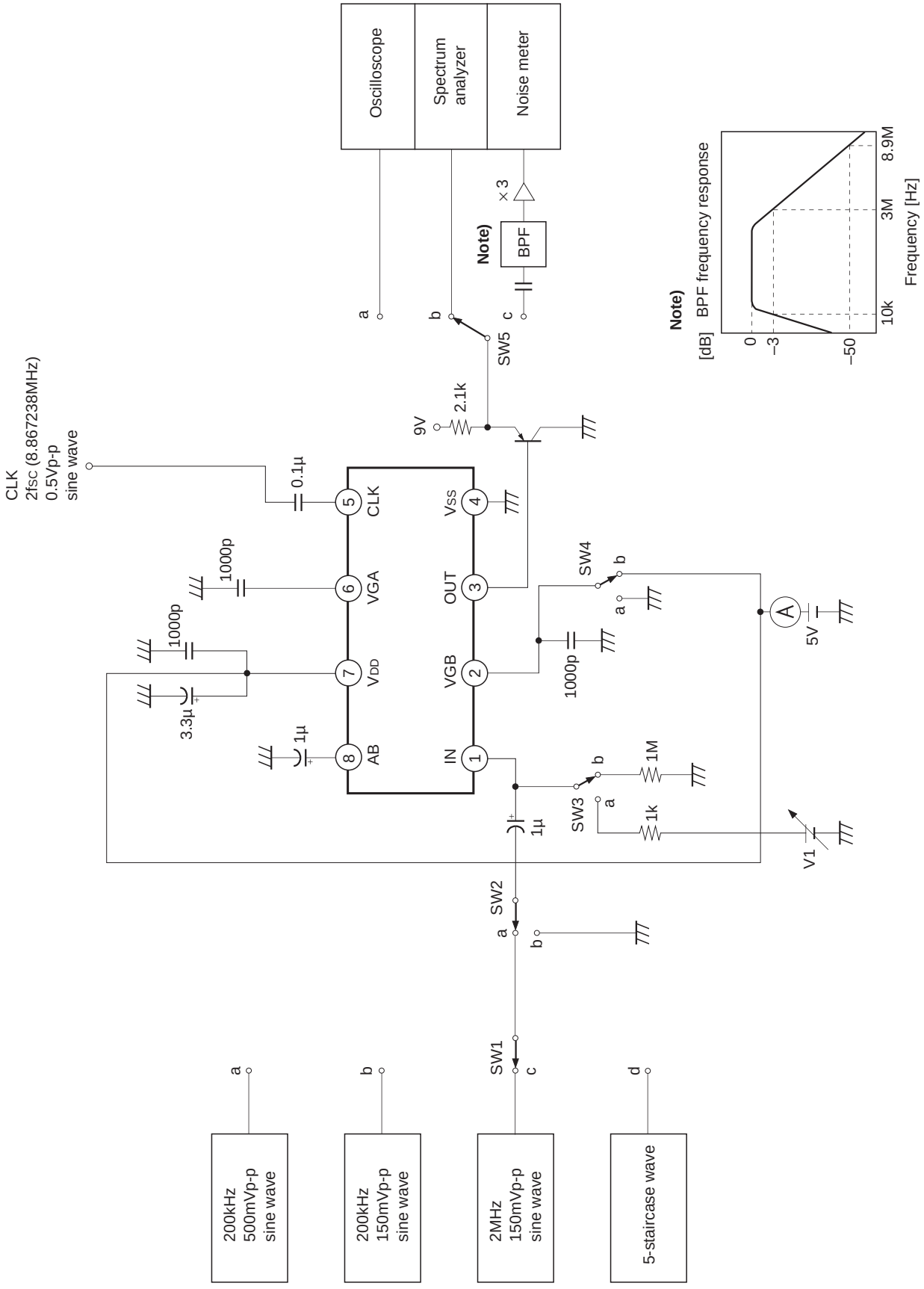
$$LIC = \frac{Vc}{Va} \times 100\ [\%]$$

Clock

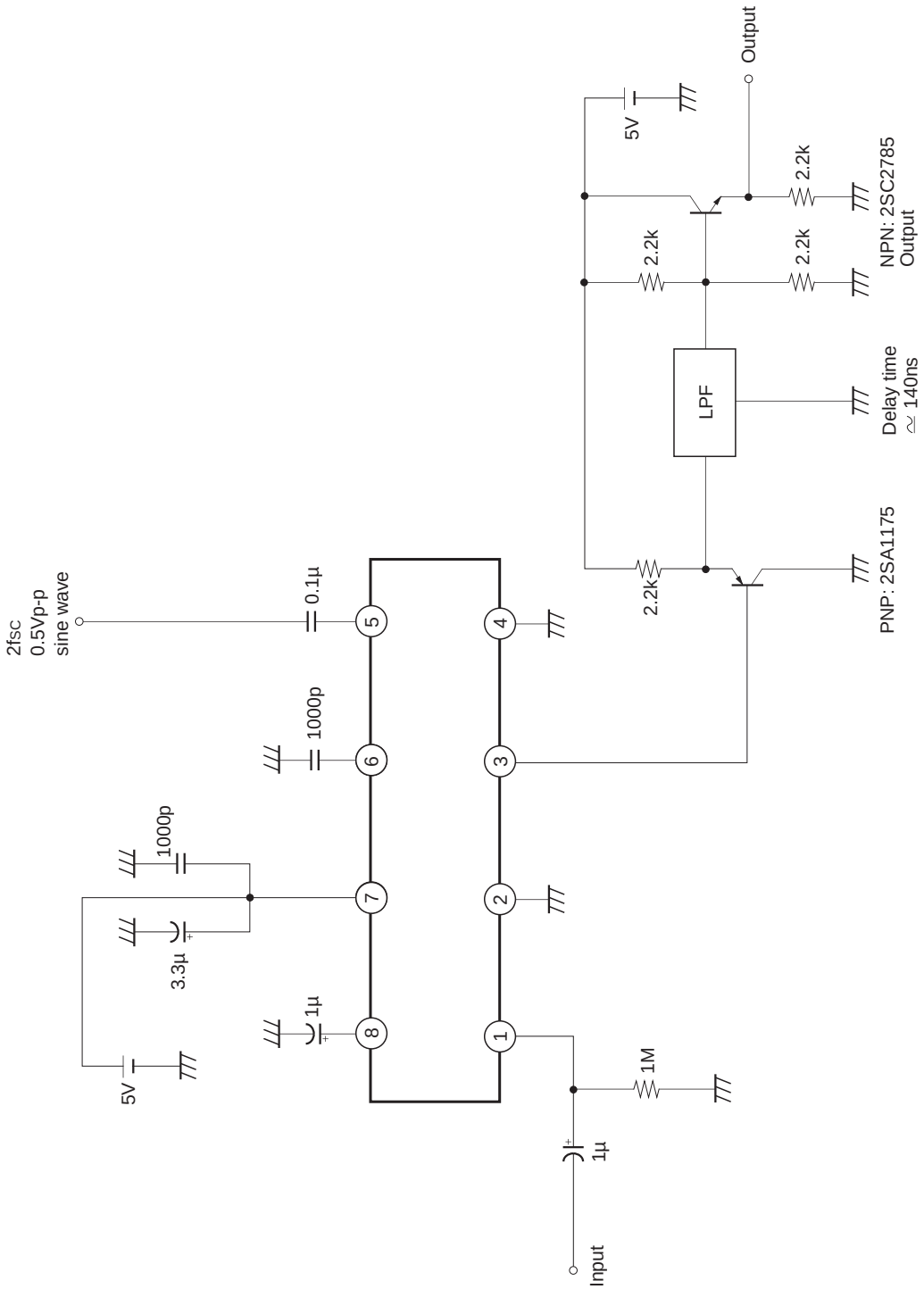
2fsc (8.867238MHz) sine wave



Electrical Characteristics Test Circuit



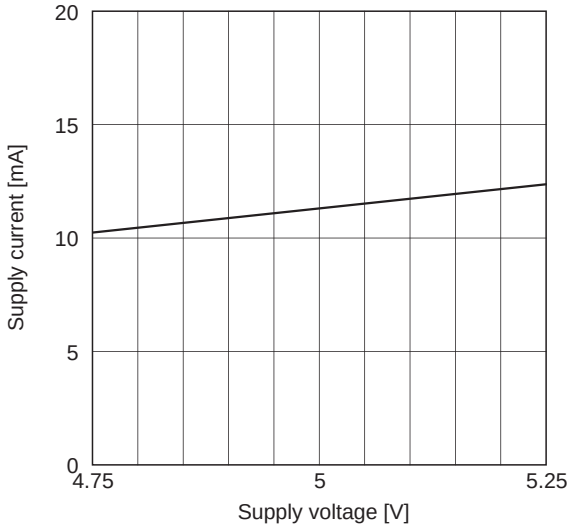
Application Circuit



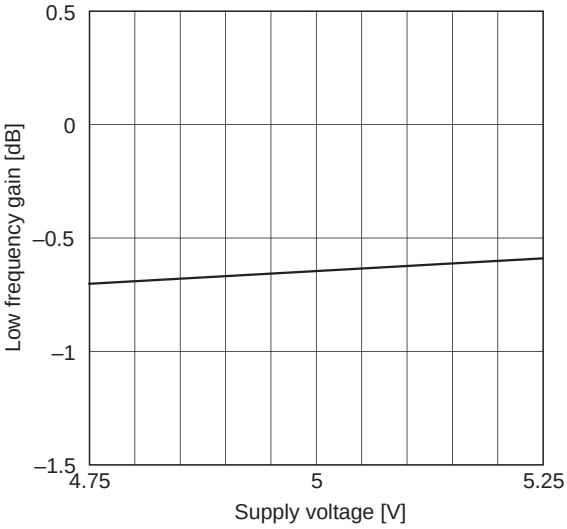
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

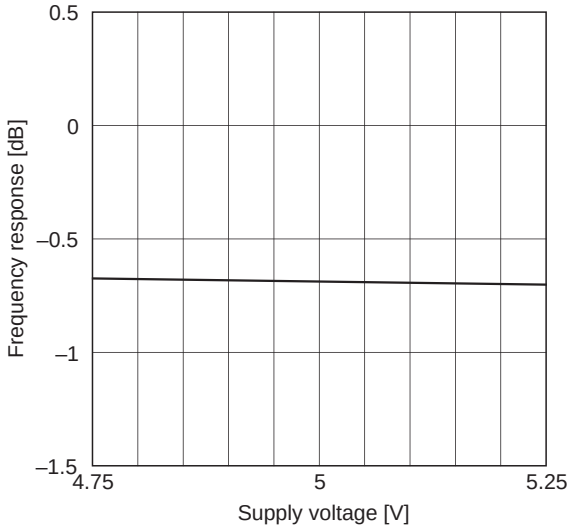
Supply current vs. Supply voltage



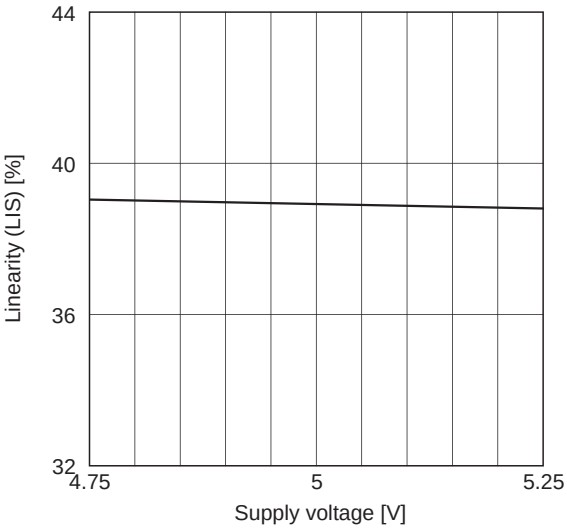
Low frequency gain vs. Supply voltage



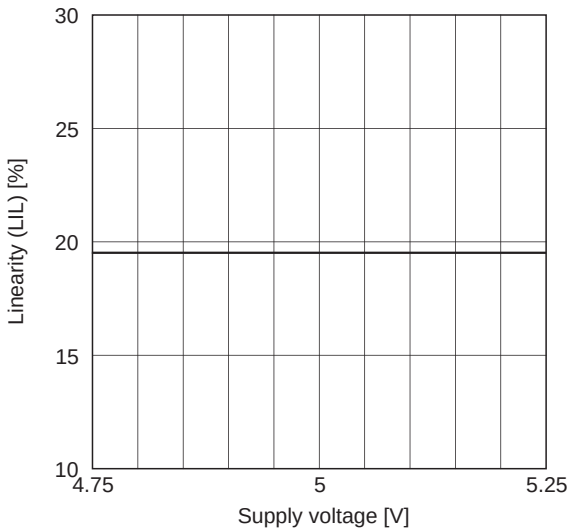
Frequency response vs. Supply voltage



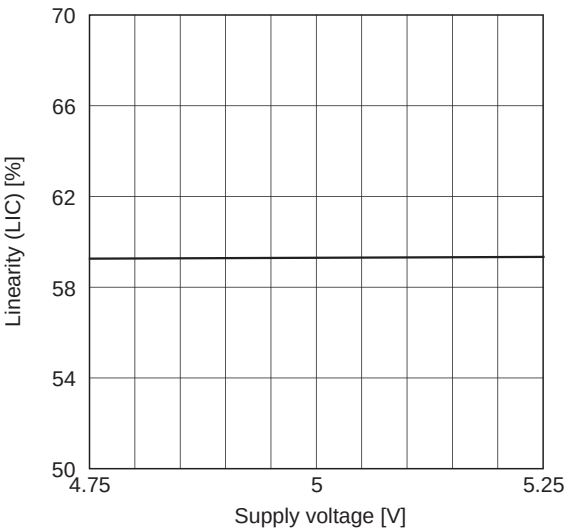
Linearity (LIS) vs. Supply voltage



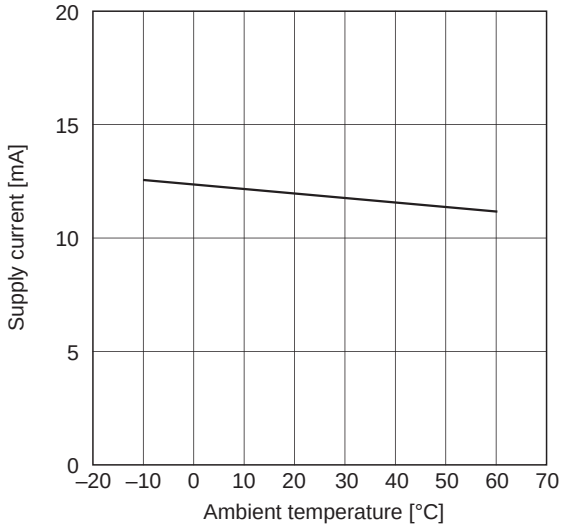
Linearity (LIL) vs. Supply voltage



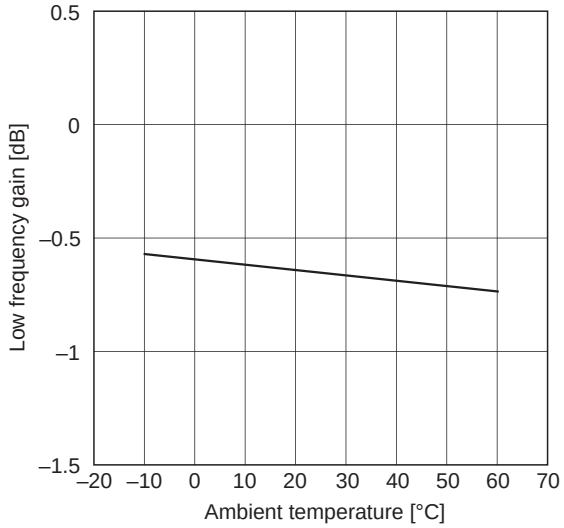
Linearity (LIC) vs. Supply voltage



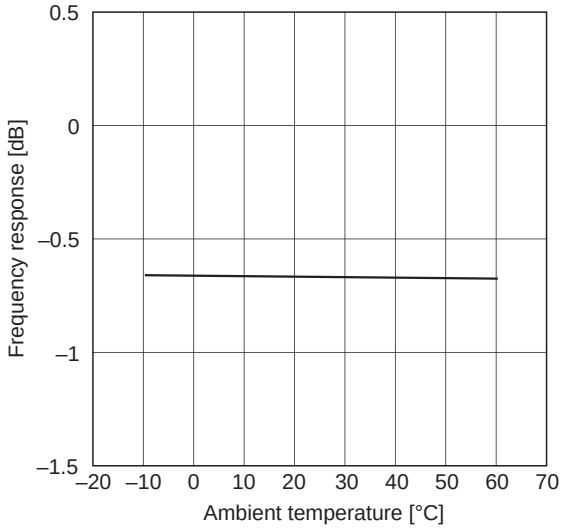
Supply current vs. Ambient temperature



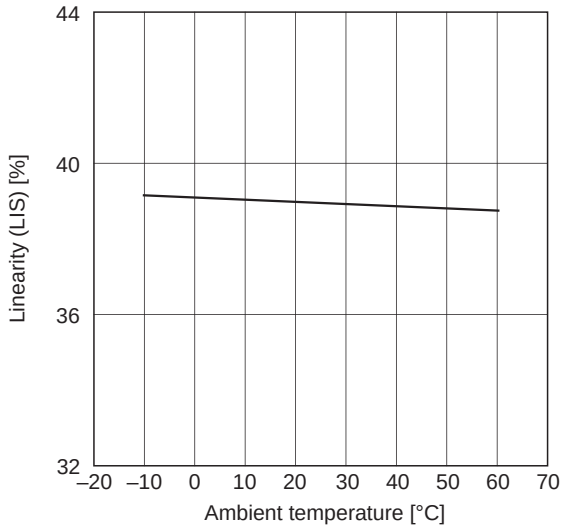
Low frequency gain vs. Ambient temperature



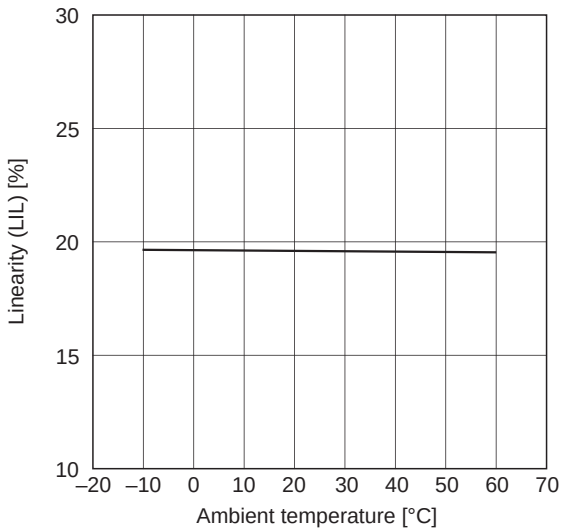
Frequency response vs. Ambient temperature



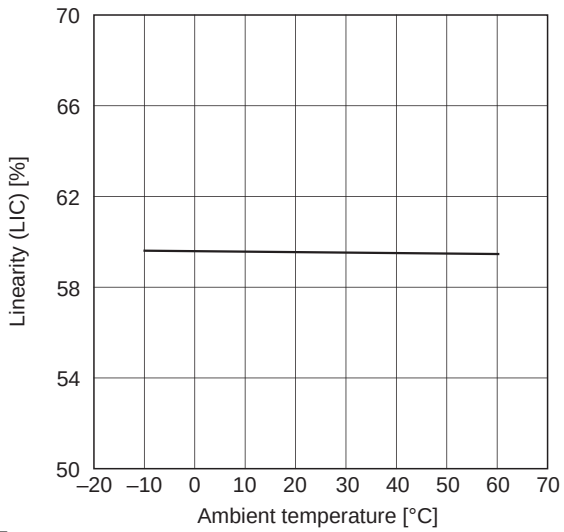
Linearity (LIS) vs. Ambient temperature



Linearity (LIL) vs. Ambient temperature



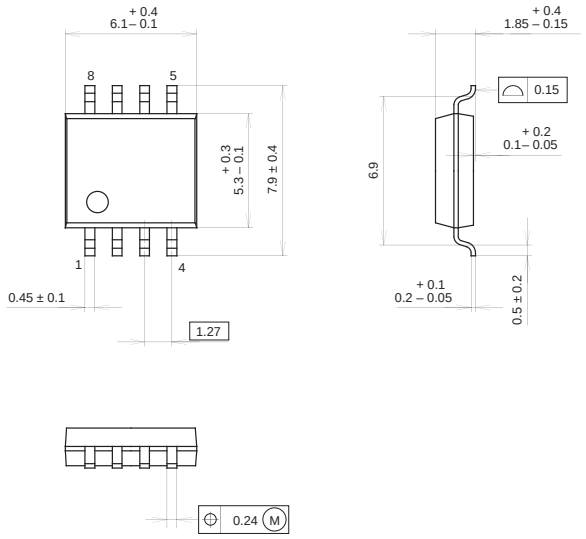
Linearity (LIC) vs. Ambient temperature



Package Outline Unit: mm

CXL5508M

8PIN SOP (PLASTIC)



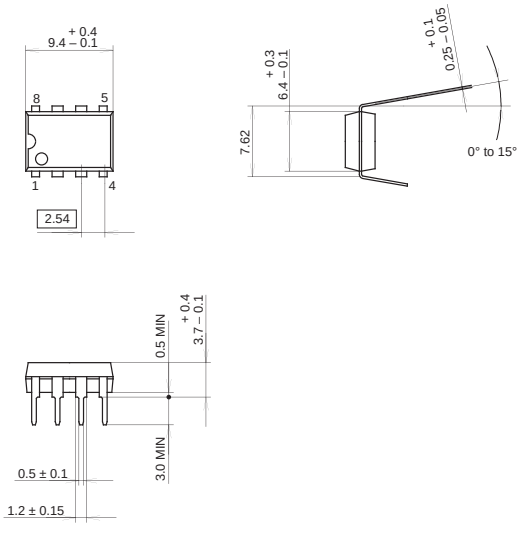
PACKAGE STRUCTURE

SONY CODE	SOP-8P-L01
EIAJ CODE	SOP008-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

CXL5508P

8PIN DIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	DIP-8P-01
EIAJ CODE	DIP008-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g