SONY

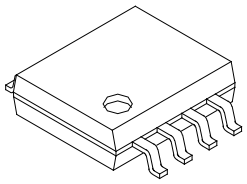
CXL5515M/P

CMOS-CCD 1H Delay Line for PAL

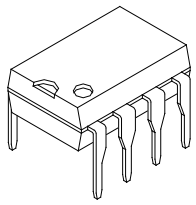
Description

The CXL5515M/P are CMOS-CCD delay line ICs designed for processing video signals. This ICs provide a 1H delay time for PAL chroma signals including the external lowpass filter.

CXL5515M
8 pin SOP (Plastic)



CXL5515P
8 pin DIP (Plastic)



Features

- Single 5V power supply
- Low power consumption
- Built-in peripheral circuit
- Built-in tripling PLL circuit
- Center bias mode

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5515M	350	mW
	CXL5515P	480	mW

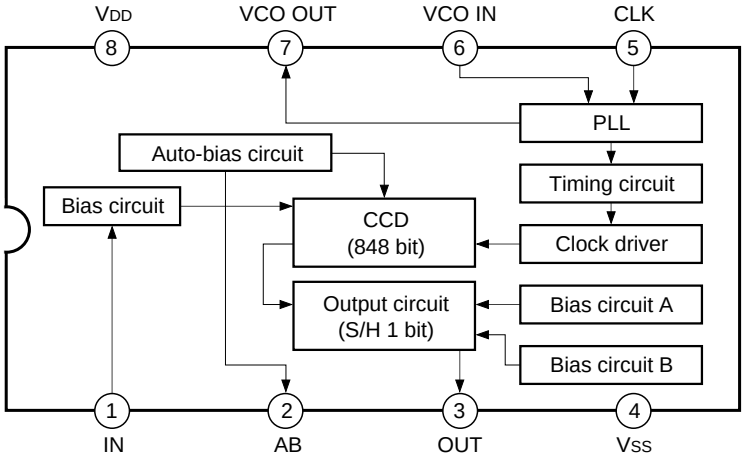
Recommended Operating Range (Ta = 25˚C)

V_{DD} 5V ± 5%

Recommended Clock Conditions (Ta = 25˚C)

- Input clock amplitude
  V_{CLK} 0.2 to 1.0Vp-p (0.4Vp-p Typ.)
- Clock frequency f_{CLK} 4.433619MHz
- Input clock waveform Sine wave

Block Diagram and Pin Configuration (Top View)



Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 575mVp-p (Max.)

Functions

- 848-bit CCD register
- Clock driver
- Auto bias circuit
- Input center bias circuit
- Sample and hold circuit
- Tripling PLL circuit
- Inverted output

Structure

CMOS-CCD

E94904-ST

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	>10KΩ
2	AB	O	Auto-bias DC output	
3	OUT	O	Signal output	40 to 500Ω
4	V_{SS}	—	GND	
5	CLK	I	Clock input (fsc)	>10KΩ
6	VCO IN	I	VCO input	
7	VCO OUT	O	VCO output (3fsc)	
8	V_{DD}	—	5V power supply	

Electrical Characteristics

($Ta = 25°C$, V_{DD}=5V, f_{CLK} = 4.433619MHz, V_{CLK} = 400mVp-p, sine wave)
See “Electrical Characteristics Test Circuit”.

Item	Symbol	Conditions	SW conditions		Min.	Typ.	Max.	Unit	NOTE
			1	2					
Supply current	I_{DD}	—	a	—	10	15	20	mA	1
Low frequency gain	GL	200kHz 500mVp-p Sine wave	a	b	–2	0	2	dB	2
Frequency response	f_R	200kHz ⟷ 4.434MHz 150mVp-p Sine wave	b ⟷ c	b	–2.7	–1.7	2.7	dB	3
Differential gain	DG	5-staircase wave (See Note 4.)	d	c	0	3	5	%	4
Differential phase	DP	5-staircase wave (See Note 4.)	d	c	0	3	5	degree	4
S/H pulse coupling	CP	No signal input	f	a	—	—	350	mVp-p	5
S/N ratio	SN	50% white video signal (See Note 6.)	e	d	52	56	—	dB	6

NOTE

1. This is the IC supply current value during clock and signal input.

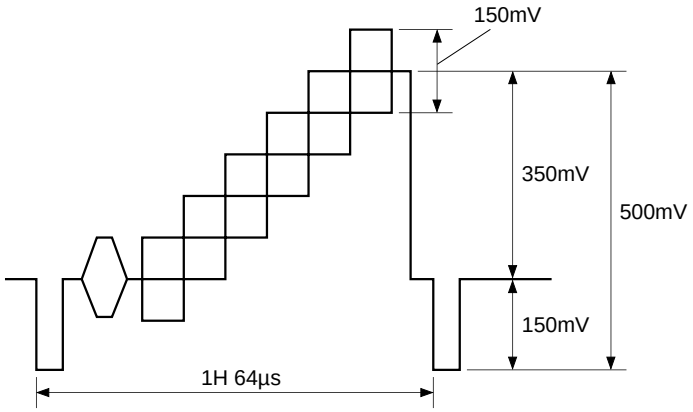
2. GL is the output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

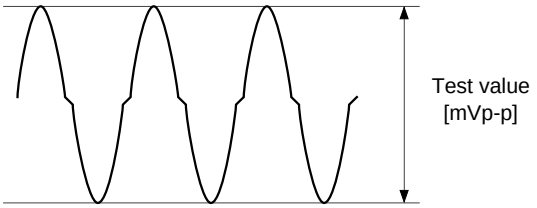
3. Indicates the dissipation at 4.434MHz in relation to 200kHz. From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 4.434MHz sine wave is fed to the same, calculation is made according to the following formula.

$$f_R = 20 \log \frac{\text{OUT pin output voltage (4.434MHz) [mVp-p]}}{\text{OUT pin output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

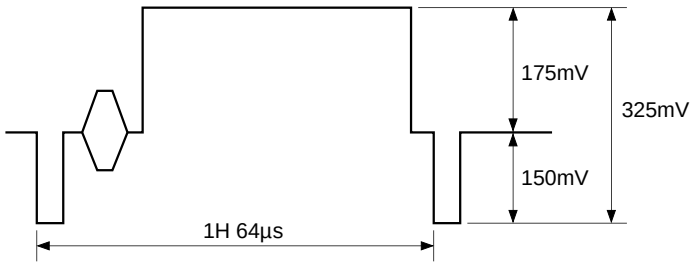
4. In Fig. below, the differential gain (DG) and the differential phase (DP), are tested with a vector scope when the 5-staircase wave is fed.



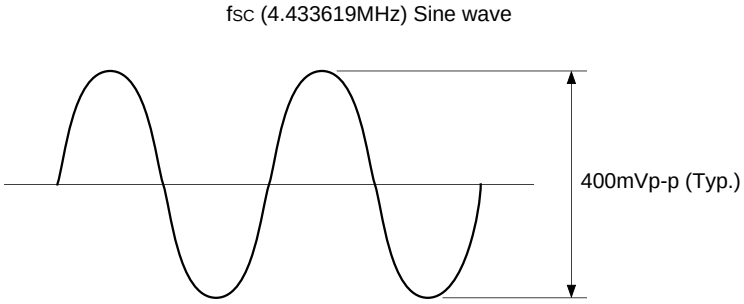
5. Leakage of internal clock components and related high frequency component to the output signal, during no signal input, is tested.



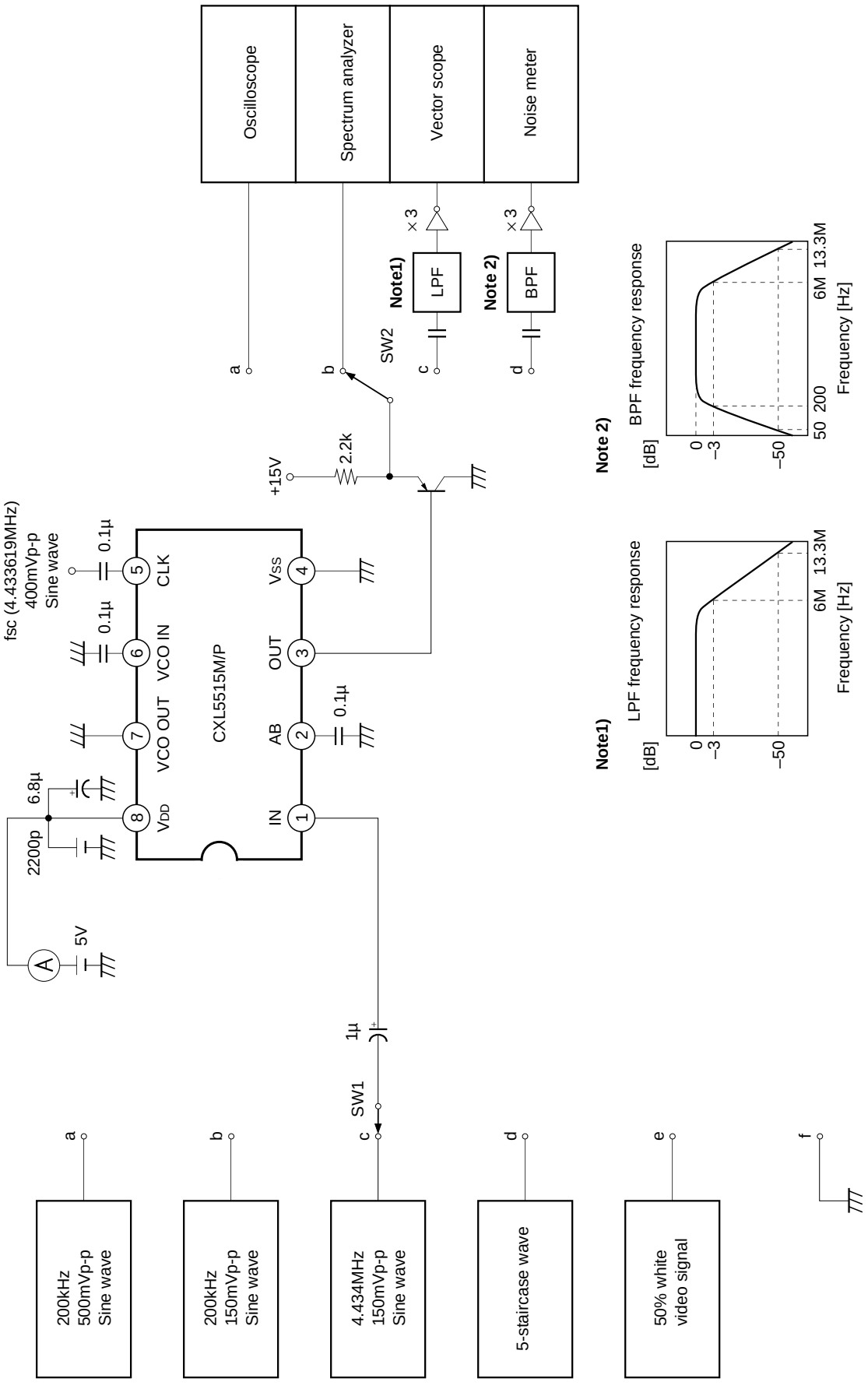
6. S/N ratio during a 50% white video signal input shown in Fig. below is tested at the video noise meter, in BPF 100kHz to 5MHz, Sub Carrier Trap mode.



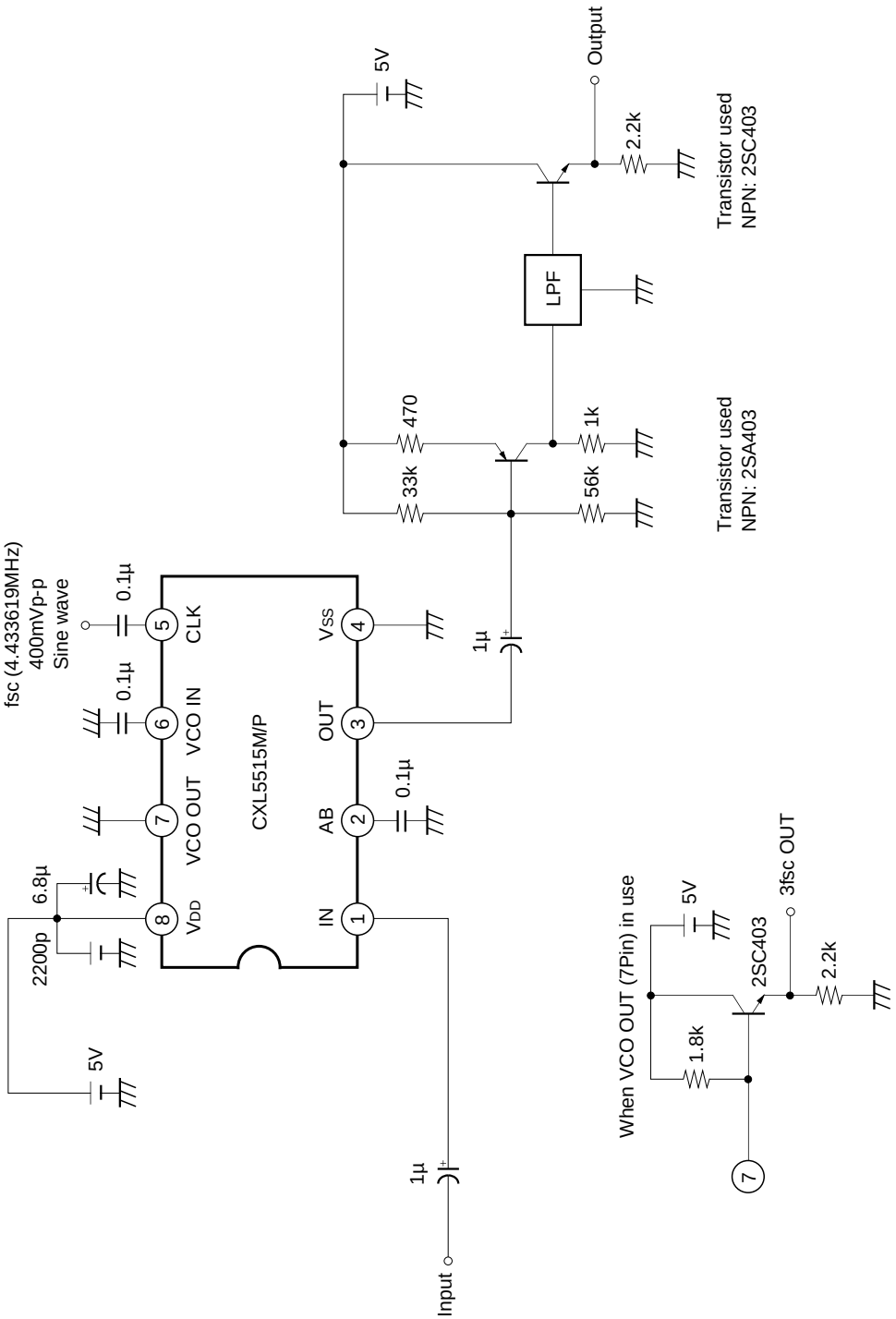
CLOCK



Electrical Characteristics Test Circuit



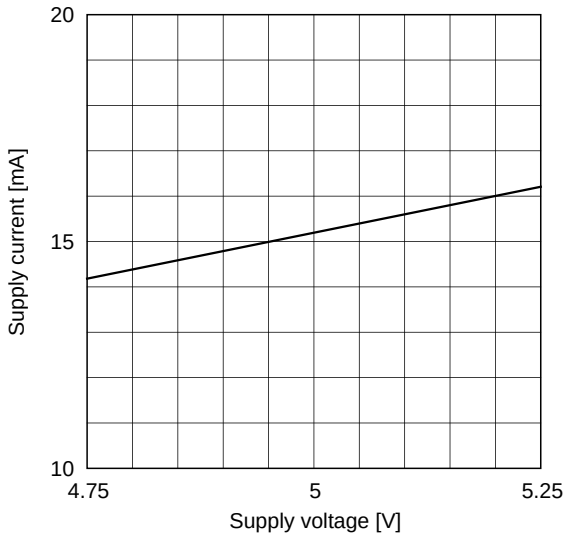
Application Circuit



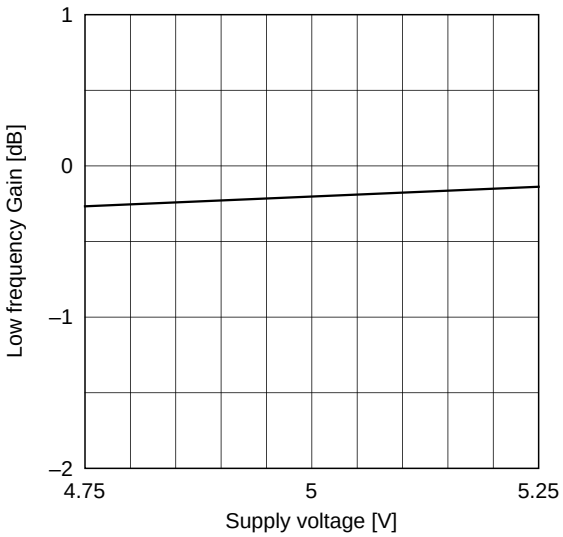
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

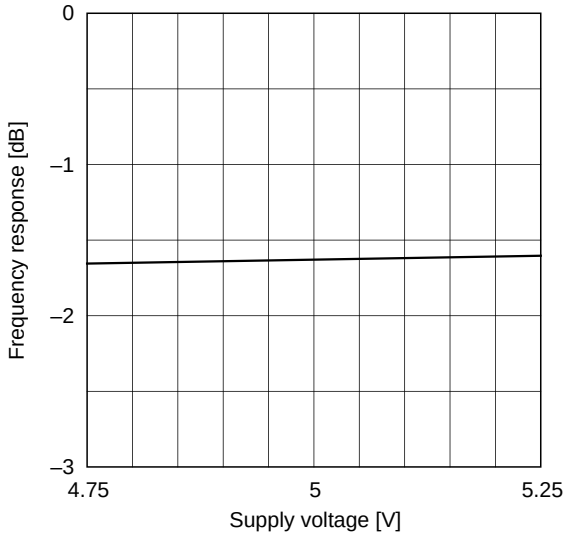
Supply current vs. Supply voltage



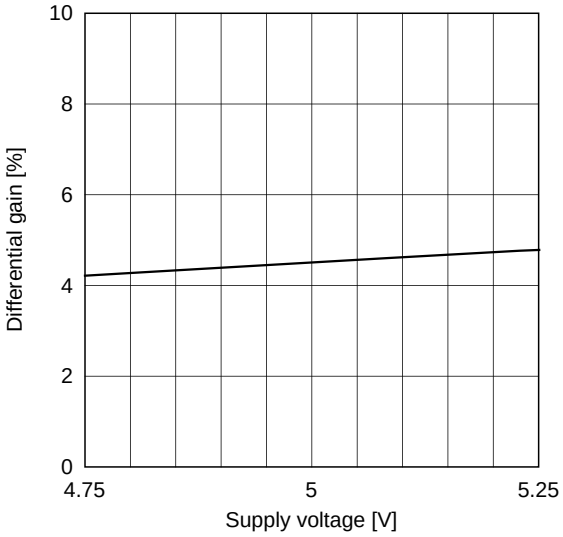
Low frequency Gain vs. Supply voltage



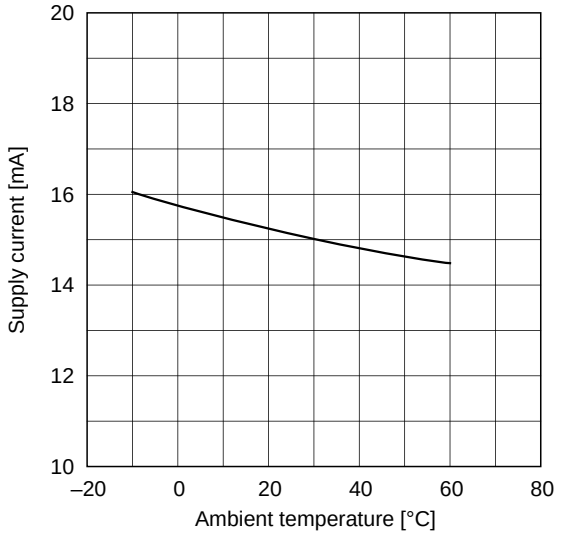
Frequency response vs. Supply voltage



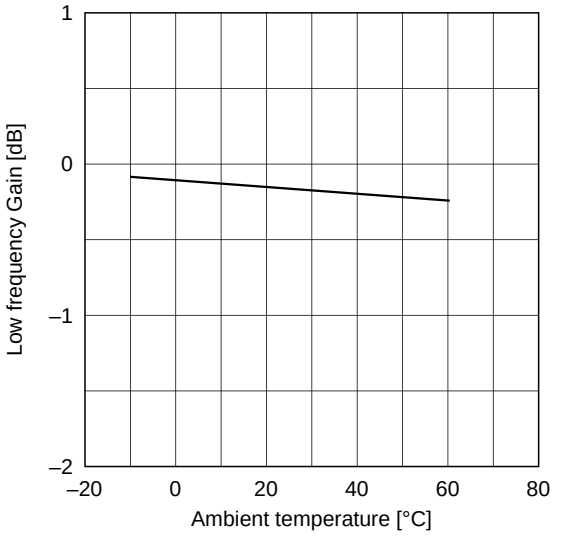
Differential gain vs. Supply voltage



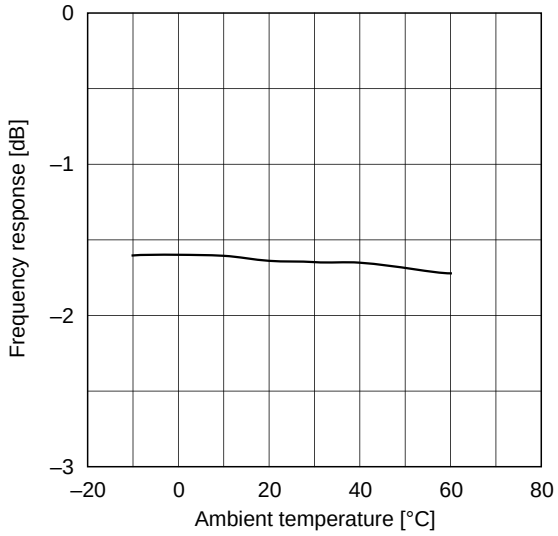
Supply current vs. Ambient temperature



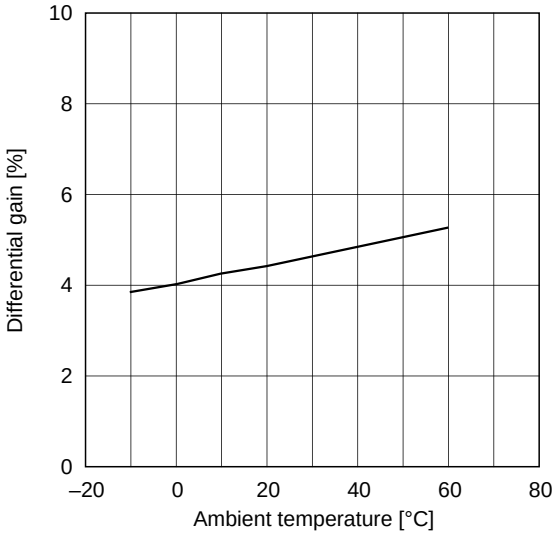
Low frequency Gain vs. Ambient temperature



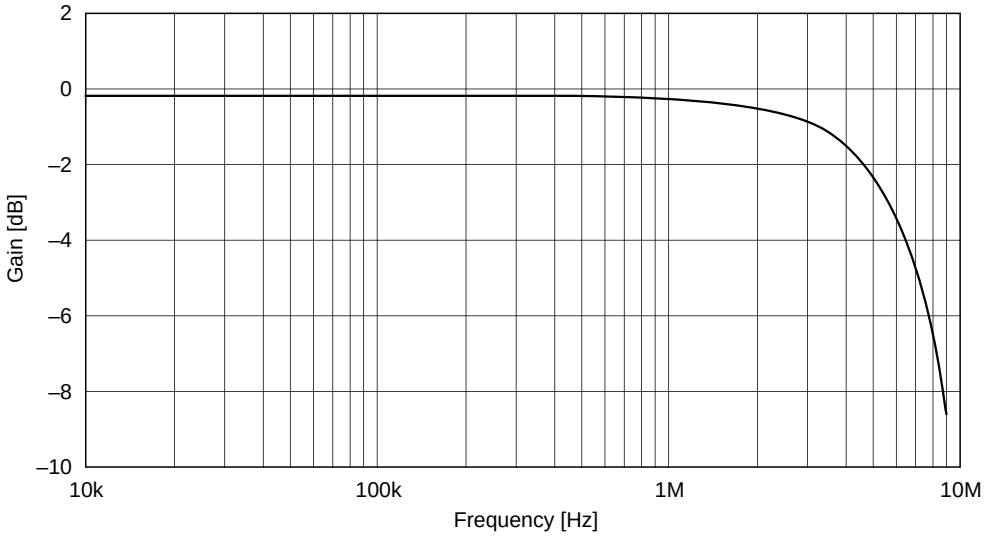
Frequency response vs. Ambient temperature



Differential gain vs. Ambient temperature



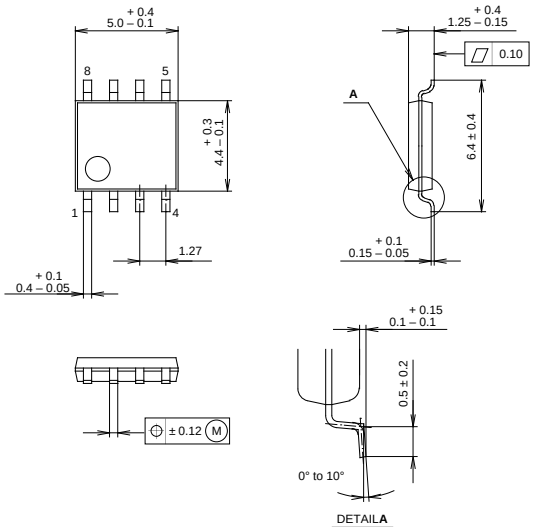
Frequency response



Package Outline Unit : mm

CXL5515M

8PIN SOP (PLASTIC)



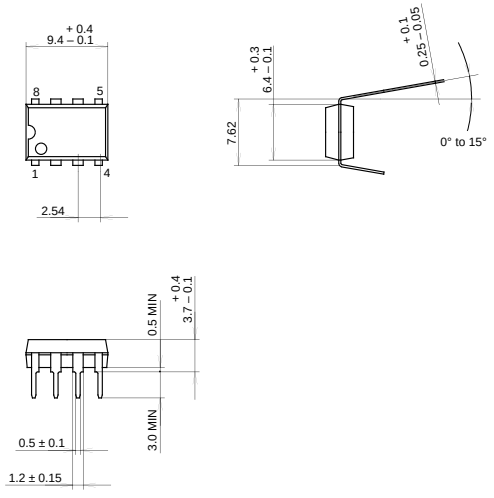
PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.1g

SONY CODE	SOP-8P-L03
EIAJ CODE	∗SOP008-P-0225-A
JEDEC CODE	

CXL5515P

8PIN DIP (PLASTIC) 300mil



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.5g

SONY CODE	DIP-8P-01
EIAJ CODE	∗DIP008-P-0300-A
JEDEC CODE	