CY74FCT16827T
CY74FCT162827T

20-Bit Buffers

Features

- **Low power, pin compatible replacement for ABT functions**
- **FCT-C speed at 4.2 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16827T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162827T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C**

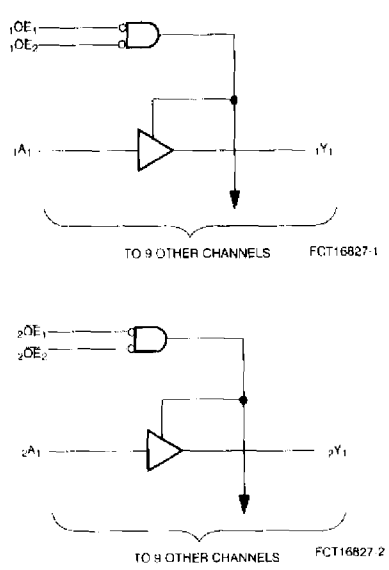
Functional Description

The CY74FCT16827T 20-bit buffer/line driver and the CY74FCT162827T 20-bit buffer/line driver provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. These parts can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed $\overline{OE}$ for increased flexibility. The outputs are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16827T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

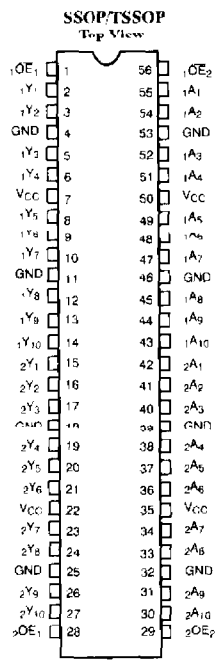
The CY74FCT162827T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162827T is ideal for driving transmission lines.

Logic Block Diagrams



Pin Configuration

SSOP/TSSOP
Top View



FCT16827-3

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162827T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	Condition[11]	74FCT16827AT 74FCT162827AT		74FCT16827BT 74FCT162827BT		74FCT16827CT 74FCT162827CT		Unit	Fig. No.[13]
			Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to Y	C_L=50 pF R_L=500Ω	1.5	8.0	1.5	5.0	1.5	4.2	ns	1, 3
		C_L=300 pF[3] R_L=500Ω	1.5	15.0	1.5	13.0	1.5	10.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	12.0	1.5	8.0	1.5	5.6	ns	1, 7, 8
		C_L=300 pF[3] R_L=500Ω	1.5	23.0	1.5	15.0	1.5	14.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y	C_L=5 pF[3] R_L=500Ω	1.5	9.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	10.0	1.5	7.0	1.5	6.0		
$t_{SK(O)}$	Output Skew[14]		—	0.5	—	0.5	—	0.5	ns	—

Ordering Information CY74FCT16827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16827CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827CTPVC	O56	56-Lead (300-Mil) SSOP	
5.0	CY74FCT16827BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827BTPVC	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT16827ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16827ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT162827CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827CTPVC	O56	56-Lead (300-Mil) SSOP	
5.0	CY74FCT162827BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827BTPVC	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT162827ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162827ATPVC	O56	56-Lead (300-Mil) SSOP	

Notes:
11. See test circuit and waveforms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information Section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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