Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{MR}=V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{MR}=V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{MR}=V_{CC}$, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{MR}=V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{MR}=V_{CC}$, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT273CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT273CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT273CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.5	CY54FCT273CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT273CTLMB	L61	20-Square Leadless Chip Carrier	
7.2	CY74FCT273ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT273ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT273ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.3	CY54FCT273ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT273ATLMB	L61	20-Square Leadless Chip Carrier	
13.0	CY74FCT273TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT273TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT273TSOC	S5	20-Lead (300-Mil) Molded SOIC	
15.0	CY54FCT273TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT273TLMB	L61	20-Square Leadless Chip Carrier	

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