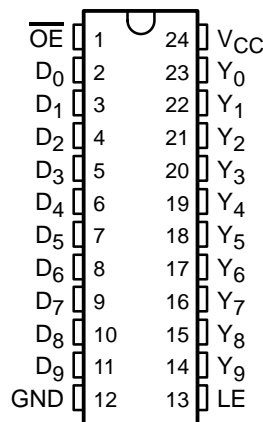


# CY54FCT841T, CY74FCT841T 10-BIT LATCHES WITH 3-STATE OUTPUTS

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- Function, Pinout, and Drive Compatible With FCT, F, and AM29841 Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- High-Speed Parallel Latches
- Buffered Common Latch-Enable Input
- 3-State Outputs
- CY54FCT841T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT841T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current

CY54FCT841T . . . D PACKAGE  
CY74FCT841T . . . P, Q, OR SO PACKAGE  
(TOP VIEW)



## description

The 'FCT841T bus-interface latches are designed to eliminate additional packages required to buffer existing latches and provide additional data width for wider address/data paths or buses carrying parity. The 'FCT841T devices are buffered 10-bit-wide versions of the FCT373 function.

The 'FCT841T devices' high-performance interface is designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	Latch data inputs
LE	I	Latch-enable input. The latches are transparent when LE is high. Input data is latched on the high-to-low transition.
Y	O	3-state latch outputs
$\overline{OE}$	I	Output-enable control. When $\overline{OE}$ is low, the outputs are enabled. When $\overline{OE}$ is high, the outputs are in the high-impedance (off) state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CY54FCT841T, CY74FCT841T

## 10-BIT LATCHES

### WITH 3-STATE OUTPUTS

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#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	5.5	CY74FCT841CTQCT	FCT841C
	SOIC – SO	Tube	5.5	CY74FCT841CTSOC	FCT841C
		Tape and reel	5.5	CY74FCT841CTSOCT	
	DIP – P	Tube	6.5	CY74FCT841BTPC	CY74FCT841BTPC
	SOIC – SO	Tube	9	CY74FCT841ATSOC	FCT841A
Tape and reel		9	CY74FCT841ATSOCT		
-55°C to 125°C	CDIP – D	Tube	10	CY54FCT841ATDMB	

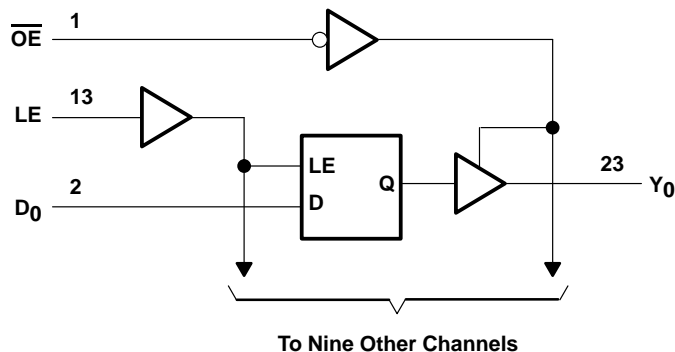
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	LE	D	O	Y	
H	X	X	X	Z	Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

H = High logic level, L = Low logic level, X = Don't care, NC = No change, Z = High-impedance state

#### logic diagram (positive logic)



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**CY54FCT841T, CY74FCT841T**  
**10-BIT LATCHES**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		CY54FCT841T			CY74FCT841T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-0.7	-1.2				V	
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA					-0.7	-1.2		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA		2.4	3.3				V	
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA			2				
		I <sub>OH</sub> = -15 mA			2.4	3.3			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA		0.3	0.55				V	
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA					0.3	0.55		
V <sub>hys</sub>	All inputs		0.2			0.2		V	
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>				5			μA	
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>						5		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V				±1			μA	
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V						±1		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V				±1			μA	
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V						±1		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V				10			μA	
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V						10		
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V				-10			μA	
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V						-10		
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V		-60	-120	-225			mA	
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V					-60	-120		-225
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V				±1		±1	μA	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.1	0.2				mA	
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V					0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open		0.5	2				mA	
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open					0.5	2		
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.5 V, One input switching at 50% duty cycle, Outputs open, OE = GND, LE = V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.06	0.12				mA/ MHz	
	V <sub>CC</sub> = 5.25 V, One input switching at 50% duty cycle, Outputs open, OE = GND, LE = V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V					0.06	0.12		

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

¶ This parameter is derived for use in total power-supply calculations.



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**10-BIT LATCHES**  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS		CY54FCT841T		CY74FCT841T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I <sub>C</sub> #	V <sub>CC</sub> = 5.5 V, Outputs open, OE = GND, LE = V <sub>CC</sub>	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	0.7	1.4		mA	
			V <sub>IN</sub> = 3.4 V or GND	1	2.4			
		10 bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	1	3.2			
			V <sub>IN</sub> = 3.4 V or GND	4.1	13.2			
	V <sub>CC</sub> = 5.25 V, Outputs open, OE = GND, LE = V <sub>CC</sub>	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V			0.7		1.4
			V <sub>IN</sub> = 3.4 V or GND			1		2.4
		10 bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V			1		3.2
			V <sub>IN</sub> = 3.4 V or GND			4.1		13.2
C <sub>i</sub>			5	10	5	10	pF	
C <sub>o</sub>			9	12	9	12	pF	

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

# I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		CY54FCT841AT		CY74FCT841AT		CY74FCT841BT		CY74FCT841CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	5		4		4		4		ns
t <sub>su</sub>	Setup time, data before LE↑	2.5		2.5		2.5		2.5		ns
t <sub>h</sub>	Hold time, data after LE↑	3		2.5		2.5		2.5		ns



**CY54FCT841T, CY74FCT841T**  
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**switching characteristics over operating free-air temperature range (see Figure 1)**

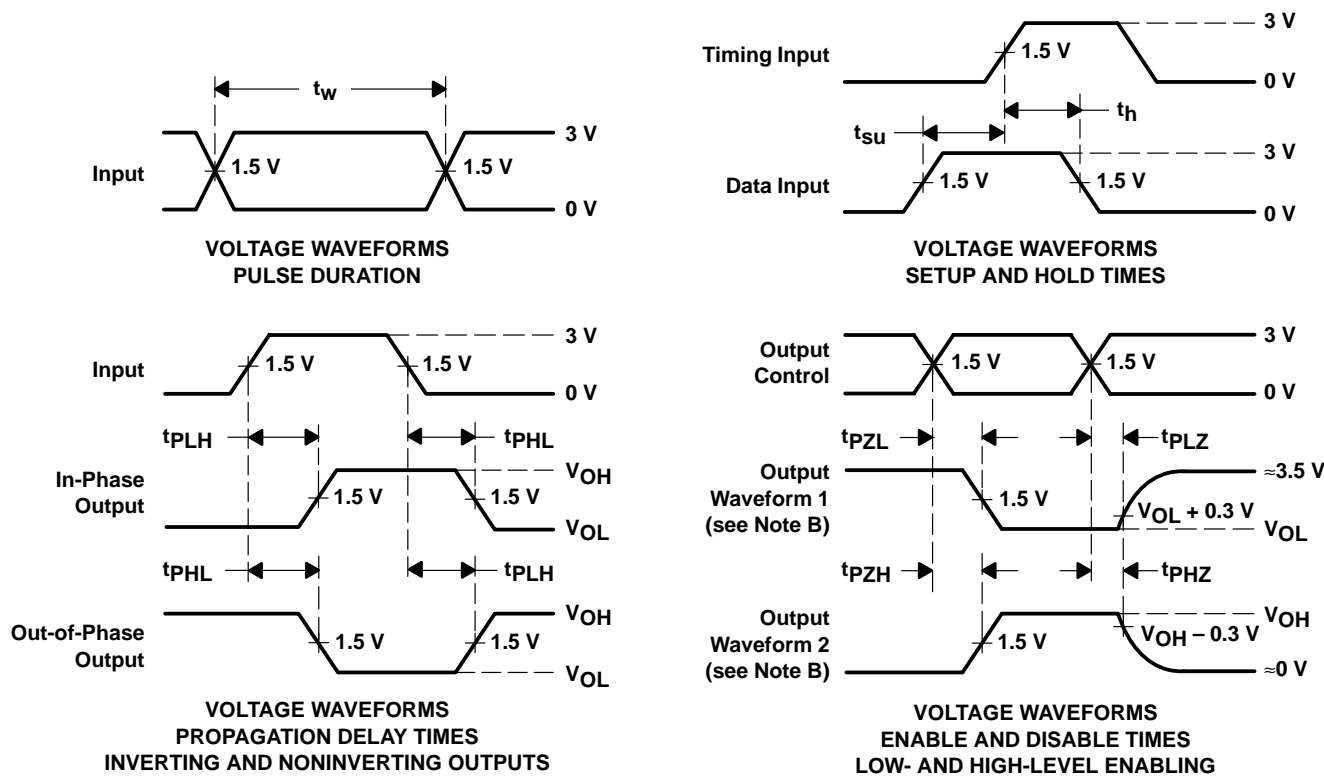
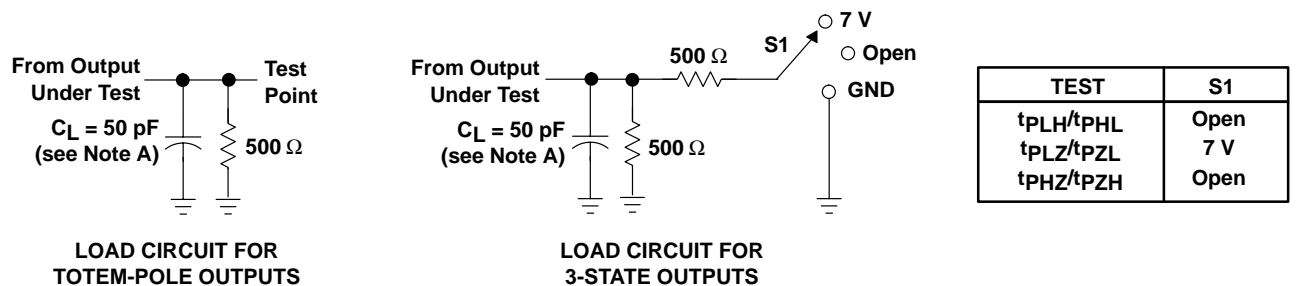
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT841AT		CY74FCT841AT		UNIT
				MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	10	1.5	9	ns
t <sub>PHL</sub>				1.5	10	1.5	9	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	15	1.5	13	ns
t <sub>PHL</sub>				1.5	15	1.5	13	
t <sub>PLH</sub>	LE	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	13	1.5	12	ns
t <sub>PHL</sub>				1.5	13	1.5	12	
t <sub>PLH</sub>	LE	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	20	1.5	16	ns
t <sub>PHL</sub>				1.5	20	1.5	16	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	13	1.5	11.5	ns
t <sub>PZL</sub>				1.5	13	1.5	11.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	25	1.5	23	ns
t <sub>PZL</sub>				1.5	25	1.5	23	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 500 Ω	1.5	9	1.5	7	ns
t <sub>PLZ</sub>				1.5	9	1.5	7	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	10	1.5	8	ns
t <sub>PLZ</sub>				1.5	10	1.5	8	

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT841BT		CY74FCT841CT		UNIT
				MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	6.5	1.5	5.5	ns
t <sub>PHL</sub>				1.5	6.5	1.5	5.5	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	13	1.5	13	ns
t <sub>PHL</sub>				1.5	13	1.5	13	
t <sub>PLH</sub>	LE	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	8	1.5	6.4	ns
t <sub>PHL</sub>				1.5	8	1.5	6.4	
t <sub>PLH</sub>	LE	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	15.5	1.5	15	ns
t <sub>PHL</sub>				1.5	15.5	1.5	15	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	8	1.5	6.5	ns
t <sub>PZL</sub>				1.5	8	1.5	6.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	14	1.5	12	ns
t <sub>PZL</sub>				1.5	14	1.5	12	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 500 Ω	1.5	6	1.5	5.7	ns
t <sub>PLZ</sub>				1.5	6	1.5	5.7	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	7	1.5	6	ns
t <sub>PLZ</sub>				1.5	7	1.5	6	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-88575013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
CY54FCT841ATDMB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
CY54FCT841ATLMB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
CY74FCT841ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841BTPC	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT841BTPCE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT841CTQCT	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT841CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT841CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT841CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered



at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT841ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT841CTQCT	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT841CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT841ATSOCT	SOIC	DW	24	2000	346.0	346.0	41.0
CY74FCT841CTQCT	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
CY74FCT841CTSCT	SOIC	DW	24	2000	346.0	346.0	41.0

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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