



1M x 4 Static RAM

Features

- High speed
 - $t_{AA} = 10$ ns
- Low active power for 10 ns speed
 - 540 mW (max.)
- Low CMOS standby power (L version)
 - 1.8 mW (max.)
- 2.0V Data Retention (400 μ W at 2.0V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features

Functional Description

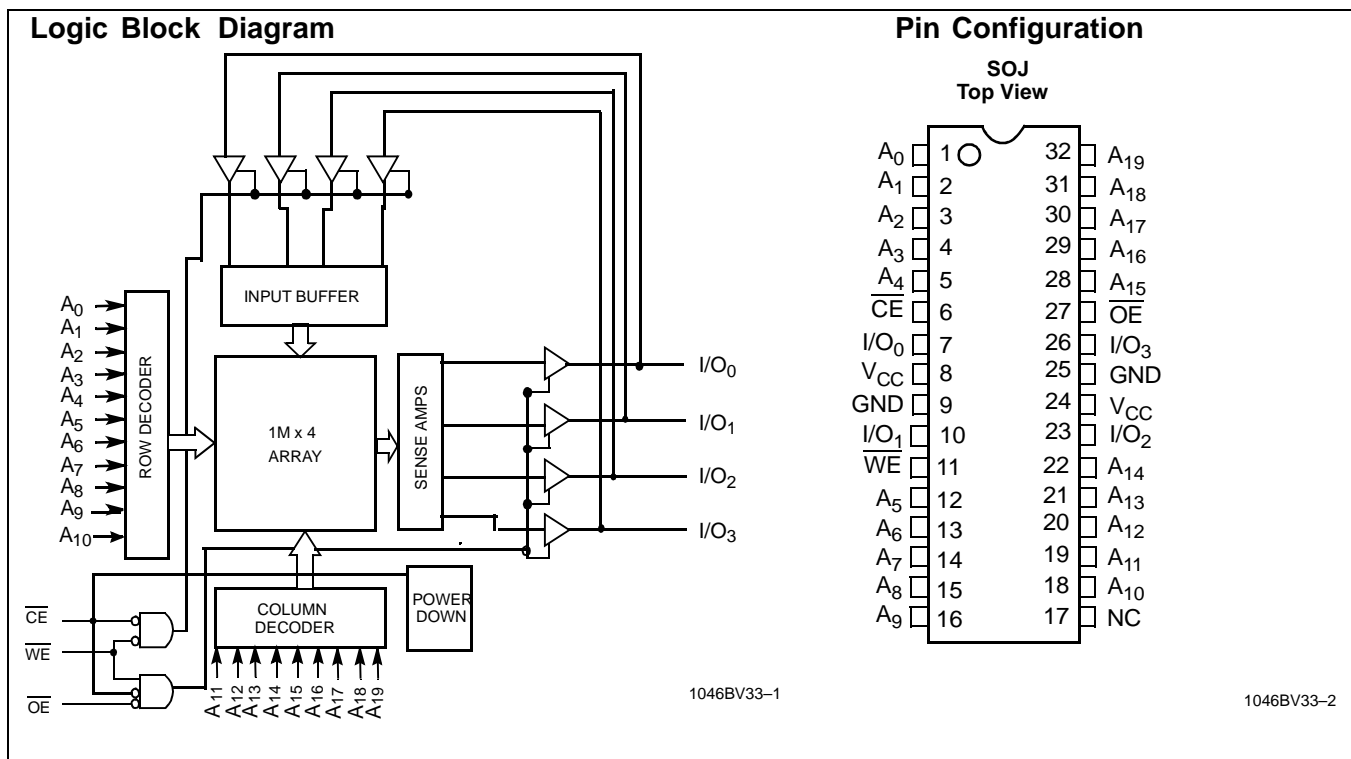
The CY7C1046BV33 is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory

expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the four I/O pins (I/O₀ through I/O₃) is then written into the location specified on the address pins (A₀ through A₁₉).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O₀ through I/O₃) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1046BV33 is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.



Selection Guide

	7C1046BV33-10	7C1046BV33-12	7C1046BV33-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	150	140	130
Maximum CMOS Standby Current (mA)	Com'l	8	8
	L version	0.5	0.5

Shaded areas contain advance information.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V
- DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

- Current into Outputs (LOW) 20 mA
- Static Discharge Voltage >2001 V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	3.0V - 3.6V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1046BV33-10		7C1046BV33-12		7C1046BV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	-1	+1	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}		150		140		130	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		20		20		20	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l	8		8		8	mA
			L version	0.5		0.5		0.5	

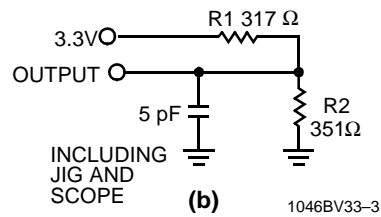
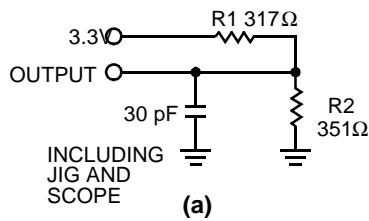
Shaded areas contain advance information.

Capacitance^[3]

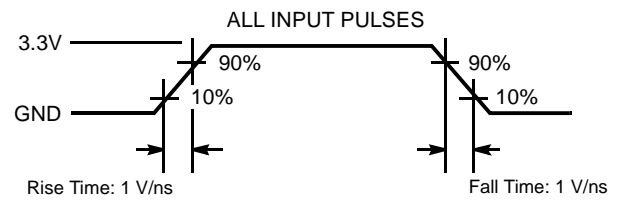
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	6	pF
C _{OUT}	I/O Capacitance		6	pF

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

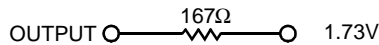
AC Test Loads and Waveforms


1046BV33-3



1046BV33-4

Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics^[4] Over the Operating Range

Parameter	Description	7C1046BV33-10		7C1046BV33-12		7C1046BV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		4		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6]	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		10		12		15	ns
WRITE CYCLE^[7, 8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	7		10		12		ns
t_{AW}	Address Set-Up to Write End	7		10		12		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	7		10		12		ns
t_{SD}	Data Set-Up to Write End	5		7		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[5, 6]		5		6		7	ns

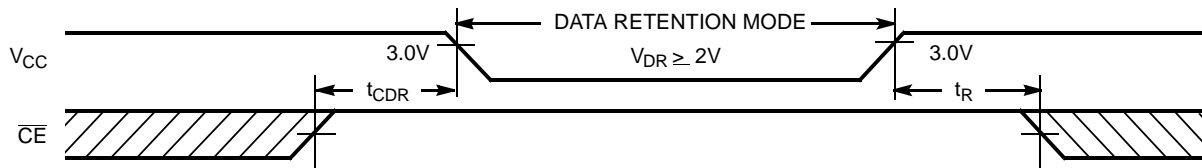
Shaded areas contain advance information.

Notes:

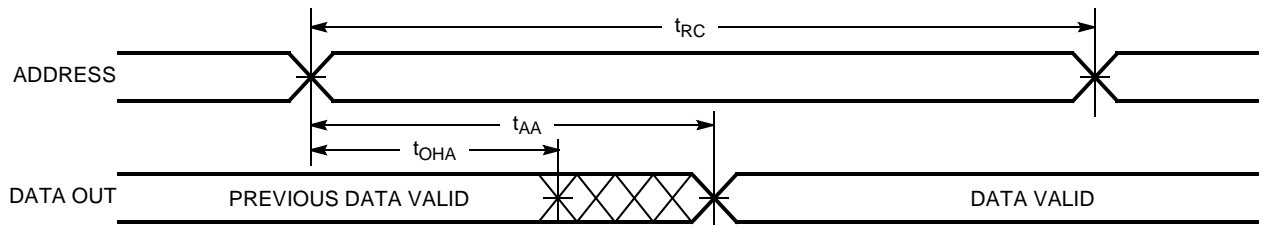
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range

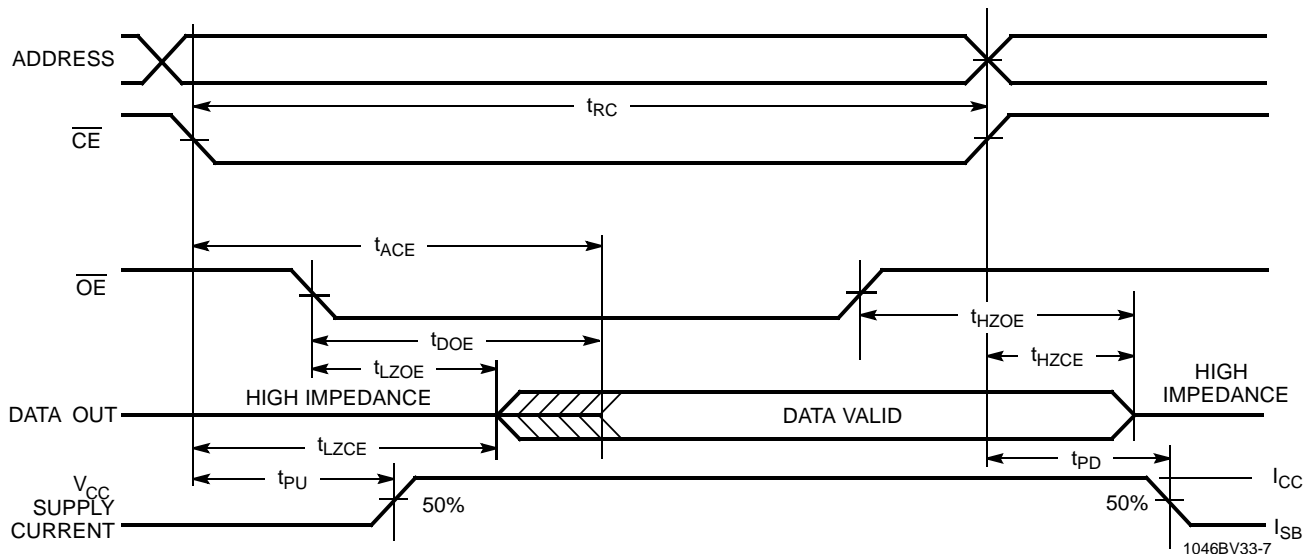
Parameter	Description	Conditions ^[10]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	Com'l		200	μ A
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[9]}$	Operation Recovery Time		10		μ s

Data Retention Waveform


1046BV33-5

Switching Waveforms
Read Cycle No. 1^[11, 12]


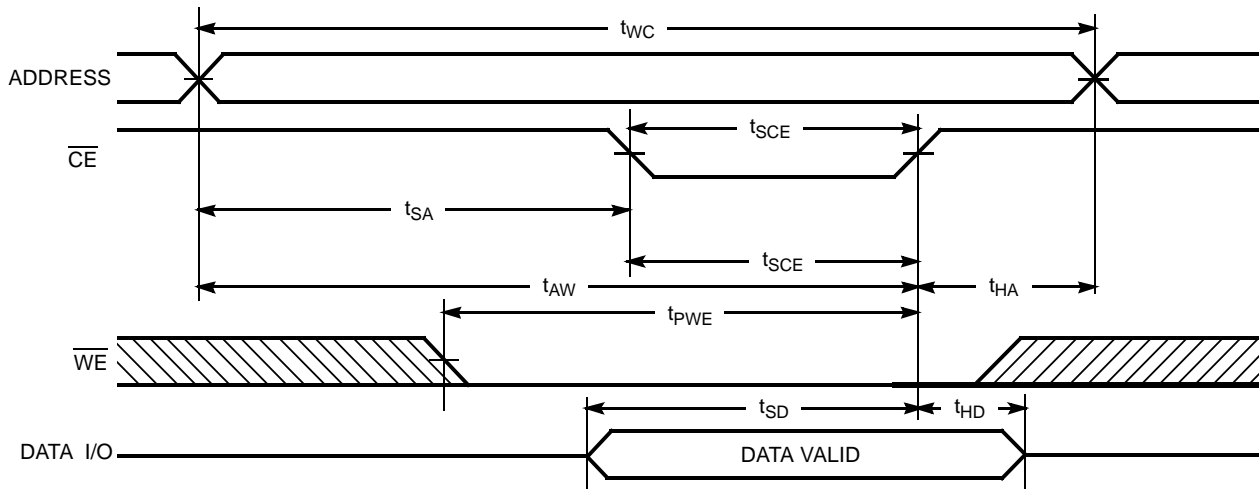
1046BV33-6

Read Cycle No. 2 (\overline{OE} Controlled)^[12, 13]


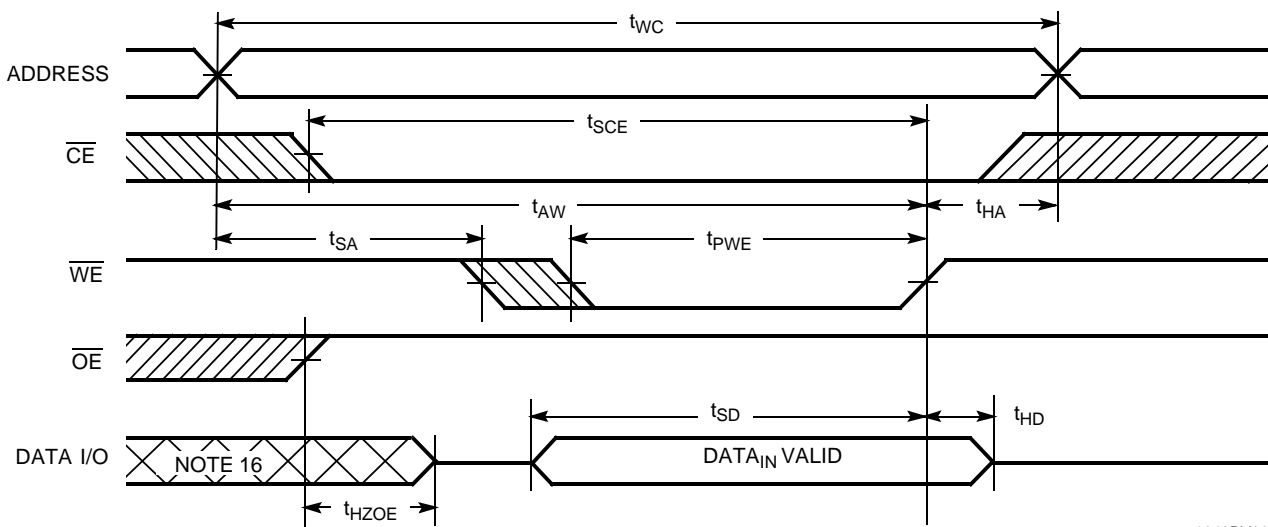
1046BV33-7

Notes:

9. $t_r \leq 3$ ns for the -10, -12, and -15 speeds.
10. No input may exceed $V_{CC} + 0.5V$.
11. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[14, 15]


1046BV33-8

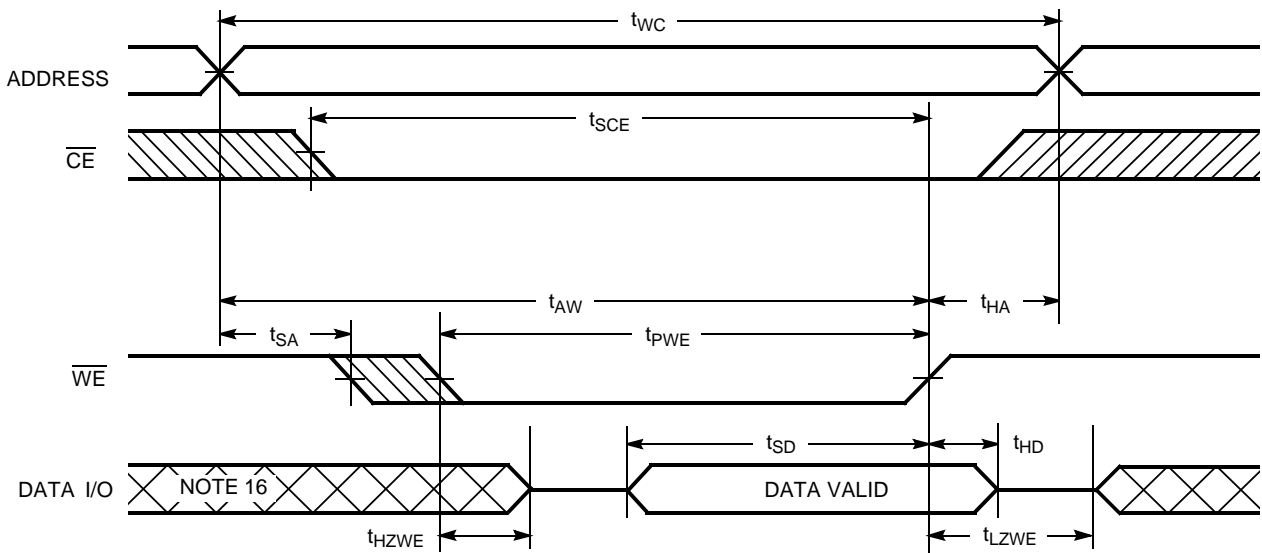
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[14, 15]


1046BV33-9

Notes:

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[15]


1046BV33-10

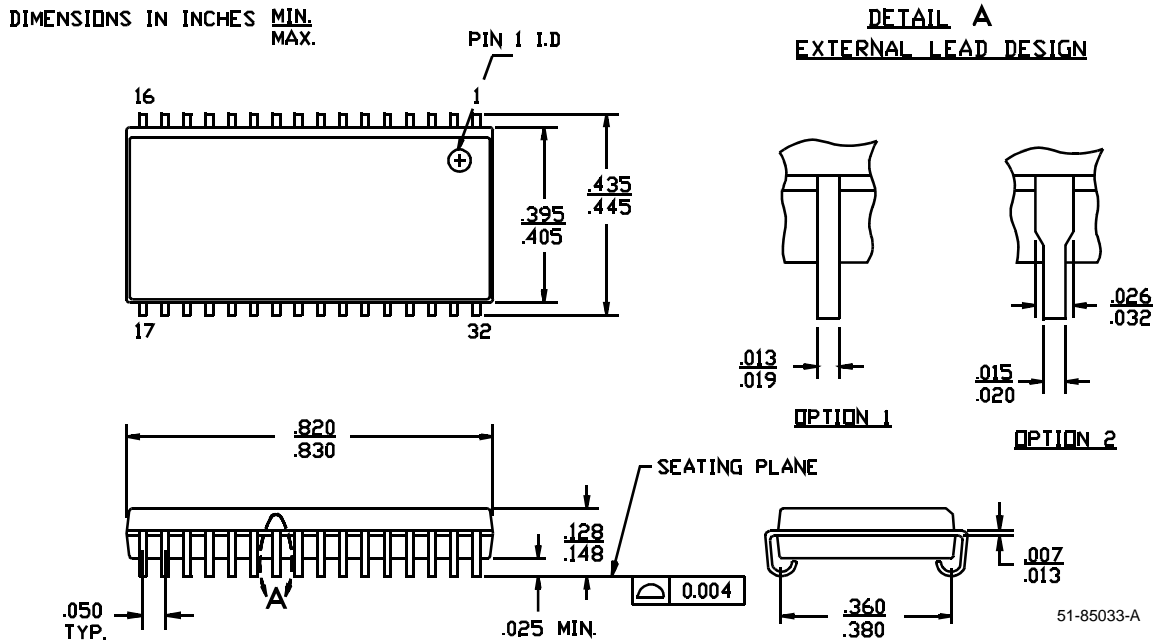
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ - I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I _{SB})
L	L	H	Data Out	Read	Active (I _{CC})
L	X	L	Data In	Write	Active (I _{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1046BV33-10VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
12	CY7C1046BV33-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046BV33-15VC	V33	32-Lead (400-Mil) Molded SOJ	
10	CY7C1046BV33L-10VC	V33	32-Lead (400-Mil) Molded SOJ	
12	CY7C1046BV33L-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046BV33L-15VC	V33	32-Lead (400-Mil) Molded SOJ	

Shaded areas contain pre-release information.

Package Diagram
32-Lead (400-Mil) Molded SOJ V33




Document Title: CY7C1046BV33 1M x 4 Static RAM Document Number: 38-05170				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110210	12/02/01	SZV	Change from Spec number: 38-00949 to 38-05170