CY7C68023/CY7C68024

EZ-USB NX2LP™ USB 2.0 NAND Flash Controller

Features

- High (480-Mbps) or Full (12-Mbps) speed USB support
- Both common NAND page sizes supported
  - 512 bytes — Up to 1 Gbit capacity
  - 2K bytes — Up to 8 Gbit capacity
- Eight chip enable pins
  - Up to 8 NAND flash single device chips
  - Up to 4 NAND flash dual device chips
- Industry Standard ECC NAND flash correction
  - 1 bit per 256 correction
  - 2 bit error detection
- Industry Standard (SmartMedia) Page Management for Wear Leveling Algorithm, Bad Block Handling, and Physical to Logical management
- Supports 8-bit NAND flash interfaces
- Supports 30 ns, 50 ns, and 100 ns NAND flash timing
- Complies with USB mass storage class specification rev 1.0
- CY7C68024 Complies with USB 2.0 Specification for Bus-Powered Devices (TID# 40460274)
- 43 mA typical active current
- Space saving and Pb-free 56-QFN Package (8 mm × 8 mm)
- Support for board-level manufacturing test through USB interface
- 3.3 V NAND flash operation
- NAND flash power management support

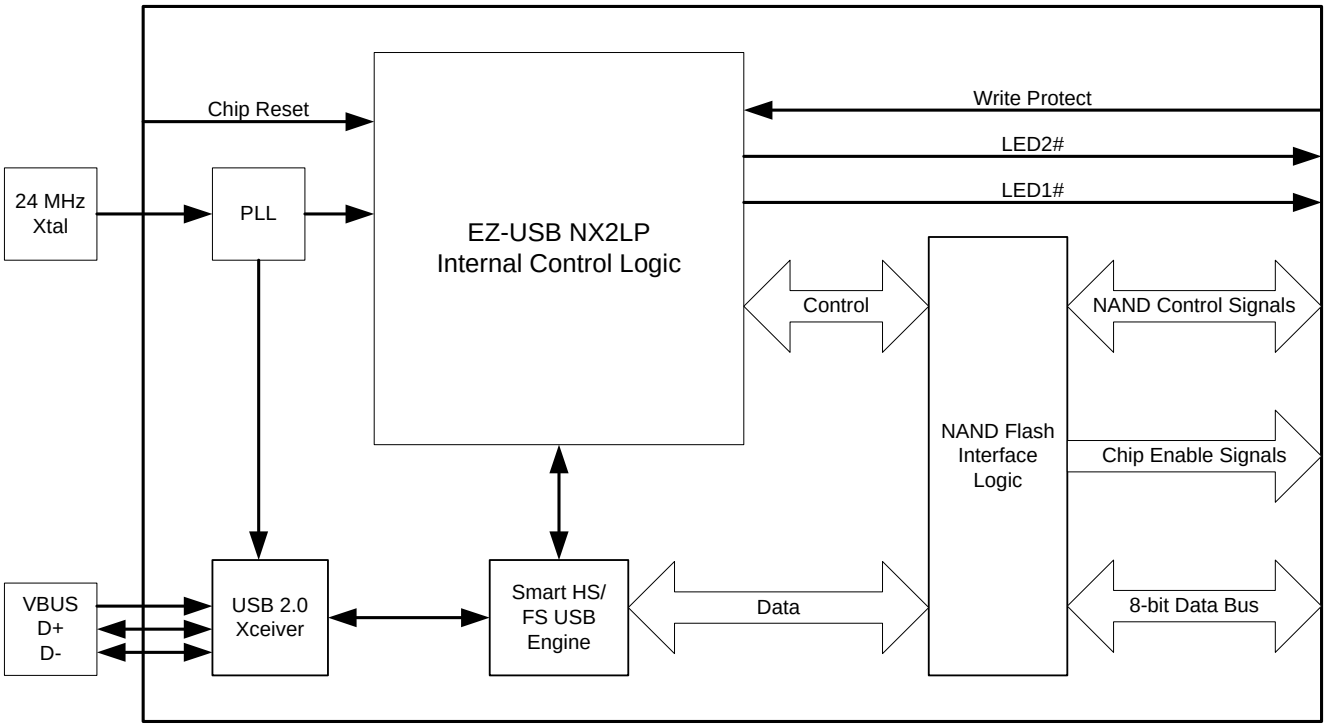
Introduction

The EZ-USB NX2LP™ (NX2LP) implements a USB 2.0 NAND Flash controller. This controller adheres to the *Mass Storage Class Bulk-Only Transport Specification*. The USB port of the NX2LP is connected to a host computer directly or through the downstream port of a USB hub. Host software issues commands and data to the NX2LP and receives status and data from the NX2LP using standard USB protocol.

The NX2LP supports industry leading 8-bit NAND Flash interfaces and both common NAND page sizes of 512 and 2k bytes. Eight chip enable pins allow the NX2LP to be connected to up to eight single or four dual device NAND Flash chips.

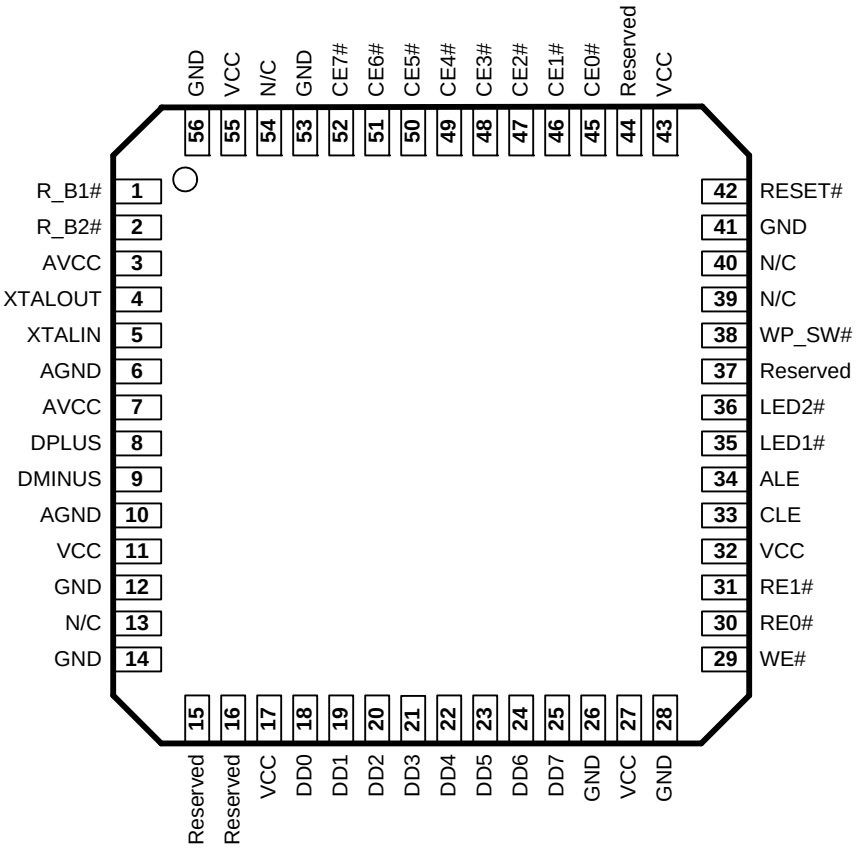
Certain NX2LP features are configurable, enabling the NX2LP to meet the needs of different design requirements.

NX2LP Block Diagram



Pin Assignments

Figure 1. 56-pin QFN



Pin Descriptions

Pin	Name	Type	Default State at Startup	Description
1	R_B1#[1]	I	Z	Ready/Busy 1 (2.2k to 4k pull up resistor is required)
2	R_B2#	I	Z	Ready/Busy 2 (2.2k to 4k pull up resistor is required)
3	AVCC	PWR	PWR	Analog 3.3 V supply
4	XTALOUT	Xtal	N/A	Crystal output
5	XTALIN	Xtal	N/A	Crystal input
6	AGND	GND	GND	Ground
7	AVCC	PWR	PWR	Analog 3.3 V supply
8	DPLUS	I/O	Z	USB D+
9	DMINUS	I/O	Z	USB D-
10	AGND	GND	GND	Ground
11	VCC	PWR	PWR	3.3 V supply
12	GND	GND	GND	Ground
13	N/C	N/A	N/A	No connect
14	GND	GND	GND	Ground
15	Reserved	N/A	N/A	Must be tied HIGH (no pull up resistor required)

Note
1. A # sign after the pin name indicates that it is an active LOW signal.

Pin Descriptions (continued)

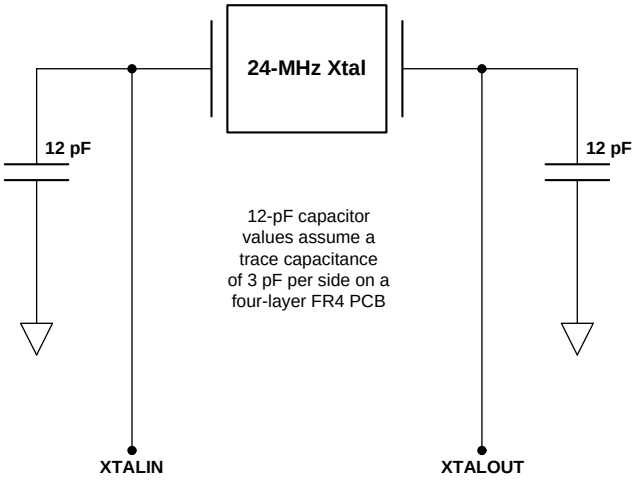
Pin	Name	Type	Default State at Startup	Description
16	Reserved	N/A	N/A	Must be tied HIGH (no pull up resistor required)
17	VCC	PWR	PWR	3.3 V supply
18	DDO	I/O	Z	Data 0
19	DD1	I/O	Z	Data 1
20	DD2	I/O	Z	Data 2
21	DD3	I/O	Z	Data 3
22	DD4	I/O	Z	Data 4
23	DD5	I/O	Z	Data 5
24	DD6	I/O	Z	Data 6
25	DD7	I/O	Z	Data 7
26	GND	GND	GND	Ground
27	VCC	PWR	PWR	3.3 V supply
28	GND	GND	GND	Ground
29	WE#	O	H	Write enable
30	RE0#	O	H	Read Enable 0
31	RE1#	O	H	Read Enable 1
32	VCC	PWR	PWR	3.3 V supply
33	CLE	O	Z	Command latch enable
34	ALE	O	Z	Address latch enable
35	LED1#	O	Z	Data activity LED sink
36	LED2#	O	Z	Chip active LED sink
37	Reserved	O	Z	No Connect
38	WP_SW#	I	Z	Write-protect switch input
39	N/C	N/A	N/A	No connect
40	N/C	N/A	N/A	No connect
41	GND	GND	GND	Ground
42	RESET#	I	Z	NX2LP chip reset
43	VCC	PWR	PWR	3.3 V supply
44	Reserved	N/A	N/A	Must be tied HIGH
45	CE0#	O	Z	Chip enable 0
46	CE1#	O	Z	Chip enable 1
47	CE2#	O	Z	Chip enable 2
48	CE3#	O	Z	Chip enable 3
49	CE4#	O	Z	Chip enable 4
50	CE5#	O	Z	Chip enable 5
51	CE6#	O	Z	Chip enable 6
52	CE7#	O	Z	Chip enable 7
53	GND	GND	GND	Ground
54	N/C	N/A	N/A	No connect
55	VCC	PWR	PWR	3.3 V supply
56	GND	GND	GND	Ground

Additional Pin Descriptions

DPLUS, DMINUS

DPLUS and DMINUS are the USB signaling pins, and they should be tied to the D+ and D– pins of the USB connector. Because they operate at high frequencies, the USB signals require special consideration when designing the layout of the PCB. General guidelines are given at the end of this document.

Figure 2. XTALIN, XTALOUT Diagram



The NX2LP requires a 24 MHz (±100 ppm) signal to derive internal timing. Typically, a 24 MHz (20 pF, 500 µW, parallel-resonant fundamental mode) crystal is used, but a 24 MHz square wave from another source can also be used. If a crystal is used, connect its pins to XTALIN and XTALOUT, and also through 12 pF capacitors to GND. If an alternate clock source is used, apply it to XTALIN and leave XTALOUT open.

Data[7-0]

The Data[7-0] I/O pins provide an 8-bit interface to a NAND Flash device. These pins are used to transfer address, command, and read/write data between the NX2LP and NAND Flash.

R_B[2-1]#

The Ready/Busy input pins are used to determine the state of the currently selected NAND Flash device. These pins must be pulled HIGH through a 2k-4k resistor. These pins are pulled LOW by the NAND Flash when it is busy.

WE#

The Write Enable output pin is used by the NAND Flash to latch commands, address, and data during the rising edge of the pulse.

RE[1-0]#

The Read Enable output pins are used to control the data flow from the NAND Flash devices. The device presents valid data and increments its internal column address counter by one step on each falling edge of the Read Enable pulse. A 10k pull up is an option For RE1-0#.

CLE

The Command Latch Enable output pin is used to indicate that the data on the I/O bus is a command. The data is latched into the NAND Flash control register on the rising edge of WE# when CLE is HIGH.

ALE

The Address Latch Enable output pin is used to indicate that the data on the I/O bus is an address. The data is latched into the NAND Flash address register on the rising edge of WE# when ALE is HIGH.

LED1#

The Data Activity LED output pin is used to indicate data transfer activity. LED1# is asserted LOW at the beginning of a data transfer, and set to a high Z state when the transfer is complete. If this functionality is not utilized, leave LED1# floating.

LED2#

The Chip Active LED output pin is used to indicate proper device operation. LED2# is asserted LOW when the NX2LP is powered and initialized. It is placed in a high Z state under all other conditions. If this functionality is not used, leave LED2# floating.

WP_SW#

The Write-protect Switch input pin is used to select whether or not NAND Flash write-protection is enabled by the NX2LP. When the pin is asserted LOW, the NAND Flash is write protected and any attempts to write to the configuration data memory are blocked.

CE[7-0]#

The Chip Enable output pins are used to select the NAND Flash that the NX2LP interfaces. Unused Chip Enable pins should be left floating.

RESET#

Asserting RESET# for 10 ms resets the NX2LP. A reset and/or watchdog chip is recommended to ensure that startup and brownout conditions are properly handled.

Applications

The NX2LP is a high speed USB 2.0 peripheral device that connects NAND Flash devices to a USB host using the USB Mass Storage Class protocol.

Additional Resources

- CY3685 EZ-USB NX2LP Development Kit
- CY4618 EZ-USB NX2LP Reference Design Kit
- USB Specification version 2.0
- USB *Mass Storage Class Bulk Only Transport Specification*, http://www.usb.org/developers/devclass_docs/usbmassbulk_10.pdf .

Functional Overview

USB Signaling Speed

The NX2LP operates at two of the three rates defined in the USB Specification Revision 2.0 dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbits/sec
- High speed, with a signaling bit rate of 480 Mbits/sec.

The NX2LP does not support the low speed signaling rate of 1.5 Mbits/sec.

NAND Flash Interface

During normal operation the NX2LP supports an 8-bit I/O interface, eight chip enable pins, and other control signals compatible with industry standard NAND Flash devices.

Enumeration

During the startup sequence, internal logic checks for the presence of NAND Flash with valid configuration data in the configuration data memory area. If valid configuration data is found, the NX2LP uses the values stored in NAND Flash to configure the USB descriptors for normal operation as a USB mass storage device. If no NAND Flash is detected, or if no valid configuration data is found in the configuration data memory area, the NX2LP uses the default values from internal ROM space for manufacturing mode operation. The two modes of operation are described in the following sections.

Normal Operation Mode

In Normal Operation Mode, the NX2LP behaves as a USB 2.0 Mass Storage Class NAND Flash controller. This includes all typical USB device states (powered, configured, and so on). The USB descriptors are returned according to the data stored in the configuration data memory area. Normal read and write access to the NAND Flash is available in this mode.

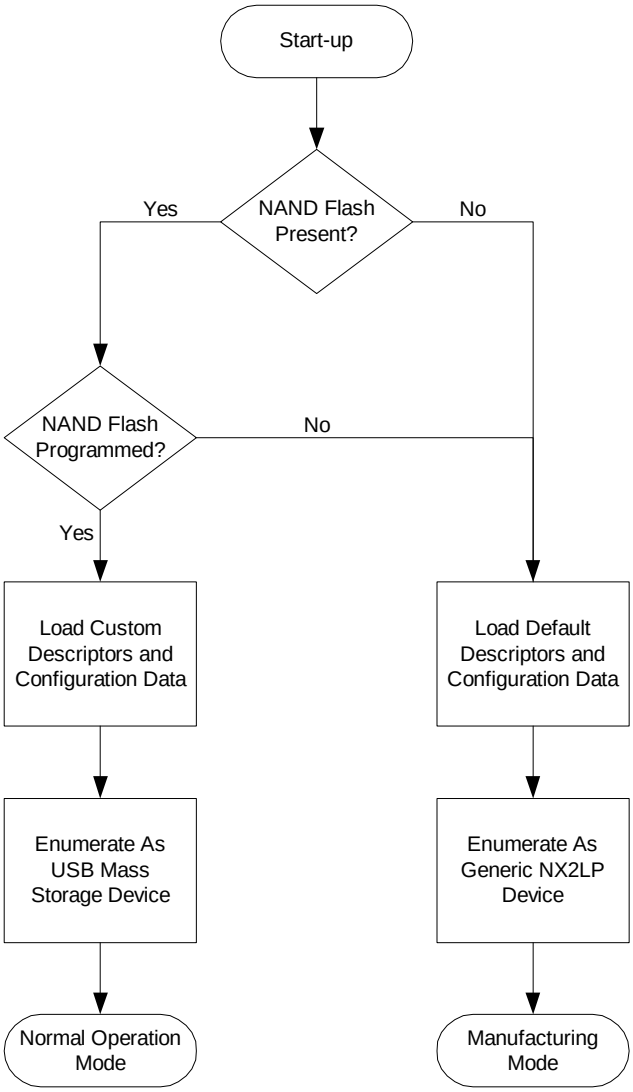
Manufacturing Mode

In Manufacturing mode, the NX2LP enumerates using the default descriptors and configuration data that are stored in internal ROM. This mode enables first-time programming of the configuration data memory area, and board-level manufacturing tests.

A unique USB serial number is required for each device in order to comply with the USB Mass Storage specification. Cypress also requires designers to use their own Vendor ID for final products. The Vendor ID is obtained through registration with the USB Implementor's Forum (USB-IF), and the Product ID is determined by the designer.

Cypress provides all the software tools and drivers necessary for properly programming and testing the NX2LP. Refer to the documentation in the development or reference design kit for more information on these topics.

Figure 3. NX2LP Enumeration Process



Configuration Data

Certain features in the NX2LP can be configured by the designer to disable unneeded features, and to comply with the USB 2.0 specification's descriptor requirements for mass storage devices. Table 1 lists the variable configuration data and the default values that are stored in internal ROM space. The default ROM values are returned by an unprogrammed NX2LP device.

Table 1. Variable Configuration Data And Default ROM Values

Configuration Data	Description	Default ROM Value
Vendor ID	USB Vendor ID (Assigned by USB-IF)	0x04B4 (Cypress)
Product ID	USB Product ID (Assigned by designer)	0x6813
Serial Number	USB serial number	N/A
Manufacturer String	Manufacturer string in USB descriptors	N/A
Product String	Product string in USB descriptors	N/A
Enable Write Protection	Enables write protection capability	Enabled
SCSI Device Name	String shown in the device manager properties	N/A

Design Notes For The Quad Flat No Lead (QFN) Package

The NX2LP comes in a 56-pin QFN package, which utilizes a metal pad on the bottom to aid in heat dissipation. The low-power operation of the NX2LP makes the thermal pad on the bottom of the QFN package unnecessary. Because of this, PCB layout may utilize the space under the NX2LP for routing signals as needed, provided that any traces or vias under the thermal pad are covered by solder mask or other material to prevent shorting. Standard PCB layout recommendations for USB devices still apply.

For further information on this package design, please refer to the application note from AMKOR titled "Surface Mount Assembly of AMKOR's MicroLeadFrame (MLF) Technology." This application note provides detailed information on board mounting guidelines, soldering flow, rework process, etc.

PCB Layout Recommendations

The following recommendations should be followed to ensure reliable High-speed USB performance operation.

- A four-layer impedance controlled board is recommended to ensure best signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- Maintain trace widths and trace spacing to control impedance.
- Minimize stubs on DPLUS and DMINUS to avoid reflected signals.
- Place any connections between the USB connector shell and signal ground near the USB connector.
- Use bypass/flyback caps on VBUS, placed near connector.
- Keep DPLUS and DMINUS trace lengths to within 2 mm of each other in length, with preferred length of 20–30 mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to be split under these traces.
- Place no vias on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces (use >10 mm. spacing for best signal quality).

Source for recommendations:

- EZ-USB FX2 PCB Design Recommendations, www.cypress.com/?docID=4696.
- High-speed USB Platform Design Guidelines, http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf.

Absolute Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Supplied..... 0 °C to +70 °C

Supply Voltage to Ground Potential.....–0.5 V to +4.0 V

DC Input Voltage to Any Input Pin ..... 5.25 V

DC Voltage Applied to Outputs in High Z State ..... –0.5 V to V_{CC} + 0.5 V

Power Dissipation..... 300 mW

Static Discharge Voltage..... 2000 V

Max Output Current per IO port..... 10 mA

Operating Conditions[2]

T_A (Ambient Temperature Under Bias) ..... 0 °C to +70 °C

Supply Voltage.....+3.00 V to +3.60 V

Ground Voltage..... 0 V

DC Characteristics

Parameter	Description		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage			3.0	3.3	3.6	V
V_{CC} Ramp	Supply Ramp-up 0 V to 3.3 V			200	–	–	µs
V_{IH}	Input High voltage			2	–	5.25	V
V_{IL}	Input Low voltage			–0.5	–	0.8	V
I_I	Input leakage current		$0 < V_{IN} < V_{CC}$	–	–	±10	µA
V_{IH_X}	Crystal Input HIGH voltage			2	–	5.25	V
V_{IL_X}	Crystal Input LOW voltage			–0.5	–	0.8	V
V_{OH}	Output voltage High		I_{OUT} = 4 mA	2.4	–	–	V
V_{OL}	Output voltage Low		I_{OUT} = –4 mA	–	–	0.4	V
I_{OH}	Output current High			–	–	4	mA
I_{OL}	Output current Low			–	–	4	mA
C_{IN}	Input pin capacitance		All but D+/D–	–	–	10	pF
			Only D+/D–	–	–	15	pF
I_{CC}	Supply current		USB High Speed	–	50	–	mA
			USB Full Speed	–	35	–	mA
I_{SUSP}	Suspend current	CY7C68023	Connected	–	0.5	1.2[3]	mA
			Disconnected	–	0.3	1.0[3]	mA
		CY7C68024	Connected	–	300	380[3]	µA
			Disconnected	–	100	150[3]	µA
$I_{UNCONFIG}$	Unconfigured current		Before current requested in USB descriptors is granted by the host	–	43	–	mA
T_{RESET}	Reset Time After Valid Power		V_{CC} > 3.0 V	5.0	–	–	mS
	Pin reset after valid startup			200	–	–	µS

AC Electrical Characteristics

USB Transceiver

The NX2LP's USB interface complies with the USB 2.0 specification for bus-powered devices.

NAND Flash Timing

The NX2LP supports 30-ns, 50-ns, and 100-ns NAND Flash devices.

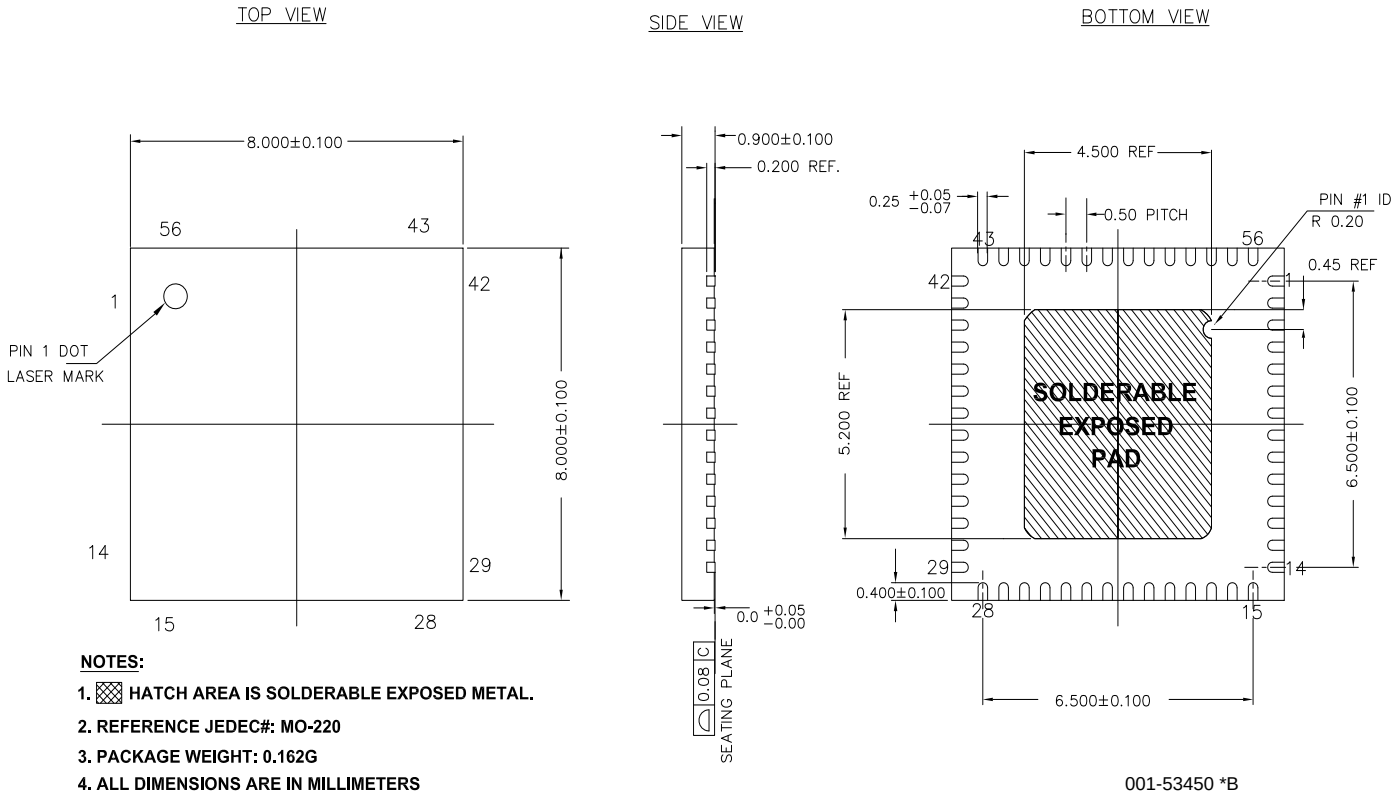
Notes
2. If an alternate clock source is input on XTALIN, it must be supplied with standard 3.3 V signaling characteristics and XTALOUT must be left floating.
3. Measured at Max V_{CC}, 25 °C.

Ordering Information

Part Number	Package Type
CY7C68023-56LTXC	56-pin QFN - Sawn type

Package Diagram

Figure 4. 56-pin QFN (8 × 8 × 0.9 mm) - Sawn



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162G
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-53450 *B

Document History Page

Description Title: CY7C68023/CY7C68024 EZ-USB NX2LP™ USB 2.0 NAND Flash Controller Document Number: 38-08055				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	286009	SEE ECN	GIR	New Data Sheet (Preliminary Information).
*A	334796	SEE ECN	GIR	Adjusted default VID/PID; released as final.
*B	397024	SEE ECN	GIR	Changed Vcc to ±10% in DC Characteristics table. Changed the supply voltage tolerance to ±10% in the Operating Conditions section. Added new logo.
*C	2717536	06/11/2009	DPT	Added 56 QFN (8 X 8 mm) package diagram and added CY7C68023-56LTXC part information in the Ordering Information table
*D	2896245	03/19/2010	CPPK	Updated ordering information and package diagrams.
*E	3208866	03/29/2011	CPPK	Updated Ordering Information. Updated Package Diagram. Updated in new template.
*F	3330673	07/28/2011	AASI	Removed 56-pin QFN (punch type) package spec.
*G	3645844	06/14/2012	GAYA	Marked WP_NF# pin as reserved, and updated the explanation for WP_SW# pin.

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