OC-48/STM-16 Framer - POSIC2G™

Features

- **OC-48/STS-48/STM-16, OC-12/STS-12/STM-4, OC-3/STS3/STM-1 rates, concatenated and nonconcatenated**
  - **Complies with ITU-Standards G.707/Y.1322 and G.783**
  - **Complies with Bellcore GR253 rev.1, 1997**
  - **Channelized operation: supports 16xOC-3/STM-1 and 4xOC-12/STM-4 within OC48 stream**
  - **Supports TUG3 mapping in SDH mode**
- **Full duplex mapping of ATM cells over SONET/SDH**
  - **Complies with ITU-Standards I 432.2**
- **Full duplex mapping of packet-over-SONET/SDH: IETF RFC 1619/1662/2615 (HDLC/PPP)**
- **Generic Protocol Encapsulator/Decapsulator delineates packets/frames with length-CRC frame construct**
  - **Generic Framing Procedure (GFP) per ANSI T1X1.5**
- **User-programmable encapsulation**
- **User-programmable clear channel transport**
- **User-programmable SONET/SDH bypass**
- **Programmable frame tagging engine for packet pre-classification enables features such as**
  - **MPLS label lookup and tagging**
  - **PPP: LCP and NCP tagging**
  - **PPP control packets optionally sent to host CPU interface**
  - **MAC/layer 3 address lookup and tagging**

- **Programmable A1A2 processing bypass in Rx direction with frame sync input**
- **Complete section overhead (SOH), line overhead (LOH), and path overhead (POH) processing**
- **APS extraction, CPU interrupt generation, and programmable insertion of APS byte**
- **Line side APS port interface**
- **Provision for protection switching on SONET/ SDH port**
- **Programmable PRBS generator and receiver**
- **Serial port to access line/section data communication channel (DCC) and voice communication channel (VCC)**
- **Full duplex UTOPIA/OIF-SPI (POS-PHY) level 3 interface**
- **16-bit/32-bit host CPU interface bus (Motorola/Intel class)**
- **JTAG and boundary scan**
- **Glueless interface with Cypress CYS25G0101DX OC-48 PHY**
- **0.18-μm CMOS, 504-pin BGA package**
- **+1.8V for core, +3.3V for LVTTL I/O, +1.5V/+3.3V for HSTL/LVPECL I/O supply and +0.75V/2.0V reference**

Applications

- **Multi-service nodes**
- **ATM switches and routers**
- **Packet routers**
- **Multi-service routers**
- **SONET/SDH/add-drop mux for packet/data applications**
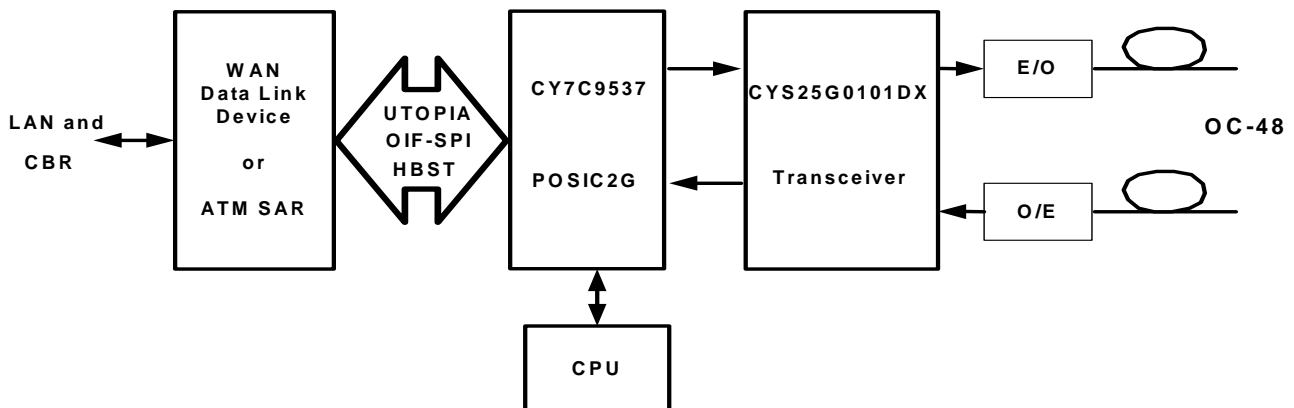- **SONET/SDH/ATM/POS test equipment**

Figure 1. POSIC2G™ System Application Diagram