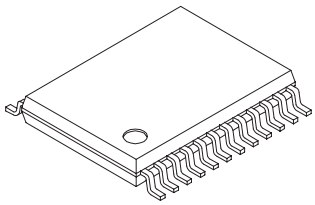
SONY

CXA3668N

Reception Analog Signal Processor IC for Infrared Space Digital Audio Communication

24 pin SSOP (Plastic)



Description

The CXA3668N is an IC that performs reception side analog signal processing for optical communication in combination with an infrared photodiode within a Digital Infrared Audio Transmission (DIAT) system.

This IC incorporates a low noise trans-conductance amplifier (I/V amplifier) that converts the optical current from the photodiode into a voltage and amplifies it, an AGC amplifier, a low-pass filter, band-pass filters, and an output amplifier.

The band-pass filters are used to separate the desired signal and the interfering signal. This chip has the two types of Full (3 to 6MHz) and Half (3 to 4.5MHz) band-pass filters, and these can be switched according to the application.

- Full: Full-band width (3 to 6MHz)
- Half: Half-band width (3 to 4.5MHz)

Features

- Wide dynamic range
- On-chip I/V amplifier
- On-chip output filter
- Filter band switching pin
- Surface mounting package (24-pin SSOP)

Applications

- Infrared headphones
- Infrared speakers

Structure

Bi-CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

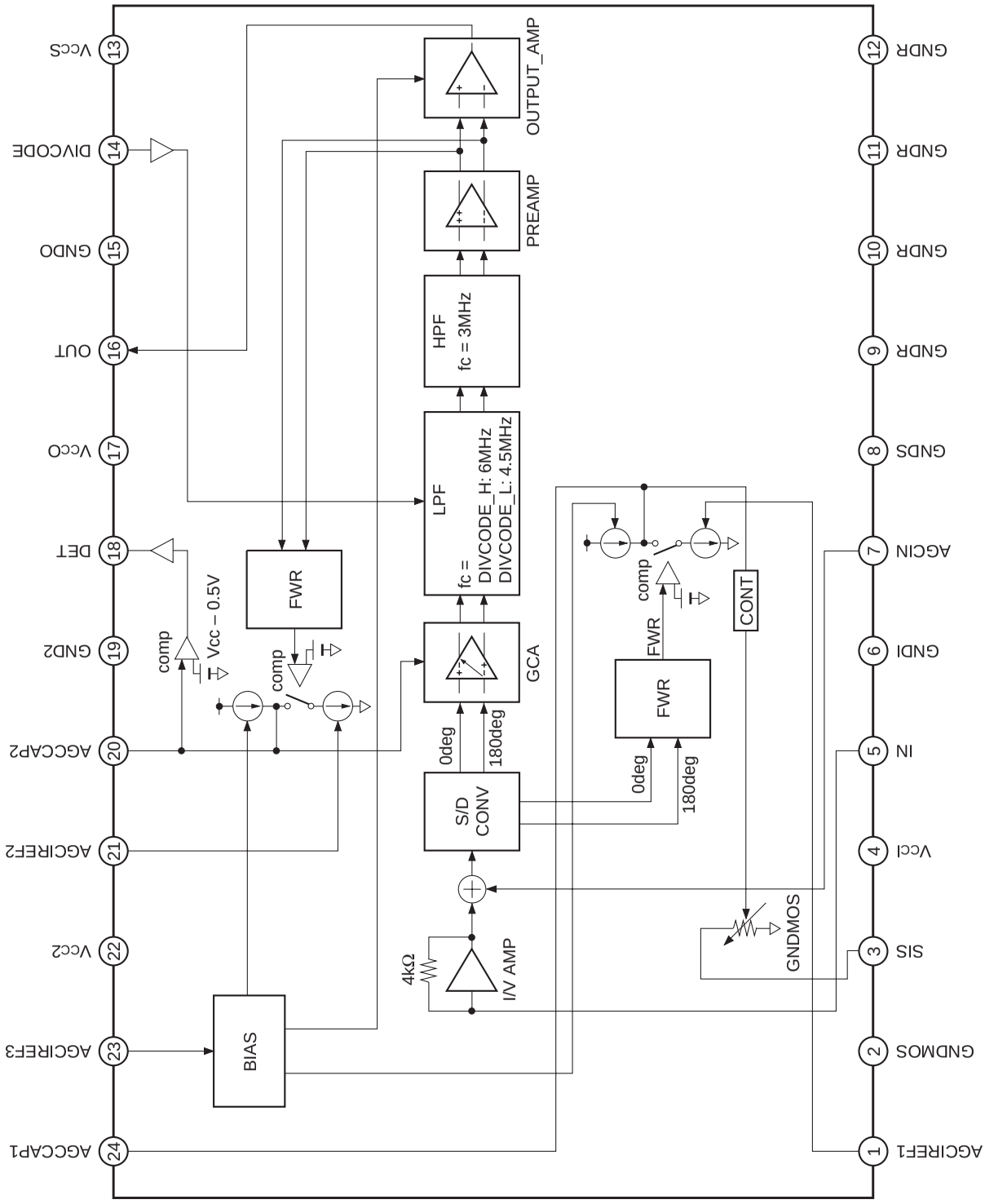
• Supply voltage	$V_{CC}I$, $V_{CC}2$, $V_{CC}S$, $V_{CC}O$	3.3	V
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	400	mW

Recommended Operating Conditions

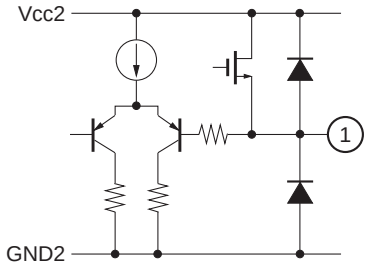
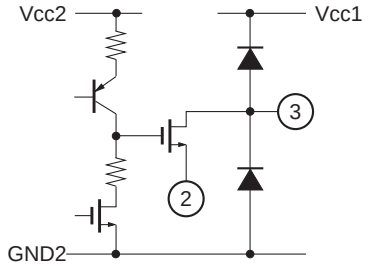
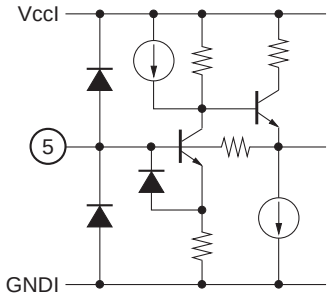
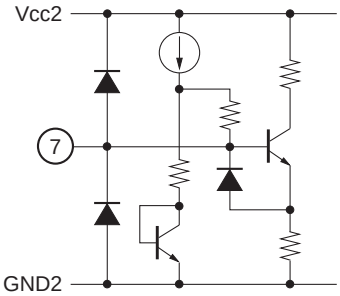
• Supply voltage	$V_{CC}I$, $V_{CC}2$, $V_{CC}S$, $V_{CC}O$	2.3 to 2.7	V
• Operating temperature	Topr	–40 to +85	°C

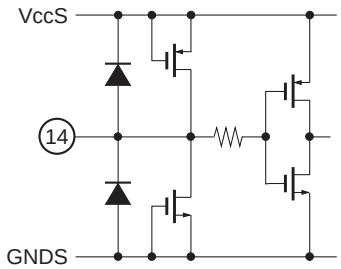
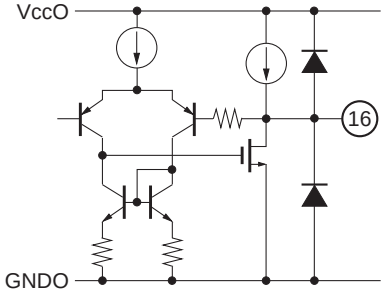
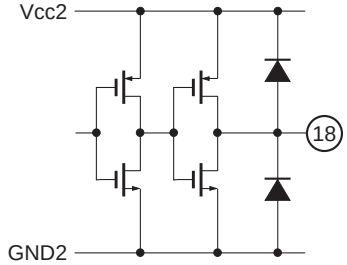
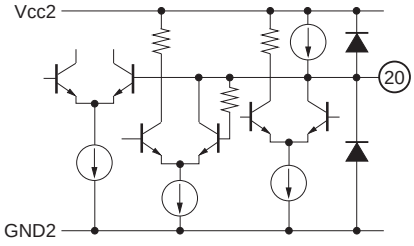
E04244-PS

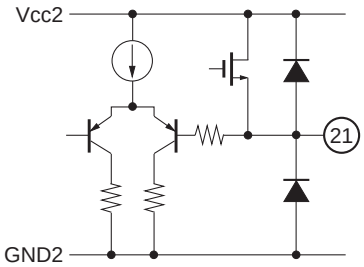
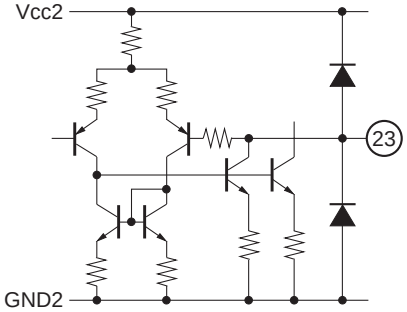
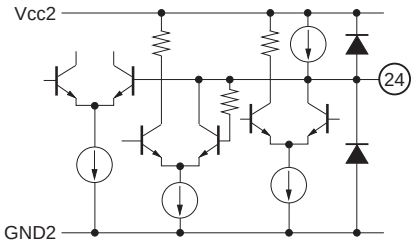
Pin Configuration and Block Diagram



Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	AGCIREF1		0.2V		Reference current generation for determining the input AGC attack time. Connect to GND2 through a 390Ω or more resistor. Reducing the resistance value shortens the attack time.
2	GNDMOS		GND		Input block shunt GND.
3	SIS	O	0V		Shunt input. This shunts the optical current of the photodiode and applies the AGC.
4	VccI		+2.5V (Typ.)		Input block power supply.
5	IN	I	0.8V		Photodiode input. This is the current-voltage conversion input for amplifying the photodiode current. Input impedance: approximately 60Ω
6	GNDI		GND		Input block GND.
7	AGCIN	I	1.1V		AGC input.
8	GNDS		GND		Signal processing block GND.
9, 10, 11, 12	GNDR		GND		GND.
13	VccS		+2.5V (Typ.)		Signal processing block power supply.

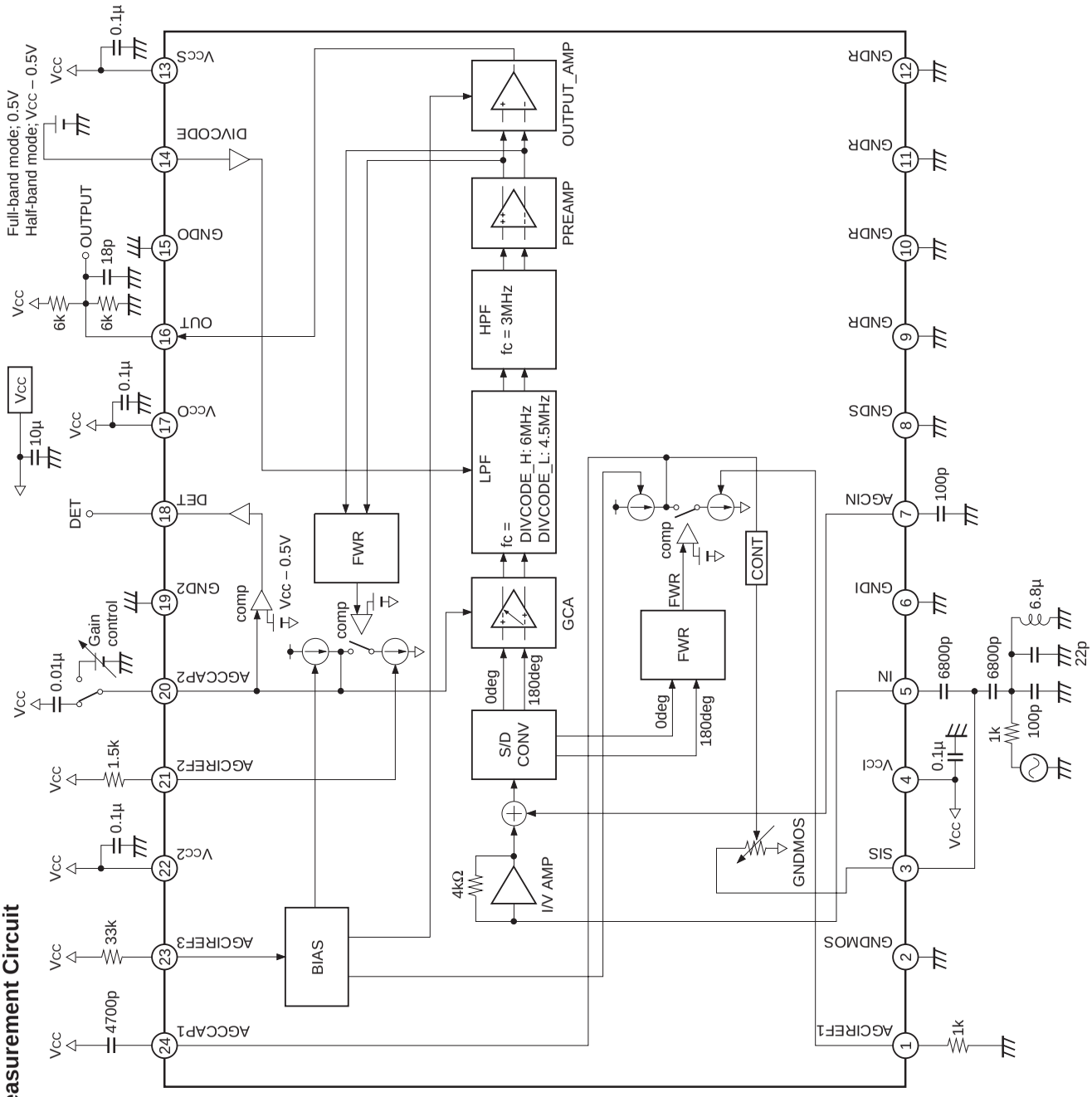
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
14	DIVCODE	I			Filter characteristics switching. • Low: Full-band BPF (3 to 6MHz) • High: Half-band BPF (3 to 4.5MHz) Logic level: • Low: 0 to 0.5V • High: 1.5V to Vcc
15	GNDO		GND		Output amplifier block GND.
16	OUT	O	1.25V		Signal output. The load capacitance should be as small as possible to ensure stable output. • Load resistance: 3kΩ or more • Load capacitance: 18pF or less
17	VccO		+2.5V (Typ.)		Output amplifier block power supply.
18	DET	O			Input level detection. This detects whether the input level is the prescribed value, and outputs the judgment results. This pin outputs low when the input level is 0.05µAp-p or less, and high when the input level is 0.3µAp-p or more.
19	GND2		GND		AGC GND.
20	AGCCAP2				AGC2 response setting. Connect to Vcc2 through a capacitor.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
21	AGCIREF2		0.2V		Reference current generation for determining the AGC2 attack time. Connect to GND2 through a 390Ω or more resistor. Reducing the resistance value shortens the attack time.
22	Vcc2		+2.5V (Typ.)		AGC power supply.
23	AGCIREF3		1.25V		Reference current generation for determining the input AGC and the AGC2 recovery time. Connect to Vcc2 through a 33kΩ resistor.
24	AGCCAP1				Input AGC response setting. Connect to Vcc2 through a capacitor.

Electrical Characteristics (Ta = 25°C, $V_{CC}I$, $V_{CC}2$, $V_{CC}S$, $V_{CC}O$ = 2.5V)

Item	Conditions	Min.	Typ.	Max.	Unit
Supply voltage V_{CC}	($V_{CC}I$, $V_{CC}2$, $V_{CC}S$, $V_{CC}O$ = V_{CC})	2.3	2.5	2.7	V
Current consumption (1) $I_{CC}1$ (H)	100µAp-p, I_{CC} total	10	18	25	mA
Current consumption difference (2) $dI_{CC}1$ (L)	300µAp-p, $dI_{CC}1$ (L) = $I_{CC}1$ (L) – $I_{CC}1$	–100	30	100	µA
AGC variable range	Input signal (1mAp-p/0.25µAp-p)	72			dB
Output amplitude (1)	0.1µAp-p input, load 3kΩ, 18pF	0.2	—	—	Vp-p
Output amplitude (2)	100µAp-p input, load 3kΩ, 18pF	1.5	—	2.0	Vp-p
[BPF characteristics]					
Full BPF-1	< 2.0/4.5MHz	—	—	–30	dB
Full BPF-2	3.15/4.5MHz	–3	0	3	dB
Full BPF-3	5.85/4.5MHz	–3	0	3	dB
Full BPF-4	> 8.0/4.5MHz	—	—	–36.1	dB
Half Low BPF-1	< 2.0/3.75MHz	—	—	–30	dB
Half Low BPF-2	3.15/3.75MHz	–3	0	3	dB
Half Low BPF-3	4.35/3.75MHz	–3	0	3	dB
Half Low BPF-4	> 5.8/3.75MHz	—	—	–36.1	dB
S/N (1)	100µAp-p input	40	—	—	dB
S/N (2)	0.1µAp-p input	20	—	—	dB
Output secondary distortion	100µAp-p input	30	—	—	dB

Electrical Characteristics Measurement Circuit

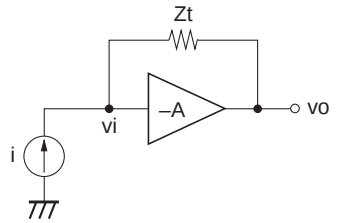


Description of Operation

(1) Trans-impedance amplifier circuit (I/V amplifier)

The input block is comprised of the trans-impedance amplifier circuit which converts the optical current Ip from the photodiode into a current, and the AGCATT circuit.

Fig. 1 shows the I/V amplifier equivalent circuit.



Zt: Trans-impedance
A: Amplifier gain

Fig. 1

The following equations are satisfied in the circuit shown in Fig. 1.

$vo = -A \times vi$

$vi - vo = i \times Zt$

The input impedance Zi of the I/V amplifier is obtained from these equations as follows.

$Zi = vi/i = Zt/ (1 + A)$

The trans-impedance Zt of this IC is 4kΩ (typ.) and the amplifier gain A is 65 times (typ.), so Zi is 60.6Ω (typ.).

(2) AGC ATT

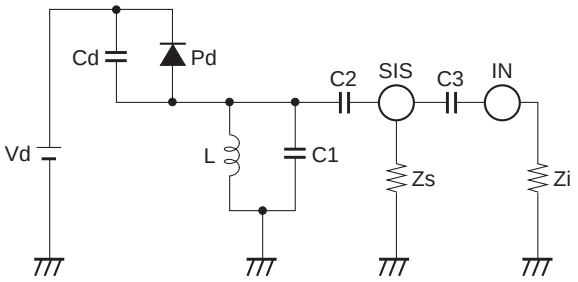
The IC operates at an input optical current of up to 1mAp-p (max.), so the trans-impedance input current It is controlled so that the trans-impedance amplifier circuit does not produce a saturated state.
Labeling the SIS impedance as Zs, $It = Ip \times Zs/(Zs + Zin)$.
It is controlled so that the trans-impedance amplifier circuit output does not go to 250mVp-p or more, and when Ip is 63.5µAp-p or less, It = Ip ($Zs \gg Zin$).
When Ip is 63.5µAp-p or more and 1mAp-p or less, Zs decreases and Ip goes to 63.5µAp-p so that the trans-impedance output level is 250mVp-p.

• The AGC ATT attack time and recovery time response are as follows.

The attack time and the recovery time are determined by the capacitor Ca connected between AGCCAP1 (Pin 24) and $V_{CC}2$. Increasing the Ca value lengthens both the attack time and the recovery time, and reducing the Ca value shortens both the attack time and the recovery time.
The reference current (Iat = 0.2/Raa) used to determine the attack time is determined by the resistor Raa connected between AGCIREF1 (Pin 1) and GND. Reducing the resistance value increases the reference current and shortens the attack time. Increasing the resistance value lengthens the attack time.
The reference current (Iar = 0.625/Rar) used to determine the recovery time is determined by the resistor Rar connected between AGCIREF3 (Pin 23) and V_{CC}. Use a Rar of 33kΩ.

(3) IN frequency response

Fig. 2 shows the IN input circuit.



Vd: Photodiode bias voltage
Cd: Photodiode junction capacitor
Pd: Photodiode
L: External inductor
C1, C2, C3: External capacitors
Zs: SIS pin impedance
Zi: I/V amplifier input impedance

Fig. 2

(1) When the photodiode current Ip ≤63.5µAp-p

Zs goes to 100kΩ and can be ignored. The circuit in Fig. 2 can be expressed by the equivalent circuit in Fig. 3.

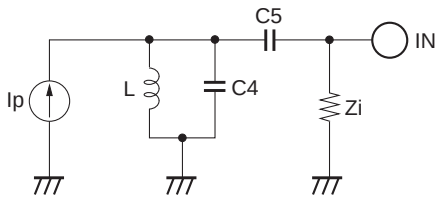


Fig. 3

However, C4 and C5 are as follows.

C4 = C1 + Cd

C5 = C2/2 (however, C2 = C3)

The IN voltage VI is obtained from the equivalent circuit in Fig. 3 as follows.

$$VI = \frac{\frac{S^2}{C_4}}{S^3 + \left(\frac{1}{C_4} + \frac{1}{C_5}\right)\frac{s^2}{Zi} + \frac{s}{C_4 L} + \frac{1}{C_4 C_5 L Zi}} \times Ip$$

VI/Ip (Ga) is as follows.

$$Ga = \frac{VI}{Ip} = \frac{-\frac{\omega^2}{C_4}}{\left[\frac{1}{C_4 C_5 L Zi} - \left(\frac{1}{C_4} + \frac{1}{C_5}\right)\frac{\omega^2}{Zi}\right] + j\left(\frac{\omega}{C_4 L} + \frac{1}{C_4 C_5 L Zi}\right)}$$

When set to Cd = 72pF, C1 = 47pF, L = 6.8µH, and C2 = C3 = 6800pF, the Ga frequency response is as shown in Fig. 4.

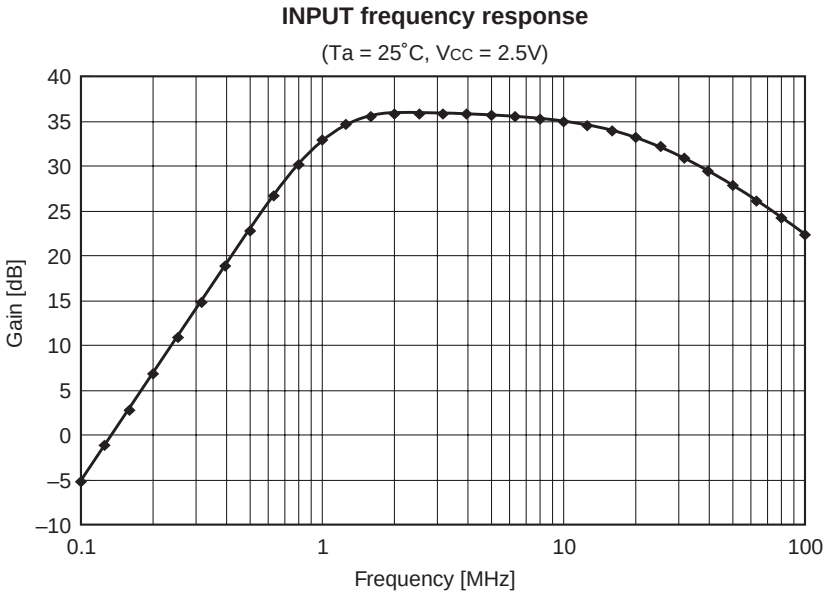


Fig. 4

Set L, C1, C2 and C3 so that the gain is flat from the 3MHz band to the 6MHz band.

(2) When the photodiode current Ip > 63.5µAp-p

Labeling the Ip peak-to-peak size as Ipp, Zs in Fig. 2 is as follows.

$$Rsis = \frac{233 \times 10^{-3}}{60.6 \times Ipp - 3.85 \times 10^{-3}}$$

In addition, the circuit in Fig. 2 can be expressed by the equivalent circuit in Fig. 5.

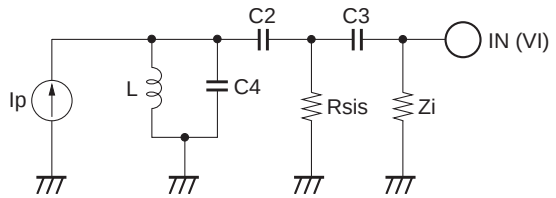


Fig. 5

However, C4 = Cp + C1.

When set to Cd = 72pF, C1 = 47pF, L = 6.8µH, and C2 = C3 = 6800pF, the VI/Ip frequency response at Ipp = 100µAp-p, 300µAp-p and 1mAp-p are as shown in Fig. 6.

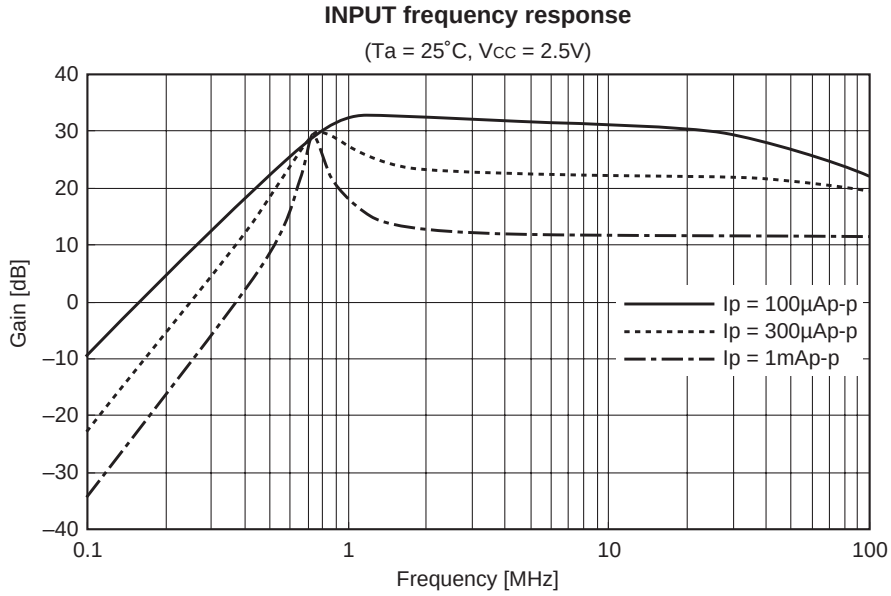


Fig. 6

(4) AGCIN

The signal input from AGCIN (Pin 7) and the I/V amplifier output signal are added and converted to a differential signal. This differential signal is input to the gain control amplifier (GCA), and the GCA output is input to the filter. When using AGCIN, input through a coupling capacitor C (100pF). When not using AGCIN, connect it to GND through C (100pF).

(5) Band-pass filter

Full-band mode and Half-band mode can be selected by the DIVCODE (Pin 14) pin voltage.
The cutoff frequencies (fc) for the Full-band and Half-band modes which correspond to the DIVCODE pin voltage are as follows.

DIVCODE	Mode
Low	Full-band (3MHz to 6MHz)
High	Half-band (3MHz to 4.5MHz)

High; 1.5V to V_{CC}, Low; 0 to 0.5V

(6) AGC2

The band-pass filter output is amplified to 4 times by the preamplifier, and the GCA gain is varied so that the preamplifier output is approximately 0.8Vp-p.
The preamplifier output is converted from a differential signal to a single signal by a subtracter with a gain of approximately 2.1 times, and is then output from OUT (Pin 16) at a level of approximately 1.7Vp-p.

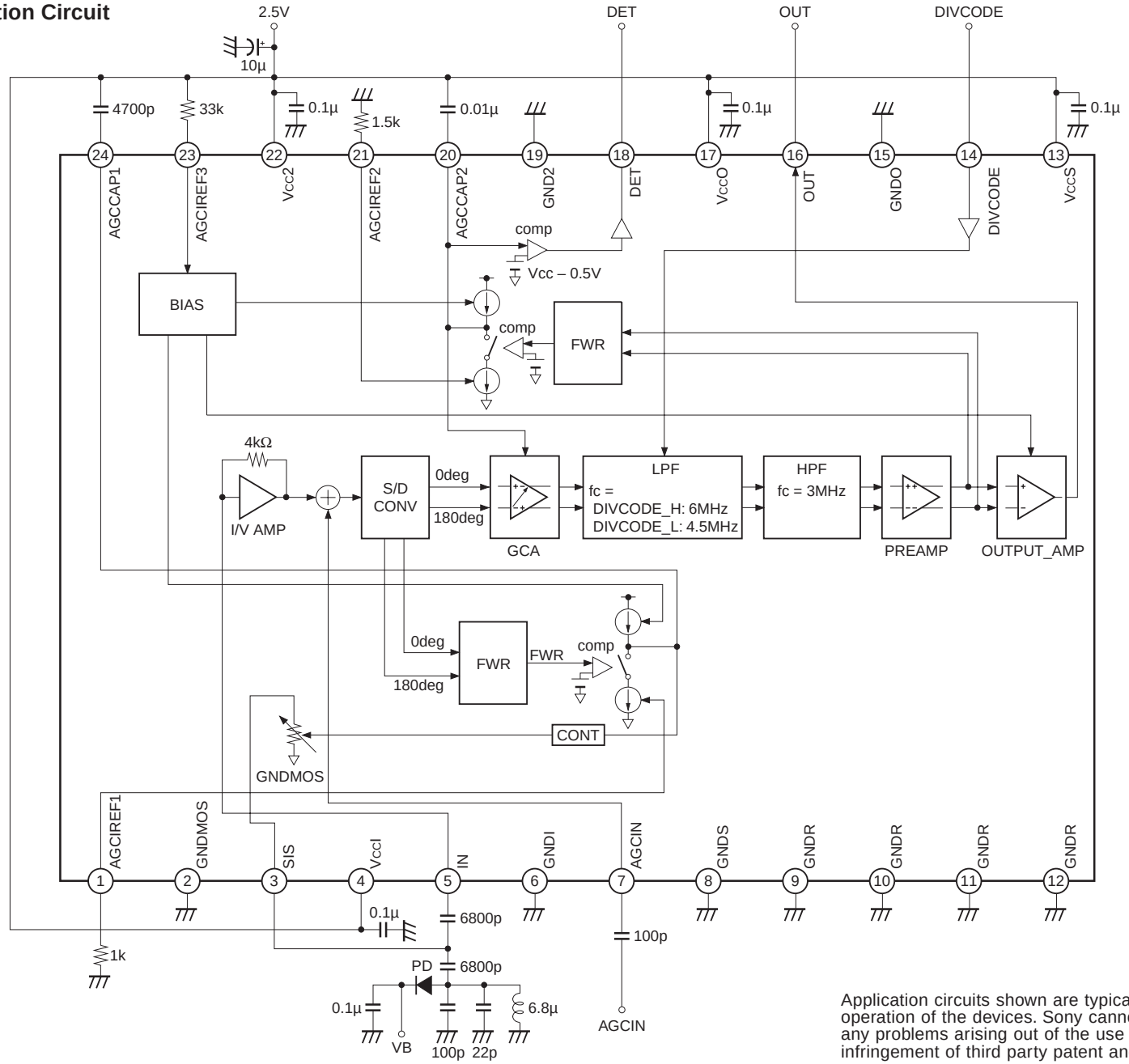
• The AGC2 attack time and recovery time response are as follows.

The attack time and the recovery time are determined by the capacitor Ca2 connected between AGCCAP2 (Pin 20) and $V_{CC}2$. Increasing the Ca2 value lengthens both the attack time and the recovery time, and reducing the Ca2 value shortens both the attack time and the recovery time.
The reference current (Iat2 = 0.2/Raa2) used to determine the attack time is determined by the resistor Raa2 connected between AGCIREF2 (Pin 21) and GND. Reducing the resistance value increases the reference current and shortens the attack time. Increasing the resistance value lengthens the attack time.
The reference current used to determine the recovery time is determined by the resistor Rar connected between AGCIREF3 (Pin 23) and V_{CC}.

(7) DET

When the GCA input level is so low that the AGC2 does not operate (typ.; Ip = less than 0.15µAp-p), DET (Pin 18) goes low. When the GCA input level is high enough for the AGC2 to operate (typ.; Ip = 0.15µAp-p or more), DET goes high.

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

Care should be taken for the following points when using the CXA3668N.

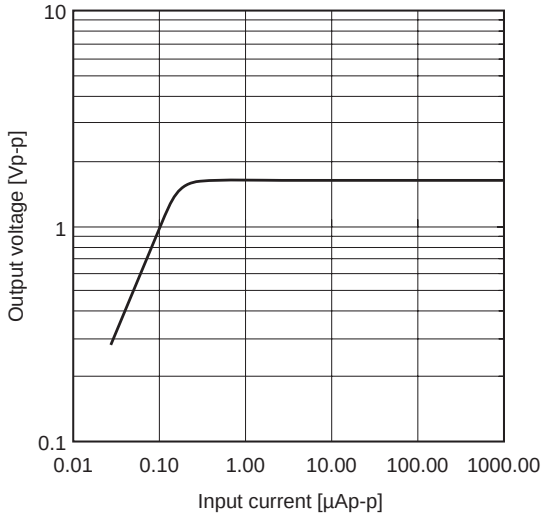
- This IC has a high I/O gain (particularly during no signal or weak signal input of 0.15µAp-p (typ.) or less at which the AGC does not operate), so care should be taken for the power supply and GND pattern when designing the printed circuit board.
  The power supplies and GND are divided by function block as follows.

  1) Input block
     Power supply: V_{CC}I
     GND: GNDI
  2) Input block shunt
     GND: GNDMOS
  3) AGC block
     Power supply: V_{CC}2
     GND: GND2
  4) Filter block
     Power supply: V_{CC}S
     GND: GNDS
  5) Output block
     Power supply: V_{CC}O
     GND: GNDO
  6) Other
     GND: GNDR

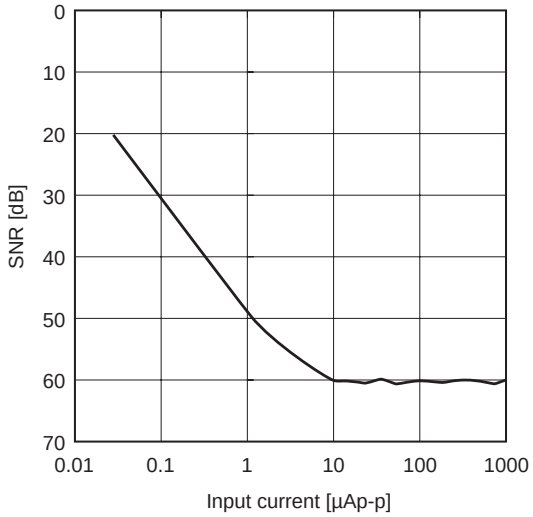
Using tantalum, ceramic or other chip capacitors with excellent frequency response to decouple the power supply and GND pins of each function block is recommended. These capacitors should be connected between the pins as close to the respective IC pins as possible. The pattern should be designed as short and wide as possible.
In addition, shielding each external circuit (particularly the input circuit connected to the IN pin) is recommended to prevent spatial crosstalk from the output circuit, etc.

Example of Representative Characteristics (Ta = 25°C, VccI, Vcc2, VccS, VccO = 2.5V)

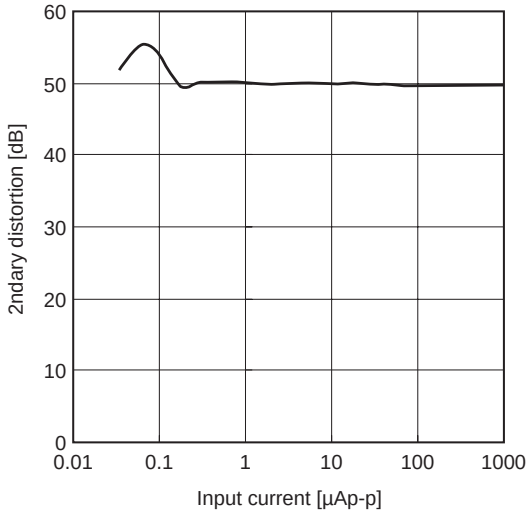
Output voltage vs. Input current



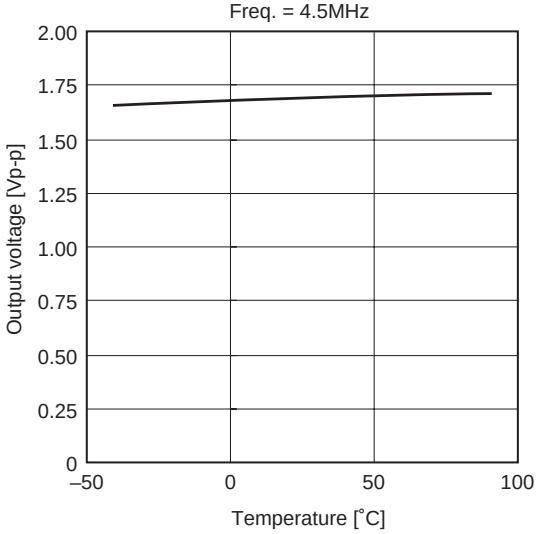
Input current vs. SNR



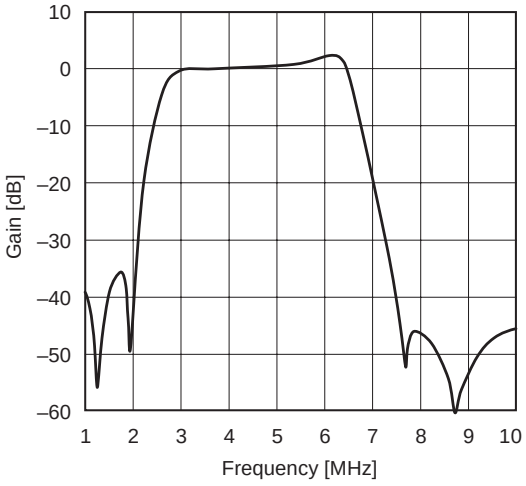
2ndary distortion vs. Input current



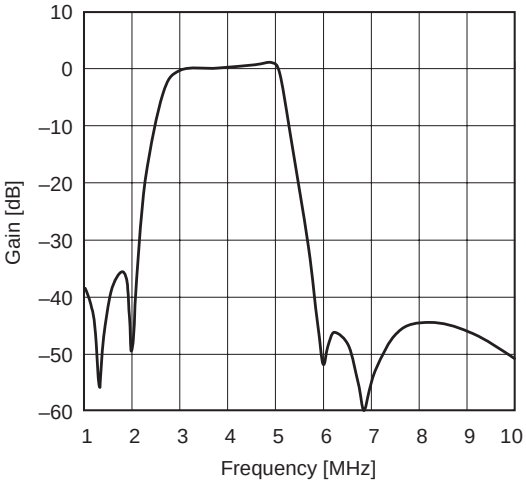
Output voltage vs. Temperature
Input current = 100µAp-p
Freq. = 4.5MHz



Filter characteristic
Full-band mode

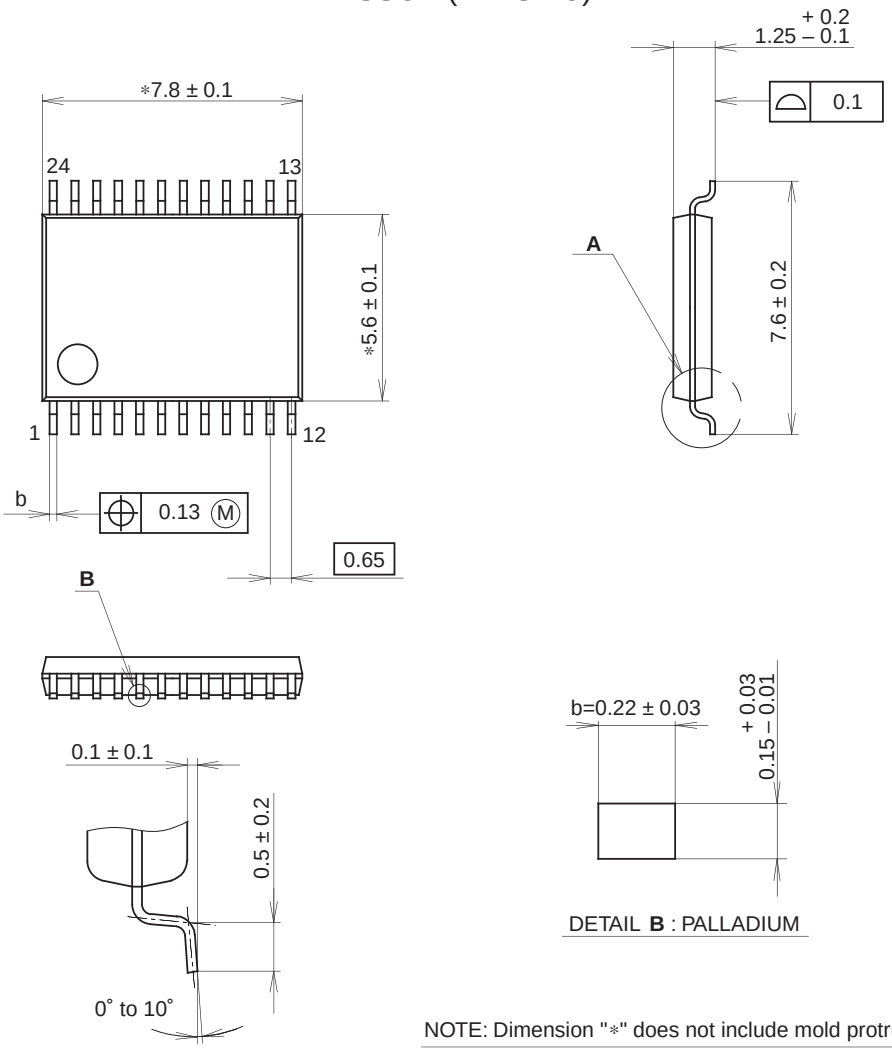


Filter characteristic
Half-band mode



Package Outline Unit: mm

24PIN SSOP (PLASTIC)



DETAIL **A**

DETAIL **B** : PALLADIUM

NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	SSOP-24P-L01
EIAJ CODE	P-SSOP24-7.8x5.6-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g