FM25C160
16Kb FRAM Serial Memory

RAMTRON

Features

16K bit Ferroelectric Nonvolatile RAM
- Organized as 2,048 x 8 bits
- High Endurance 1 Trillion (10^{12}) Read/Writes
- 10 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Very Fast Serial Peripheral Interface - SPI
- Up to 5 MHz maximum Bus Frequency
- Direct hardware replacement for EEPROM
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

Sophisticated Write Protection Scheme
- Hardware Protection
- Software Protection

Low Power Consumption
- 10 µA Standby Current

Industry Standard Configuration
- Industrial Temperature -40° C to +85° C
- 8-pin SOP or DIP

Description

The FM25C160 is a 16-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile but operates in other respects as a RAM. It provides reliable data retention for 10 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

Unlike serial EEPROMs, the FM25C160 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array mere hundreds of nanoseconds after it has been successfully transferred to the device. The next bus cycle may commence immediately. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The FM25C160 is capable of supporting up to 10^{12} read/write cycles -- far more than most systems will require from a serial memory.

These capabilities make the FM25C160 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss.

The FM25C160 provides substantial benefits to users of serial EEPROM, in a hardware drop-in replacement. The FM25C160 uses the high-speed SPI bus, which enhances the high-speed write capability of FRAM technology. The specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration
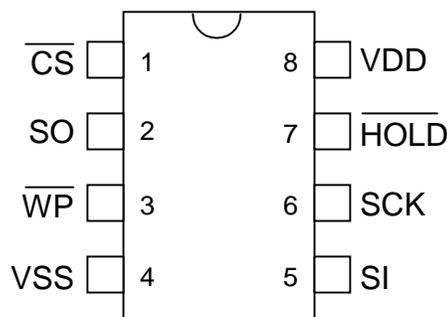
Pin Name	Function
/CS	Chip Select
/WP	Write Protect
/HOLD	Hold
SCK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	5V
VSS	Ground

Ordering Information

FM25C160-P	8-pin plastic DIP
FM25C160-S	8-pin SOP

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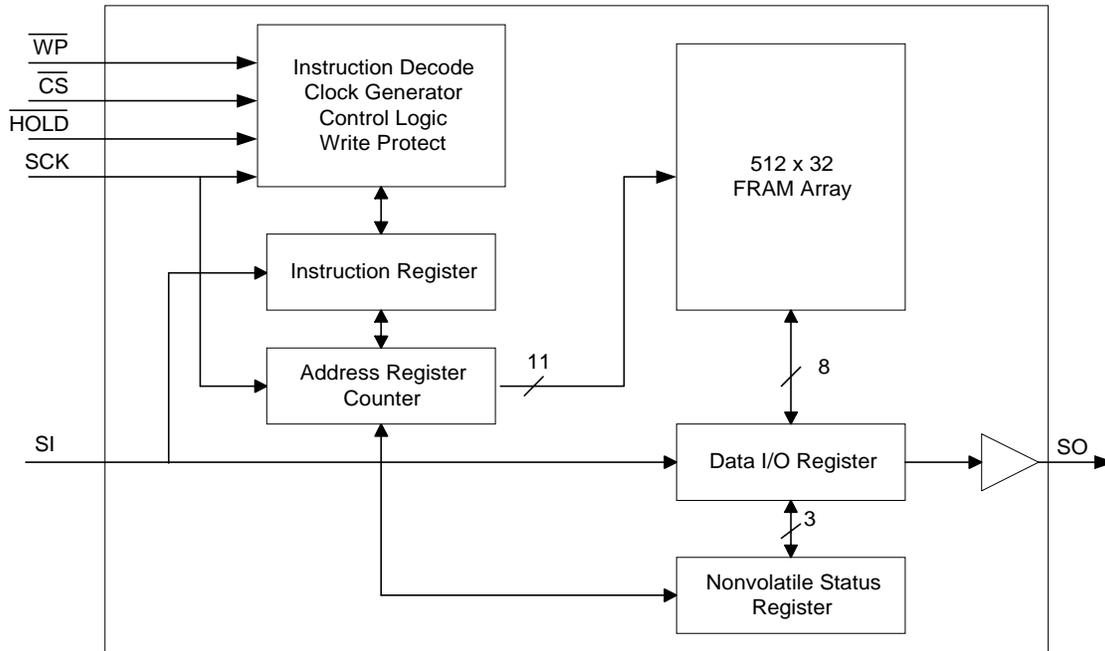
Figure 1. Block Diagram

Pin Description

Pin Name	I/O	Pin Description
/CS	Input	Chip Select: This active low input activates the device. When high, the device enters low-power standby mode, ignores other inputs, and all outputs are tri-stated. When low, the device internally activates the SCK signal. A falling edge on /CS must occur prior to every op-code.
SCK	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Since the device is static, the clock frequency may be any value between 0 and 5 MHz and may be interrupted at any time.
/HOLD	Input	Hold: The /HOLD pin is used when the host CPU must interrupt a memory operation for another task. When /HOLD is low, the current operation is suspended. The device ignores any transition on SCK or /CS. All transitions on /HOLD must occur while SCK is low.
/WP	Input	Write Protect: This active low pin prevents write operations to the status register. This is critical since other write protection features are controlled through the status register. A complete explanation of write protection is provided on page 6. *Note that the function of /WP is different from the FM25160.
SI	Input	Serial Input: All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet IDD specifications. * SI may be connected to SO for a single pin data interface.
SO	Output	Serial Output. SO is the data output pin. It is driven actively during a read and remains tri-state at all other times including when /HOLD is low. Data transitions are driven on the falling edge of the serial clock. * SO may be connected to SI for a single pin data interface.
VDD	Supply	Supply Voltage. 5V
VSS	Supply	Ground

Overview

The FM25C160 is a serial FRAM memory. The memory array is logically organized as 2,048 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the FRAM is similar to serial EEPROMs. The major difference between the FM25C160 and a serial EEPROM with the same pin-out relates to its superior write performance. It also differs from Ramtron's 25160 by supporting SPI mode 3 and the industry standard 16-bit addressing protocol. This makes the FM25C160 a drop-in replacement for most 16Kb SPI EEPROMs that support modes 0 & 3.

Memory Architecture

When accessing the FM25C160, the user addresses 2,048 locations each with 8 data bits. These data bits are shifted serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an op-code and a two-byte address. The upper 5 bits of the address range are 'don't care' values. The complete address of 11-bits specifies each byte address uniquely.

Most functions of the FM25C160 either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation essentially is zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation will be complete. This is explained in more detail in the interface section below.

Users expect several obvious system benefits from the FM25C160 due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that the FM25C160 contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

Serial Peripheral Interface – SPI Bus

The FM25C160 employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 5 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25C160 operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. It is possible to connect the two data lines together. Figure 2 illustrates a typical system configuration using the FM25C160 with a microcontroller that offers an SPI port. Figure 3 shows a similar configuration for a microcontroller that has no hardware support for the SPI bus.

Protocol Overview

The SPI interface is a synchronous serial interface using clock and data lines. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM25C160 will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25C160 supports modes 0 and 3. Figure 4 shows the required signal relationships for modes 0 and 3. For both modes, data is clocked into the FM25C160 on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock begins from a high state, it will fall prior to beginning data transfer in order to create the first rising edge.

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the part. After /CS is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred.

Certain op-codes are commands with no subsequent data transfer. The /CS must go inactive after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.
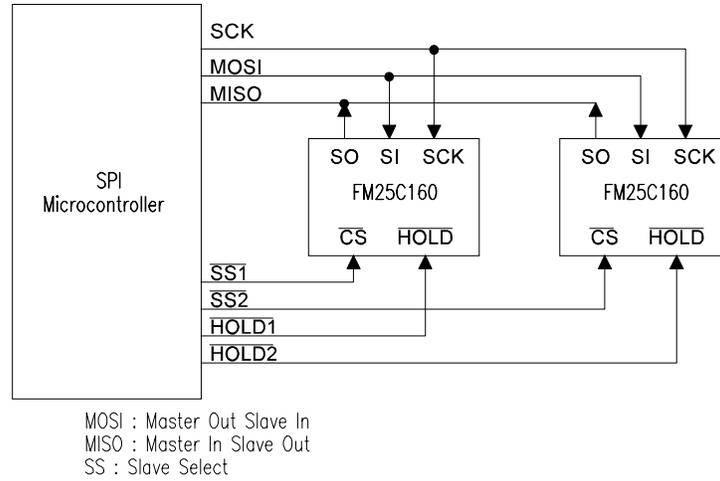
MOSI : Master Out Slave In
MISO : Master In Slave Out
SS : Slave Select

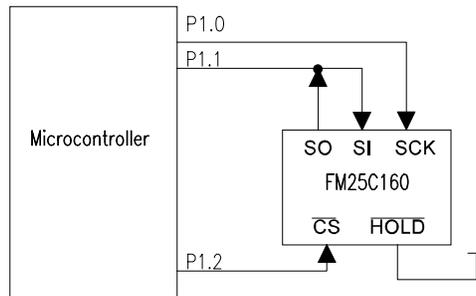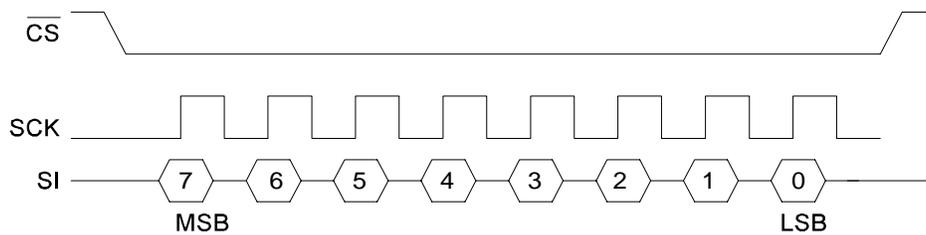**Figure 2. System Configuration with SPI port**

Figure 3. System Configuration without SPI port

SPI Mode 0: CPOL=0, CPHA=0
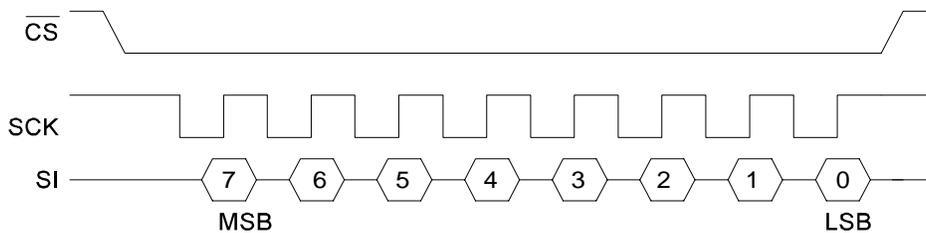

SPI Mode 3: CPOL=1, CPHA=1

Figure 4. SPI Modes 0 & 3

Data Transfer

All data transfers to and from the FM25C160 occur in 8-bit groups. They are synchronized to the clock signal (SCK) and they transfer most significant bit (MSB) first. Serial inputs are clocked in on the rising edge of SCK. Outputs are driven on the falling edge of SCK.

Command Structure

There are six commands called op-codes that can be issued by the bus master to the FM25C160. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, are commands that have no subsequent operations. They perform a single function such as to enable a write operation. Second are commands followed by one byte, either in or out. They operate on the status register. Last are commands for memory transactions followed by address and one or more bytes of data.

Table 1. Op-code Commands

| Name	Description	Op-code value
WREN	Set Write Enable Latch	00000110b
WRDI	Write Disable	00000100b
RDSR	Read Status Register	00000101b
WRSR	Write Status Register	00000001b
READ	Read Memory Data	00000011b
WRITE	Write Memory Data	00000010b

WREN - Set Write Enable Latch

The FM25C160 will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the status register and writing the memory.

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the status register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. A write to the status register has no effect on the WEL bit. Completing any write operation will automatically clear the write-enable latch and prevent further writes without another WREN command. Figure 5 below illustrates the WREN command bus configuration.

WRDI - Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the status register and verifying that WEL=0. Figure 6 illustrates the WRDI command bus configuration.
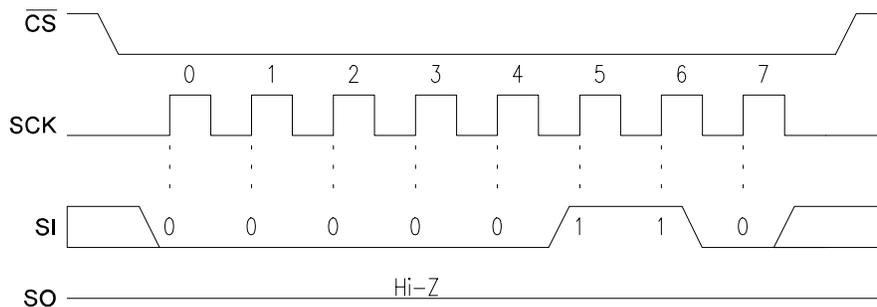
**Figure 5. WREN Bus Configuration**
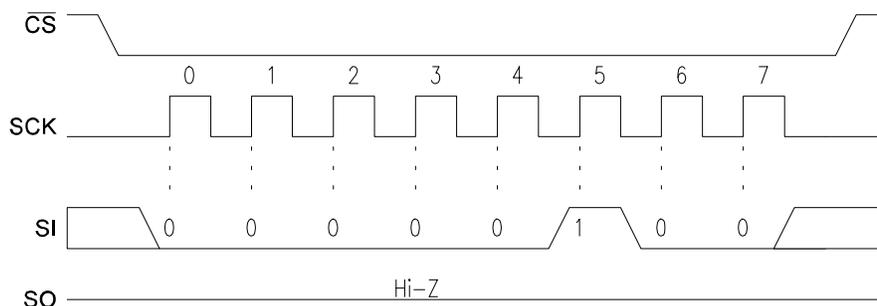
Figure 6. WRDI Bus Configuration

RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25C160 will return one byte with the contents of the Status register. The Status register is described in detail in a later section.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status register. Prior to issuing a WRSR command, the /WP pin must be high or inactive. Note that on the FM25C160, /WP only prevents writing to the Status register, not the memory array. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus timing for RDSR and WRSR are shown below.
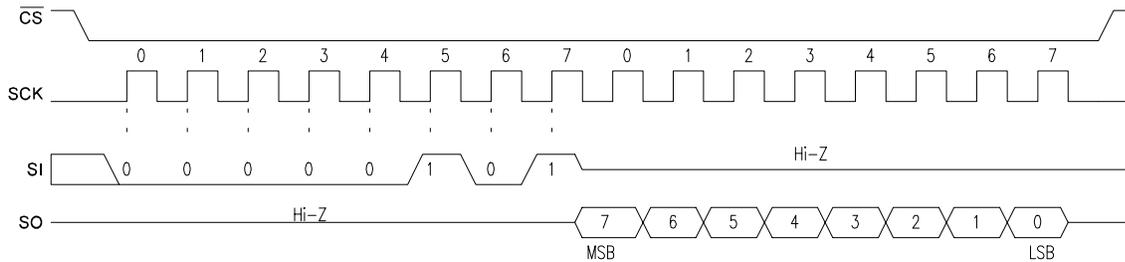
Figure 7. RDSR Bus Timing
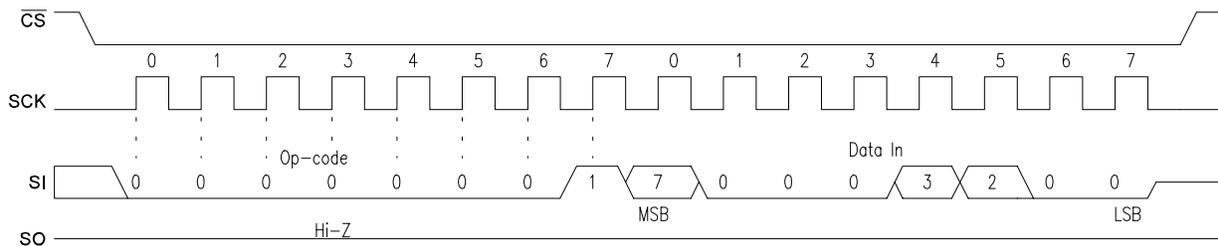
Figure 8. WRSR Bus Timing

Status Register & Write Protection

The write protection features of the FM25C160 are multi-tiered. First, a WREN op-code must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the Status register. As described above, writes to the status register are performed using the WRSR command and subject to the /WP pin. The Status register is organized as follows.

Table 2. Status Register

Bit	7	6	5	4	3	2	1	0
Name	WPEN	0	0	0	BP1	BP0	WEL	0

Bits 0 and 4-6 are fixed at 0 and cannot be modified. Note that the Ready bit in many EEPROMs is unnecessary as the FRAM writes in real-time and is never busy. The WPEN, BP1 and BP0 control write protection features. They are nonvolatile! The WEL

flag indicates the state of the Write Enable Latch. Writing the WEL bit in the status register has no effect.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write protected as shown in the following table.

Table 3. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	600h to 7FFh (upper ¼)
1	0	400h to 7FFh (upper ½)
1	1	000h to 7FFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The WPEN bit controls the effect of the hardware /WP pin. When WPEN is low, the /WP pin is ignored. When WPEN is high, the /WP pin controls write access to the status register. Thus the Status register is write protected if WPEN=1 and /WP=0.

This scheme provides a write protection mechanism, which can prevent software from writing the memory under any circumstances. This occurs if the BP1 and BP0 are set to 1, the WPEN bit is set to 1, and /WP is set to 0. This occurs because the block protect bits prevent writing memory and the /WP signal in hardware prevents altering the block protect bits (if WPEN is high). Therefore in this condition, hardware must be involved in allowing a write operation. The following table summarizes the write protection conditions.

Table 4. Write Protection

WEL	WPEN	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Memory Operation

The SPI interface, with its relatively high maximum clock frequency, highlights the fast write capability of the FRAM technology. Unlike SPI-bus EEPROMs, the FM25C160 can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory array begin with a WREN op-code. The next op-code is the WRITE instruction. This op-code is followed by a two-byte address value. The upper 5-bits of the address are don't care. In total, the 11-bits specify the address of the first byte of the write operation. Subsequent bytes are data and they are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 7FFh is reached, the counter will roll over to 0000h. Data is written MSB first.

Unlike EEPROMs, any number of bytes can be written sequentially and each byte is written to memory immediately after it is clocked in (after the 8th clock). The rising edge of /CS terminates a WRITE op-code operation.

Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Following this instruction is a two-byte address value. The upper 5-bits of the address are don't care. In total, the 11-bits specify the address of the first byte of the read operation. After the op-code and address are complete, the SI line is ignored. The bus master issues 8 clocks, with one bit read out for each. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 7FFh is reached, the counter will roll over to 0000h. Data is read MSB first. The rising edge of /CS terminates a READ op-code operation. The bus configuration for read and write operations is shown below.

Hold

The /HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master takes the /HOLD pin low while SCK is low, the current operation will pause. Taking the /HOLD pin high while SCK is low will resume an operation. The transitions of /HOLD must occur while SCK is low, but the SCK pin can toggle during a hold state.
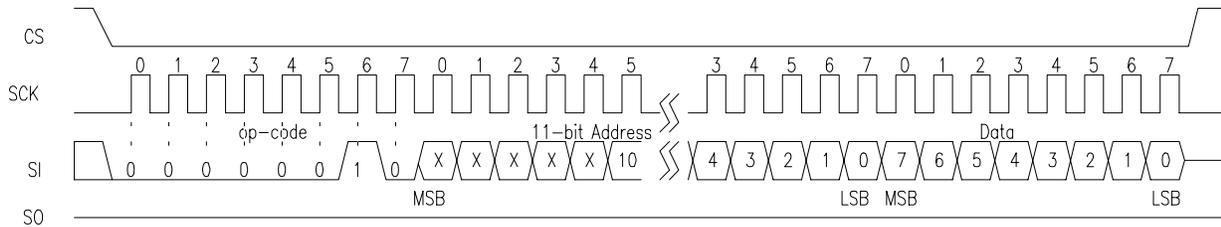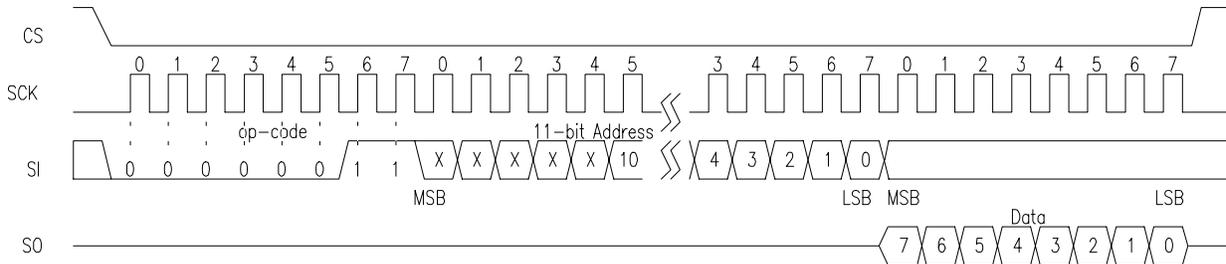
Figure 9. Memory Write

Figure 10. Memory Read

Endurance

Internally, a FRAM operates with a read and restore mechanism similar to a DRAM. Therefore, endurance cycles are applied for each access: read or write. The FRAM architecture is based on an array of rows and columns. Each access causes an endurance cycle for an entire row. Therefore, data locations targeted for substantially differing numbers of cycles should not be located within the same row. In the FM25C160, there are 512 rows each 32 bits wide. Regardless, FRAM read and write endurance is effectively unlimited at the 5MHz clock speed. Even at 2000 accesses per second to the same row, 15 years time will elapse before 10^{12} endurance cycles occur.

Applications

The versatility of FRAM technology fits into many diverse applications. Clearly the strength of higher write endurance and faster writes make FRAM superior to EEPROM in all but one-time programmable applications. The advantage is most obvious in data collection environments where writes are frequent and data must be nonvolatile.

The attributes of fast writes and high write endurance combine in many innovative ways. A short list of ideas is provided here.

1.   Data collection. In applications where data is collected and saved, FRAM provides a superior alternative to other solutions. It is more cost effective than battery backup for SRAM and provides better write attributes than EEPROM.

2.   Configuration. Any nonvolatile memory can retain a configuration. However, if the configuration changes and power failure is a possibility, the higher write endurance of FRAM allows changes to be recorded without restriction. Any time the system-state is altered, the change can be written. This avoids writing to memory on power-down when the available time is short and power scarce.

3.   High noise environments. Writing to EEPROM in a noisy environment can be challenging. When severe noise or power fluctuations are present, the long write time of EEPROM creates a window of vulnerability during which the write can be corrupted. The fast write of FRAM is complete within a microsecond. This time is typically too short for noise or power fluctuations to disturb it.

4.   Time to market. In a complex system, multiple software routines may need to access the nonvolatile memory. In this environment the time delay associated with programming EEPROM adds undue complexity to the software development. Each software routine must wait for complete programming before allowing access to the next routine. When time to market is critical, FRAM can eliminate this simple obstacle. As soon as a write is issued to the FM25C160, it is effectively done -- no waiting.

5.   RF/ID. In the area of contactless memory, FRAM provides an ideal solution. Since RF/ID memory is powered by an RF field, the long programming time and high current consumption needed to write EEPROM is unattractive. FRAM provides a superior solution. The FM25C160 is suitable for multi-chip RF/ID products.

6.   Maintenance tracking. In sophisticated systems, the operating history and system-state during a failure is important knowledge. Maintenance can be expedited when this information has been recorded. Due to the high write endurance, FRAM makes an ideal system log. In addition, the convenient interface of the FM25C160 allows memory to be distributed throughout the system using minimal additional resources.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{IN}, V_{OUT}	Voltage on Any Pin with Respect to V_{SS}	-1.0V to V_{DD}+1V
I_{IN}, I_{OUT}	DC Current on Any Pin	5 mA
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	1
I_{DD}	VDD Supply Current @ SCK = 1.0 MHz @ SCK = 2.0 MHz @ SCK = 5.0 MHz		0.9 1.6 3.0	1.2 2.5 4.5	mA	2
I_{SB}	Standby Current		1	10	µA	3
I_{LI}	Input Leakage Current			10	µA	4
I_{LO}	Output Leakage Current			10	µA	4
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	1, 5
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.5	V	1, 5
V_{OL}	Output Low Voltage @ I_{OL} = 2 mA			0.4	V	1, 5
V_{OH}	Output High Voltage @ I_{OH} = -2 mA	V_{DD} - 0.8			V	1, 5
V_{HYS}	Input Hysteresis	0.05 V_{DD}			V	1, 5

Notes
1. Referenced to V_{SS}.
2. SCK toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V
3. SCK = SI = /CS=V_{DD}. All inputs V_{SS} or V_{DD}.
4. V_{IN} or V_{OUT} = V_{SS} to V_{DD}
5. Characterized but not 100% tested in production.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
f_{CK}	SCK Clock Frequency	0	5.0	MHz	
t_{CH}	Clock High Time	90		ns	
t_{CL}	Clock Low Time	90		ns	
t_{CSU}	Chip Select Setup	90		ns	
t_{CSH}	Chip Select Hold	90		ns	
t_{OD}	Output Disable		100	ns	2
t_{ODV}	Output Data Valid		60	ns	
t_{OH}	Output Hold	0		ns	
t_D	Deselect Time	100		ns	
t_R	Data In Rise Time		1	µs	1, 2
t_F	Data In Fall Time		1	µs	1, 2
t_{SU}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_{HS}	/Hold Setup Time	70		ns	
t_{HH}	/Hold Hold Time	40		ns	
t_{HZ}	/Hold Low to Hi-Z		100	ns	2
t_{LZ}	/Hold High to Data Active		50	ns	2

Notes
1.   Rise and fall times measured between 10% and 90% of waveform.
2.   This parameter is periodically sampled and not 100% tested.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

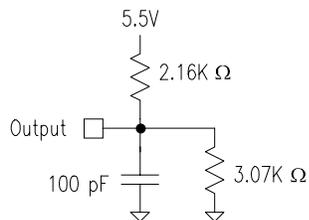| Symbol	Parameter	Max	Units	Notes
C_O	Output capacitance (SO)	8	pF	1
C_I	Input capacitance	6	pF	1

Notes
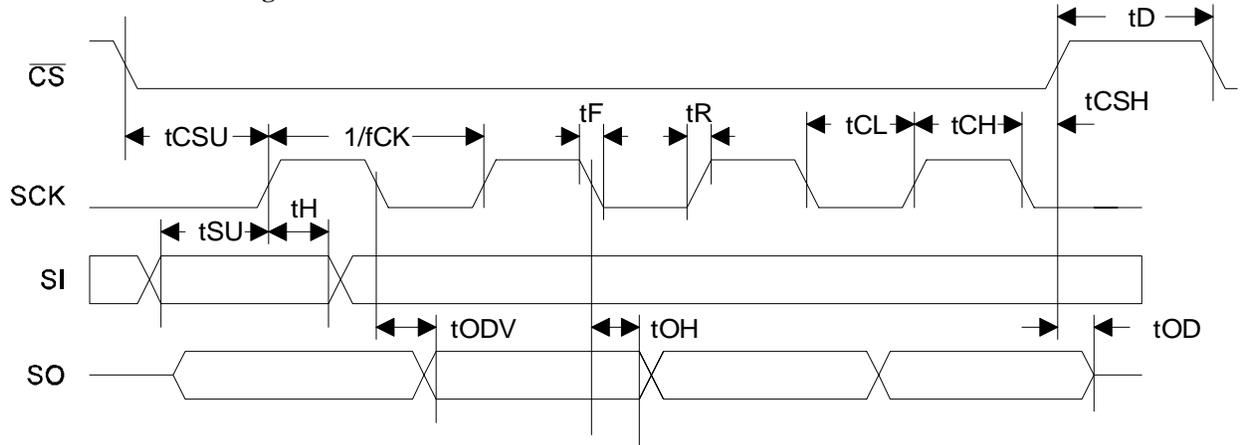1.   This parameter is periodically sampled and not 100% tested.

AC Test Conditions
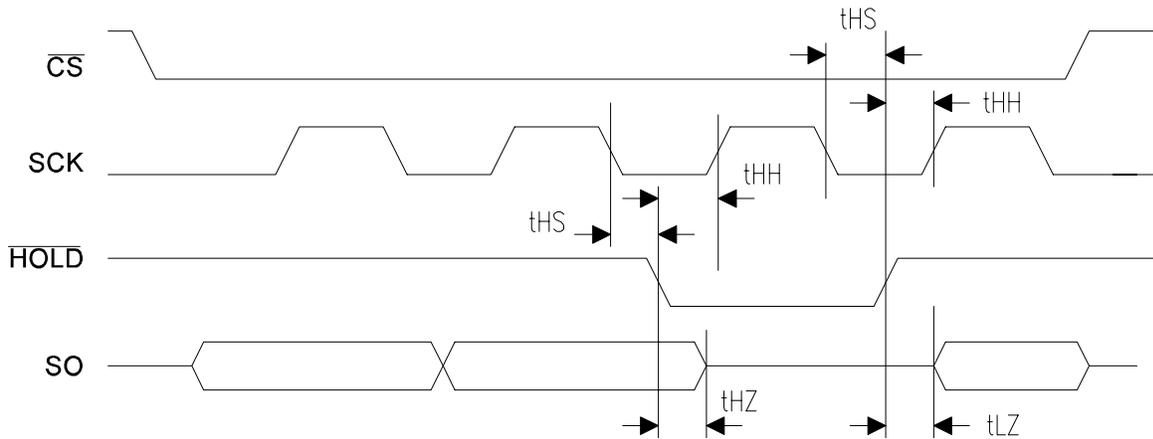
Input Pulse Levels	10% and 90% of V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}

Equivalent AC Load Circuit

Serial Data Bus Timing

/Hold Timing

Data Retention ($V_{DD} = 4.5V$ to $5.5V$ unless otherwise specified)

Parameter	Min	Units	Notes
Data Retention	10	Years	1

Notes
1. The relationship between retention, temperature, and the associated reliability level is characterized in a separate reliability report.
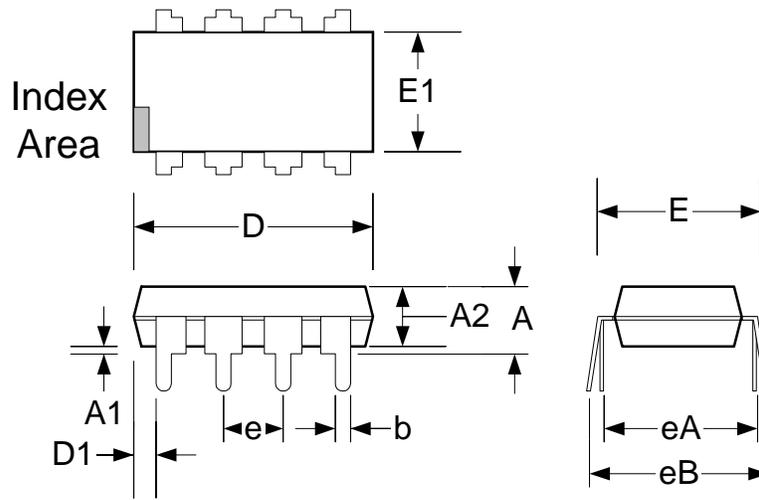
8-pin SOP JEDEC MS-012

Selected Dimensions

Symbol	Dim	Min.	Nom.	Max.
A	mm	1.35		1.75
	in.	0.053		0.069
A1	mm	0.10		0.25
	in.	0.004		0.010
B	mm	0.33		0.51
	in.	0.013		0.020
C	mm	0.19		0.25
	in.	0.007		0.010
D	mm	4.80		5.00
	in.	0.189		0.197
E	mm	3.80		4.00
	in.	0.150		0.157
e	mm		1.27 BSC	
	in.		0.050 BSC	
H	mm	5.80		6.20
	in.	0.228		0.244
h	mm	0.25		0.50
	in.	0.010		0.197
L	mm	0.40		1.27
	in.	0.016		0.050
α		0°		8°

Refer to JEDEC MS-012 for complete dimensions and notes.
Controlling dimensions in <u>millimeters</u>. Conversions to inches are not exact.

8-pin DIP JEDEC MS-001

Selected Dimensions

Symbol	Dim	Min	Nom.	Max
A	in.			0.210
	mm			5.33
A1	in.	0.015		
	mm	0.381		
A2	in.	0.115	0.130	0.195
	mm	2.92	3.30	4.95
b	in.	0.014	0.018	0.022
	mm	0.356	0.457	0.508
D	in.	0.355	0.365	0.400
	mm	9.02	9.27	10.2
D1	in.	0.005		
	mm	0.127		
E	in.	0.300	0.310	0.325
	mm	7.62	7.87	8.26
E1	in.	0.240	0.250	0.280
	mm	6.10	6.35	7.11
e	in.		0.100 BSC	
	mm		2.54 BSC	
eA	in.		0.300 BSC	
	mm		7.62 BSC	
eB	in.			0.430
	mm			10.92
L	in.	0.115	0.130	0.150
	mm	2.92	3.30	3.81

Refer to JEDEC MS-001 for complete dimensions and notes.
Controlling dimensions in <u>inches</u>. Conversions to millimeters are not exact.

Revision History

Revision	Date	Summary
0.0	7/28/00	Initial Release
0.1	7/25/01	Editorial Changes.
2.0	8/5/02	Production status.