Data Sheet | July 1999 | FN4614.1

Radiation Hardened Inverting 3-to-8 Line Decoder/Demultiplexer

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCS138T is a Radiation Hardened 3-to-8 Line Decoder/Demultiplexer. The outputs are active in the low state. Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, E3) are provided. If the device is enabled, the binary inputs (A0, A1, A2) determine which one of the eight normally high outputs will go to a low logic level.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HCS138T are contained in SMD 5962-95727. Visit our website for more information at: **www.intersil.com/**

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9572701TEC	HCS138DTR	-55 to 125
5962R9572701TXC	HCS138KTR	-55 to 125

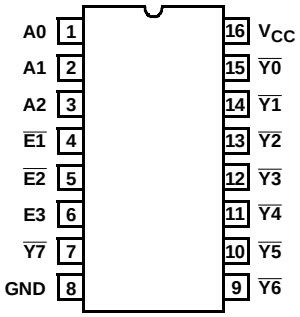
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

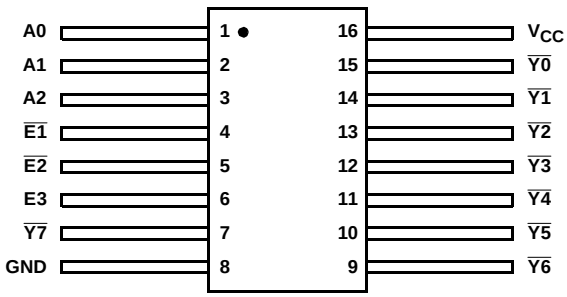
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets: >100 MEV-cm^2/mg
  - Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened SOS CMOS
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - V_{IL} = 0.3 V_{CC} Max
  - V_{IH} = 0.7 V_{CC} Min
- Input Current Levels Ii ≤ 5mA at V_{OL}, V_{OH}

Pinouts

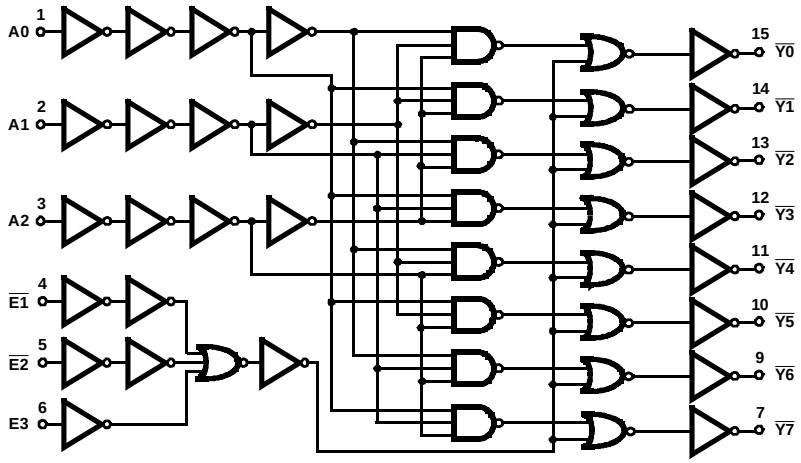
HCS138DTR (SBDIP), CDIP2-T16
TOP VIEW



HCS138KTR (FLATPACK), CDFP4-F16
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE													
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	$\overline{H}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Die Characteristics

DIE DIMENSIONS:

(2159µm x 2565µm x 533µm ±51µm)

85 x 101 x 21mils ±2mil

METALLIZATION:

Type: Al Si

Thickness: 11.0kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Unbiased Silicon on Sapphire

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 13.0kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

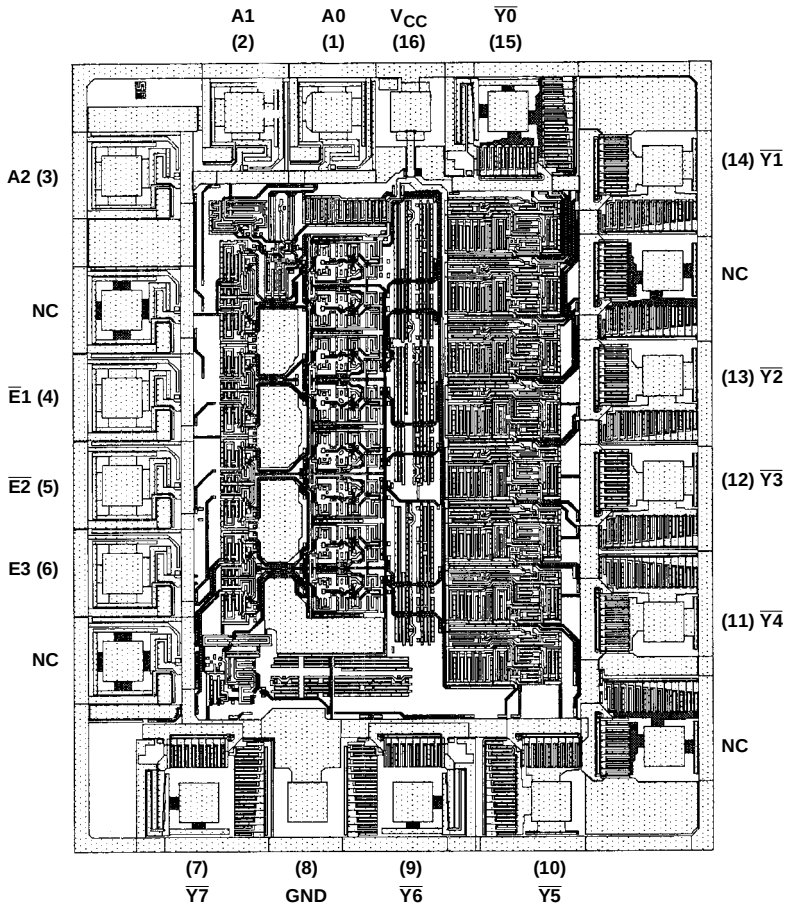
264

PROCESS:

CMOS SOS

Metallization Mask Layout

HCS138T



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCS138 is TA14361A.