HI1276

August 1997

8-Bit, 500 MSPS, Flash A/D Converter

Features

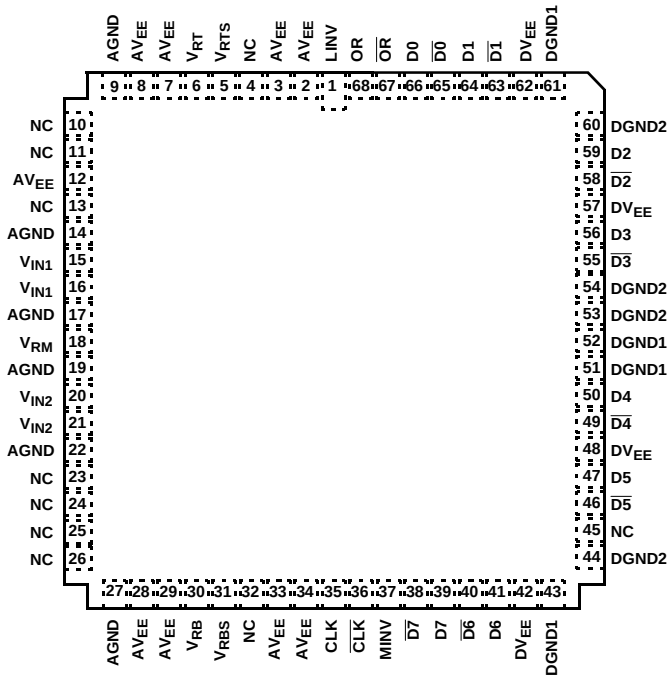
- Differential Linearity Error . . . . . ±0.5 LSB
- Integral Linearity Error . . . . . ±0.7 LSB
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate (Min). . . . . 500 MSPS
- Low Input Capacitance (Typ) 20pF
- Wide Analog Input Bandwidth (Min for Full Scale Input) 300MHz
- Single Power Supply . . . . . -5.2V
- Low Power Consumption (Typ) 2.8W
- Low Error Rate
- Capable of Driving 50Ω Loads
- Direct Replacement for Sony CXA1276K

Applications

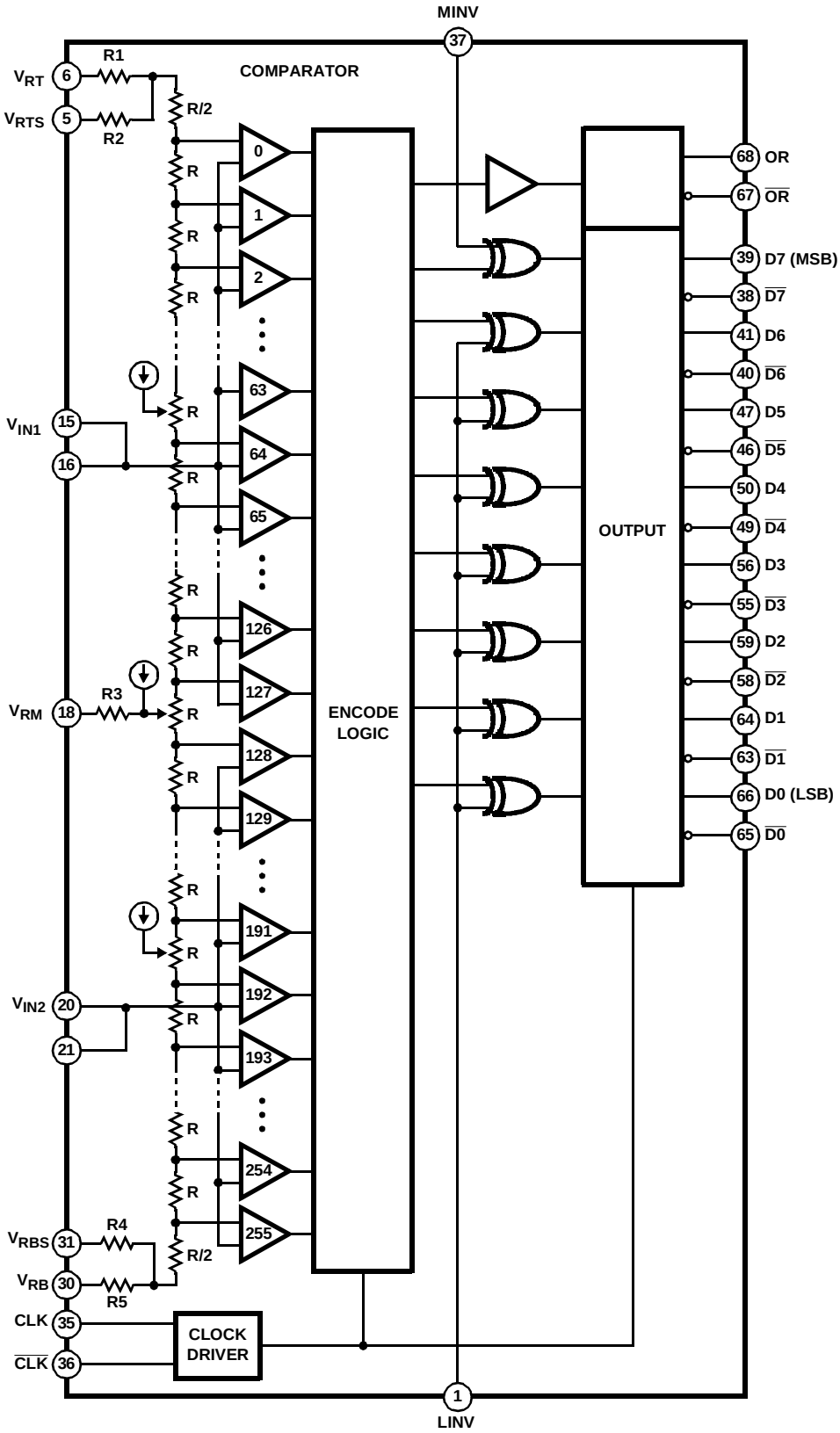
- Radar Systems
- Communication Systems
- Digital Oscilloscopes
- Direct RF Down-Conversion

Pinout

HI1276 (CLCC)
HEAT SINK UP, RECESSED CAVITY DOWN



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V to +0.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7 to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} . . . . . AV_{EE} to +0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
MINV, $\overline{LINV}$ . . . . . -4V to +0.5V
CLK, $\overline{CLK}$, ... DV_{EE} to +0.5V
$|CLK-\overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current
(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$) . . . . . -30mA to 0mA

Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
CLCC Package	18	4

Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions (Note 1)

Supply Voltage	MIN	TYP	MAX
AV_{EE}, DV_{EE}	-5.5V	-5.2V	-4.95V
AV_{EE} - DV_{EE}	-0.05V	0V	0.05V
AGND - DGND	-0.05V	0V	0.05V
Temperature Range (Note 5)			
T_C	-20^oC	-	100^oC

Reference Input Voltage	MIN	TYP	MAX
V_{RT}	-0.1V	-2	0.1V
V_{RB}	-2.2V	-2	-1.8V
Analog Input Voltage, V_{IN}	V_{RB}	-	V_{RT}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL	f_C = 500 MSPS	-	±0.3	±0.7	LSB
Differential Linearity Error, DNL	f_C = 500 MSPS	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1kHz, Full Scale, f_C = 500 MSPS	-	46	-	dB
	Input = 100MHz, Full Scale, f_C = 500 MSPS	-	37	-	dB
Error Rate	Input = 100MHz, Full Scale, Error > 16 LSB, f_C = 400 MSPS	-	10^{-11}	10^{-9}	TPS (Note 3)
	Input = 125MHz, Full Scale, Error > 16 LSB, f_C = 500 MSPS	-	10^{-8}	10^{-6}	TPS (Note 3)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 500 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Overrange Recovery Time		-	1.0	-	ns
Maximum Conversion Rate, f_C		500	-	-	MSPS
Aperture Jitter, t_{AJ}	Input = 150MHz	-	11	-	ps
Sampling Delay, t_{DS}	Input = 150MHz	0.2	0.8	1.5	ns
ANALOG INPUT					
Analog Input Capacitance, C_{IN}	$V_{IN} = 1V + 0.07V_{RMS}$	-	20	-	pF
Analog Input Resistance, R_{IN}		30	70	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	-	-	850	µA
Full Scale Input Bandwidth	$V_{IN} = 2V_{P-P}$	300	-	-	MSPS
REFERENCE INPUTS					
Reference Resistance, R_{REF}		70	110	160	Ω

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Residual Resistance	R1	Note 2	0.1	0.5	2.0	Ω
	R2		0.5	5.2	10	Ω
	R3		0.5	1.6	5.0	Ω
	R4		0.5	8.7	20	Ω
	R5		0.1	0.5	2.0	Ω
DIGITAL INPUTS						
Logic H Level, V_{IH}			-1.10	-	-	V
Logic L Level, V_{IL}			-	-	-1.55	V
Logic H Current, I_{IH}		Input Connected to -0.8V	0	-	70	µA
Logic L Current, I_{IL}		Input Connected to -1.6V	-50	-	60	µA
Input Capacitance			-	6	-	pF
DIGITAL OUTPUTS						
Logic H Level, V_{OH}		$R_L = 50\Omega$	-1.03	-	-	V
Logic L Level, V_{OL}		$R_L = 50\Omega$	-	-	-1.58	V
TIMING CHARACTERISTICS						
Clock Duty Cycle			45	50	55	%
Output Rise Time, t_r		$R_L = 50\Omega$, 20% to 80%	0.5	0.7	1.0	ns
Output Fall Time, t_f		$R_L = 50\Omega$, 80% to 20%	0.5	0.7	1.0	ns
Output Delay, t_{OD}			1.5	1.9	2.3	ns
POWER SUPPLY CHARACTERISTICS						
Supply Current, I_{EE}			-680	-520	-	mA
Power Consumption, P_D		Note 4	-	2.8	3.6	W

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. See Functional Block Diagram.
3. TPS: Times Per Sample.
4. $P_D = I_{EEA} \bullet AV_{EE} + I_{EED} \bullet DV_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$.
5. T_A is specified in still air and without heatsink. To extend temperature range, appropriate heat management techniques must be employed (See Figure 2).

Timing Diagram

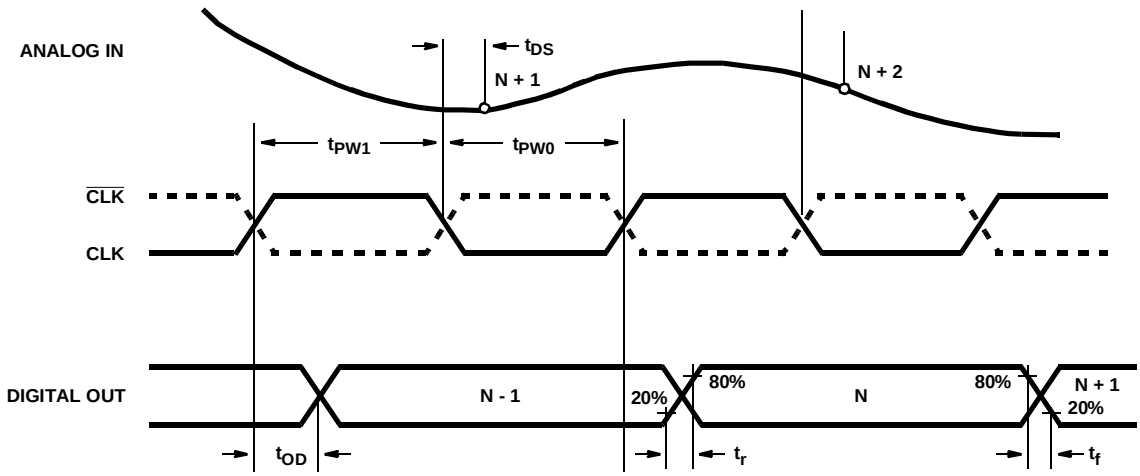


FIGURE 1.

Typical Performance Curves

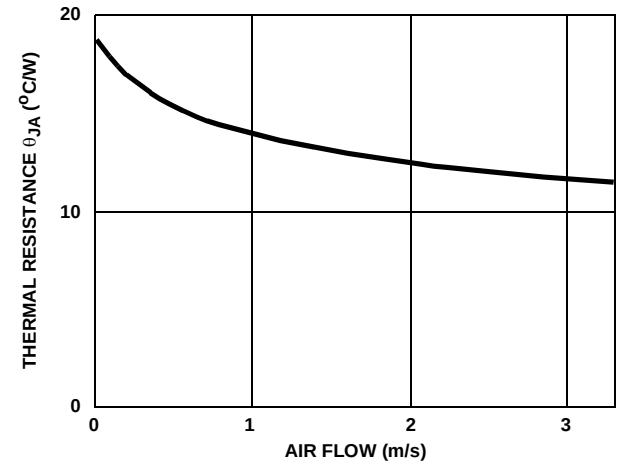


FIGURE 2. THERMAL RESISTANCE MOUNTED ON-BOARD

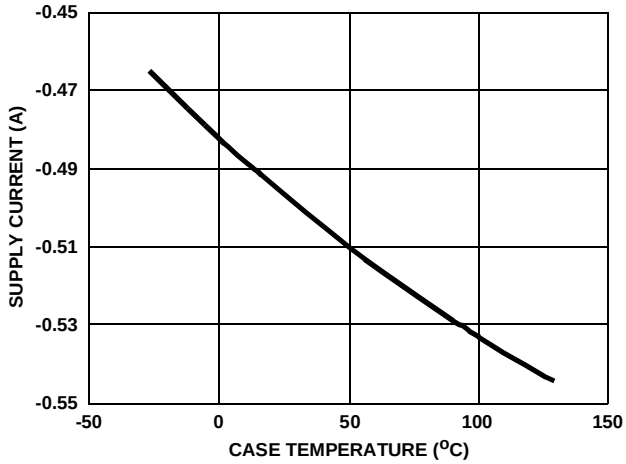


FIGURE 3. SUPPLY CURRENT vs TEMPERATURE CHARACTERISTICS

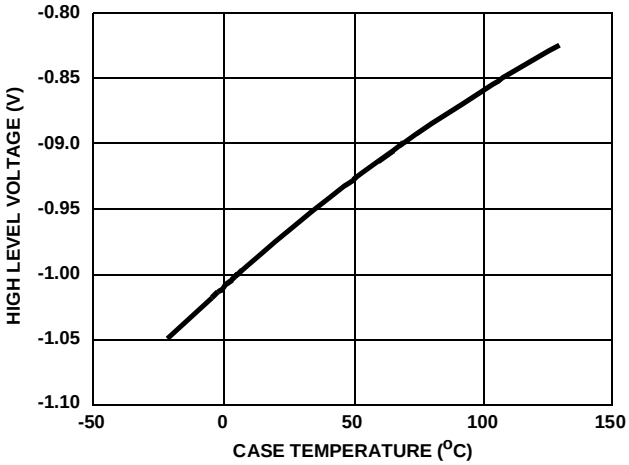


FIGURE 4. DO PIN HIGH LEVEL VOLTAGE vs TEMPERATURE CHARACTERISTICS

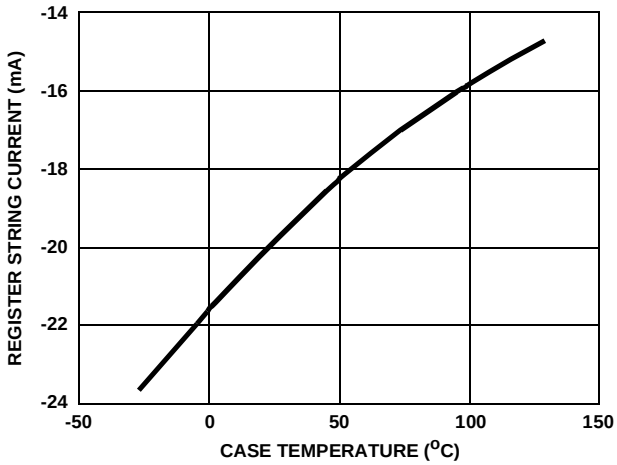


FIGURE 5. REGISTER STRING CURRENT vs TEMPERATURE CHARACTERISTICS

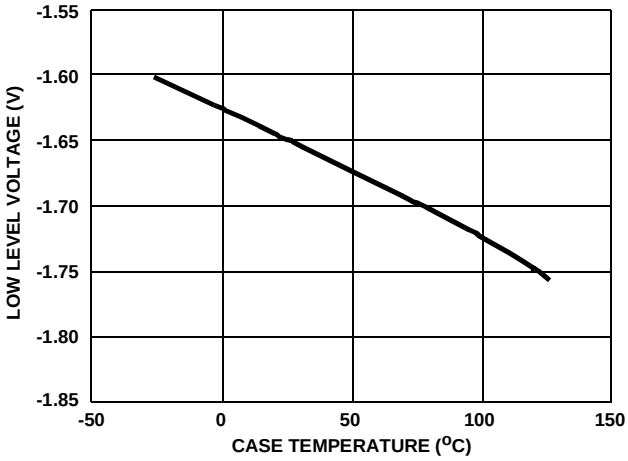


FIGURE 6. D0 PIN LEVEL VOLTAGE vs TEMPERATURE CHARACTERISTICS

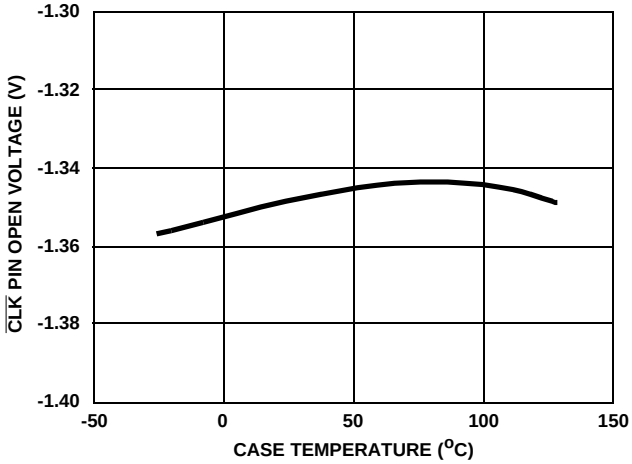


FIGURE 7. $\overline{CLK}$ PIN OPEN VOLTAGE vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

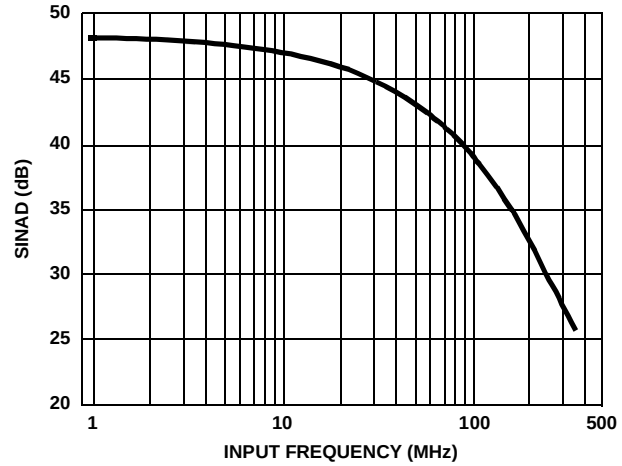


FIGURE 8. SINAD vs INPUT FREQUENCY CHARACTERISTICS

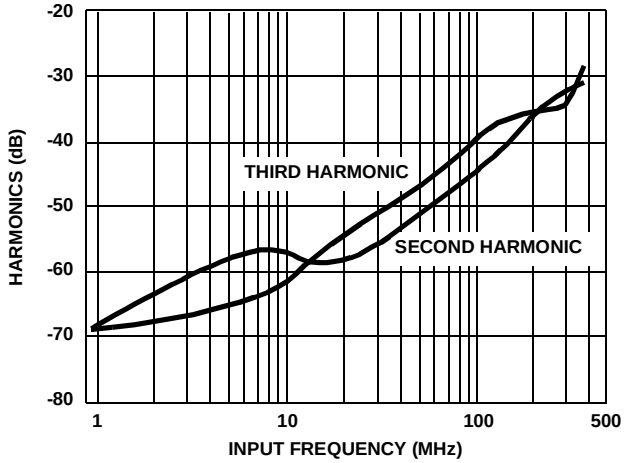


FIGURE 9. HARMONIC DISTORTION vs INPUT FREQUENCY CHARACTERISTICS

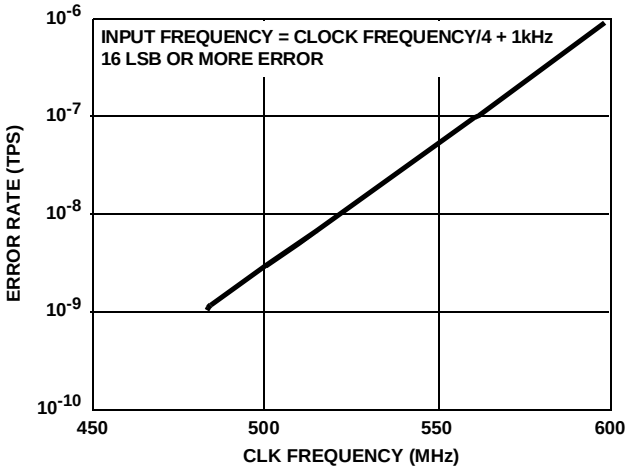


FIGURE 10. ERROR RATE vs CONVERSION FREQUENCY CHARACTERISTICS

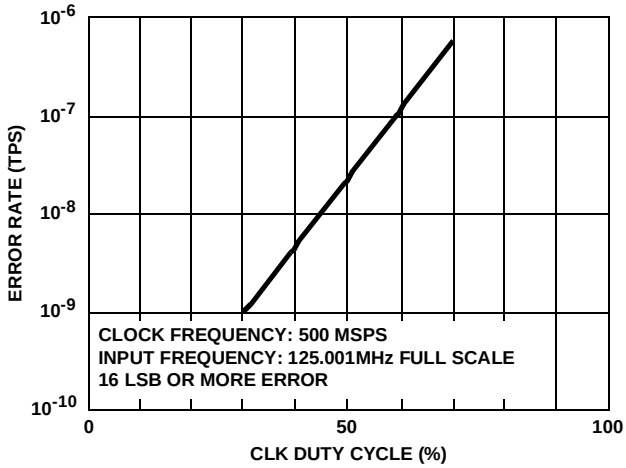


FIGURE 11. ERROR RATE vs CLOCK DUTY CYCLE CHARACTERISTICS

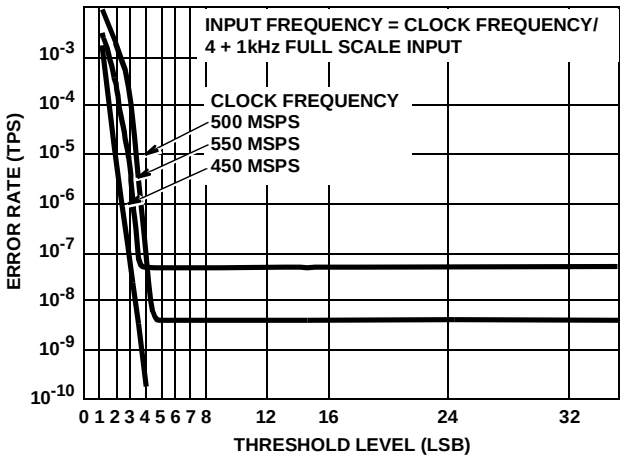
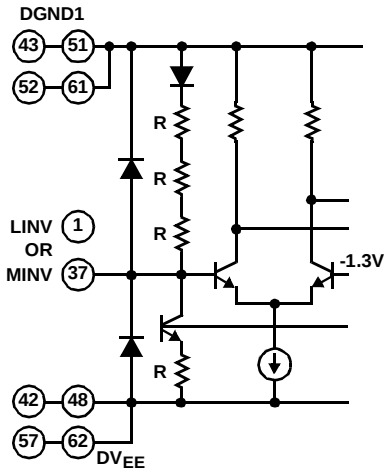
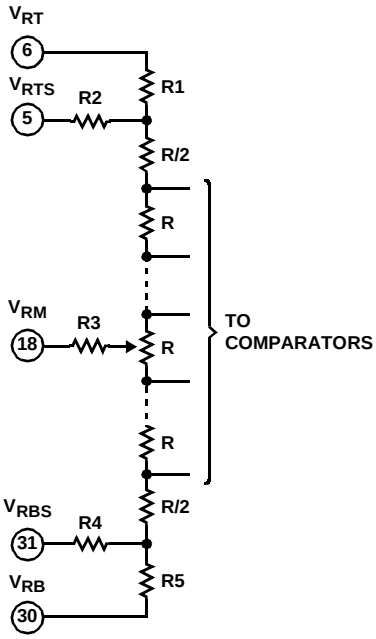
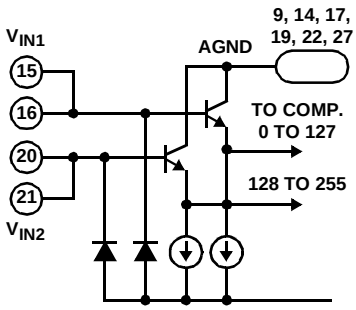


FIGURE 12. ERROR RATE vs THRESHOLD LEVEL CHARACTERISTICS

Pin Descriptions

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	LINV	I	ECL		Polarity Selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.
37	MINV				Polarity Selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.
6	V_{RT}	I	0V		Analog Reference Voltage (Top) (0V Typ).
5	V_{RTS}	O	0V		Reference Voltage Sense (Top).
18	V_{RM}	I	$V_{RB/2}$		Reference Voltage Mid Point. Can be used for linearity compensation.
31	V_{RBS}	O	-2V		Reference Voltage Sense (Bottom).
30	V_{RB}	I	-2V		Analog Reference Voltage (Bottom).
15, 16	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog Input. All of the pins must be wired externally.
20, 21	V_{IN2}				

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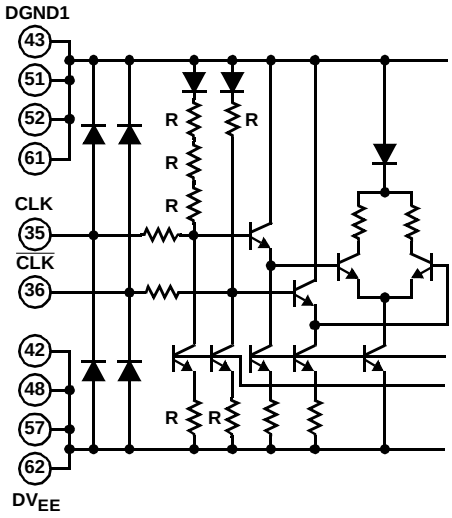
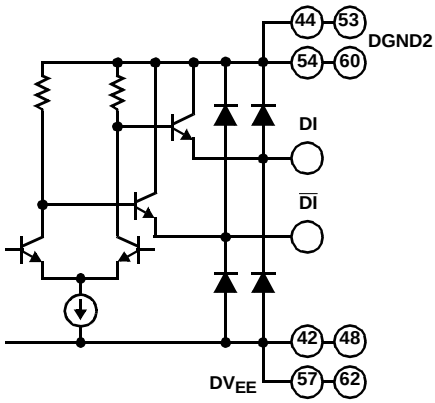
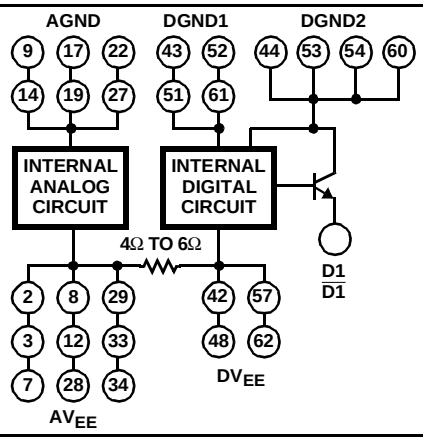
Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
35	CLK	I	ECL		CLK Input.
36	$\overline{CLK}$				Complementary CLK Input. Pulled down to -1.3V when left open.
38, 39	$\overline{D7}$, D7	O	ECL		MSB and Complementary Msb Data Output.
40, 41	$\overline{D6}$, D6				D1 to D6: Data output D1 to D6: Complementary data output
46, 47	$\overline{D5}$, D5				
49, 50	$\overline{D4}$, D4				
55, 56	$\overline{D3}$, D3				
58, 59	$\overline{D2}$, D2				
63, 64	$\overline{D1}$, D1				
65, 66	$\overline{D0}$, D0				LSB Data Complementary Output LSB Data Output.
67, 68	$\overline{OR}$, OR				Overrange and Complementary Overrange Output.
2, 3, 7, 8, 12, 28, 29, 33, 34	AV_{EE}	-	-5.2V		Analog Supply. Internally connected to DV_{EE} (resistance: 4Ω to 6Ω).
9, 14, 17, 19, 22, 27	AGND		0V		Analog Ground.
42, 48, 57, 62	DV_{EE}		-5.2V		Digital Supply. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω).
43, 51, 52, 61	DGND1		0V		Digital Ground.
44, 53, 54, 60	DGND2 (Note 6)		0V		Digital Ground for Output Drive.
4, 10, 11, 13, 23, 24, 25, 26, 32	NC				No-Connect pins. It is recommended to wire these pins to AGND.
45	NC				No-Connect pin. It is recommended to wire these pins to DGND.

NOTE:

6. $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or open, $V_{RB} = V_{RBS} = -2V$

A/D OUTPUT CODE TABLE

(NOTE 1) V_{IN}	STEP	MINV 1, LINV 1			0, 1			1, 0			0, 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		1	000 • • • • • 00		1	100 • • • • • 00		1	011 • • • • • 11		1	111 • • • • • 11	
	0	0	000 • • • • • 00		0	100 • • • • • 00		0	011 • • • • • 11		0	111 • • • • • 11	
	1	0	000 • • • • • 01		0	100 • • • • • 01		0	011 • • • • • 10		0	111 • • • • • 10	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
-1V	127	0	011 • • • • • 11		0	111 • • • • • 11		0	000 • • • • • 00		0	100 • • • • • 00	
	128	0	100 • • • • • 00		0	000 • • • • • 00		0	111 • • • • • 11		0	011 • • • • • 11	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
	254	0	111 • • • • • 10		0	011 • • • • • 10		0	100 • • • • • 01		0	000 • • • • • 01	
	255	0	111 • • • • • 11		0	011 • • • • • 11		0	100 • • • • • 00		0	000 • • • • • 00	
-2V		0	111 • • • • • 11		0	011 • • • • • 11		0	100 • • • • • 00		0	000 • • • • • 00	

Test Circuits

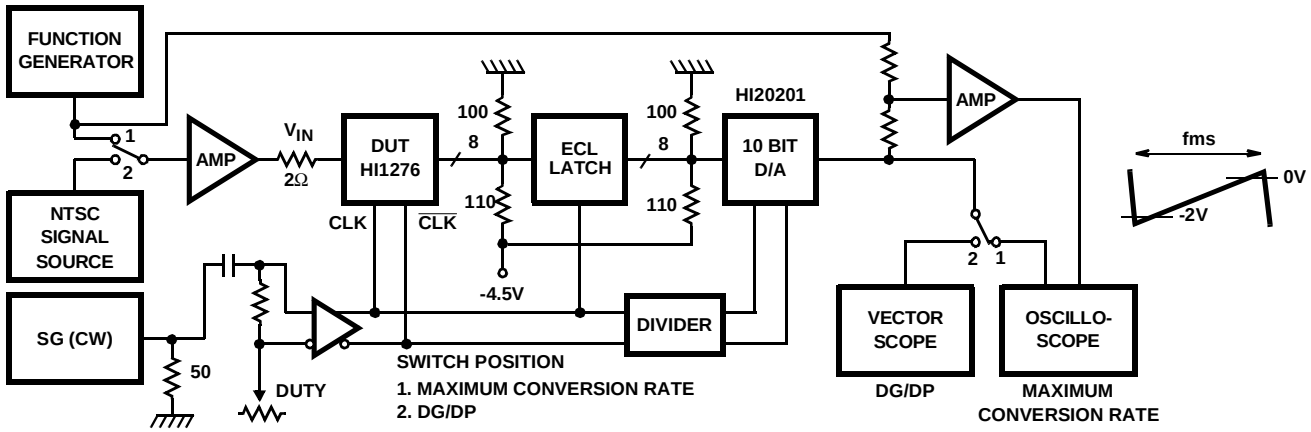


FIGURE 13. MAXIMUM CONVERSION RATE AND DIFFERENTIAL GAIN/PHASE ERROR TEST CIRCUIT

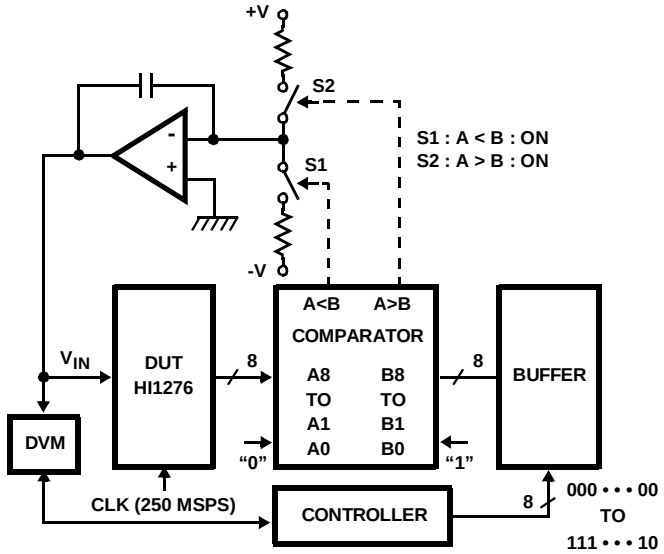


FIGURE 14. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

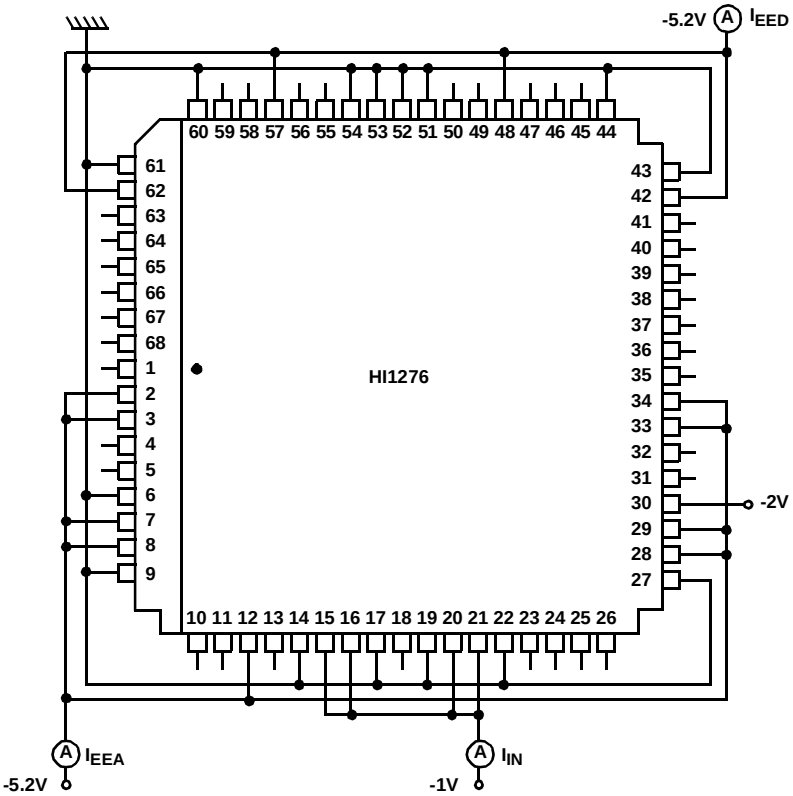


FIGURE 15. POWER SUPPLY AND ANALOG INPUT BIAS CURRENT TEST CIRCUIT

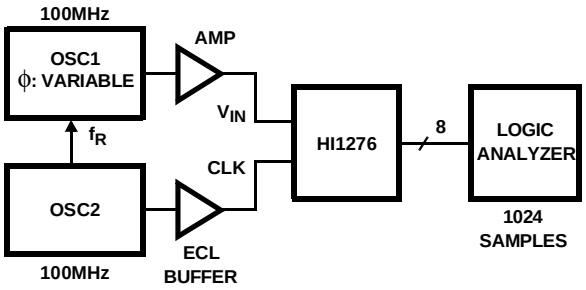
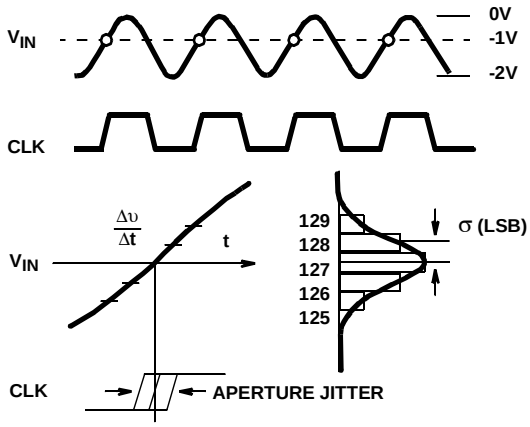


FIGURE 16A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma / \frac{\Delta\upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right),$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 16B. APERTURE JITTER TEST METHOD

FIGURE 16. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT