HI2315

10-Bit, 80 MSPS D/A Converter (Ultra-Low Glitch Version)

August 1997

Features

- **Throughput Rate 80MHz**
- **Low Power 150mW**
- **Single Power Supply . . . . . +5V**
- **Differential Linearity Error . . . . . ±0.5 LSB**
- **TTL/CMOS Compatible Inputs**
- **Built in Bandgap Voltage Reference**
- **Power Down and Blanking Control Pins**
- **Low Glitch**
- **Pin Compatible with Sony CXD2306**
- **Direct Replacement for Sony CXD2315Q**

Applications

- **Wireless Communications**
- **Direct Digital Frequency Synthesis**
- **Signal Reconstruction**
- **Test Equipment**
- **High Resolution Imaging and Graphics Systems**

Description

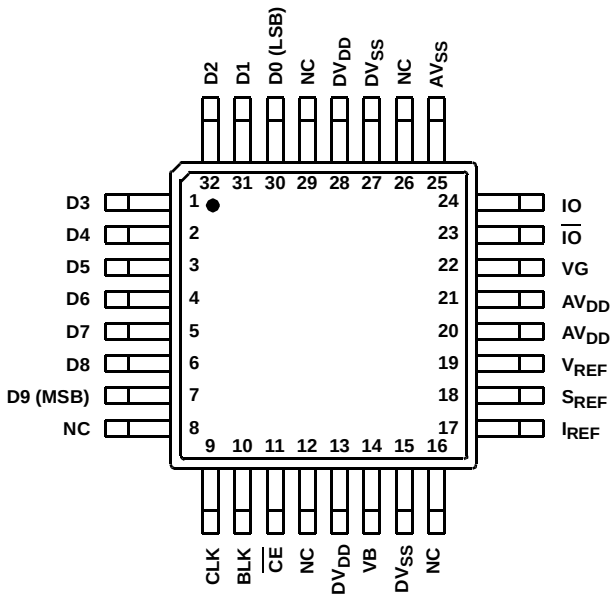
The HI2315 is a 10-bit, 80MHz, high speed, low power CMOS D/A converter. The converter incorporates a 10-bit input data register with current outputs. The HI2315 includes a power down feature that reduces power consumption and a blanking control. The on-chip bandgap reference can be used to set the output current range of the D/A.

Ordering Information

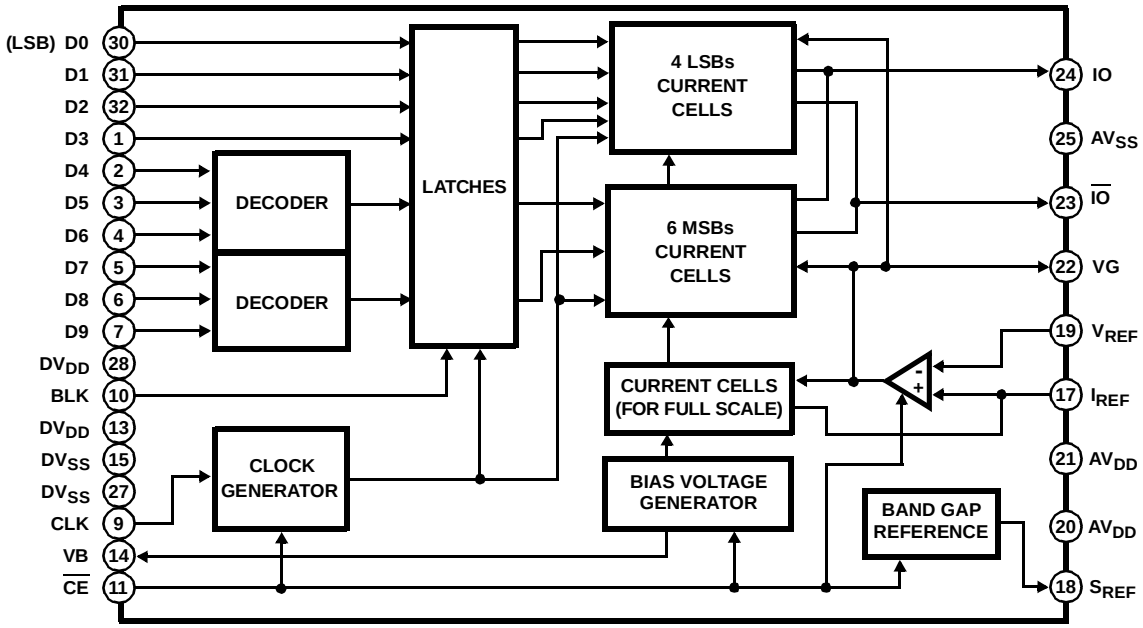
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2315JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S

Pinout

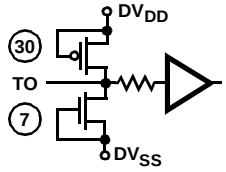
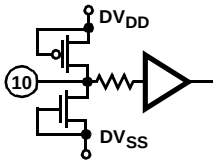
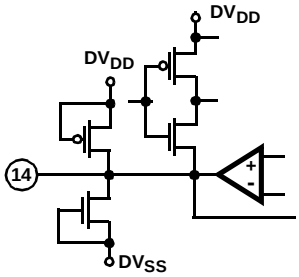
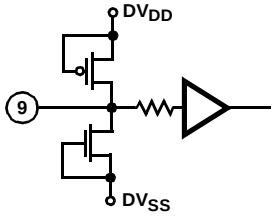
HI2315
(MQFP)
TOP VIEW



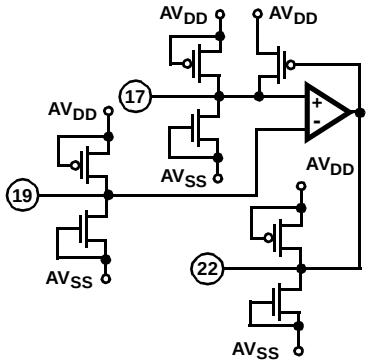
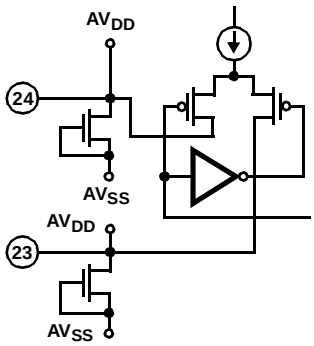
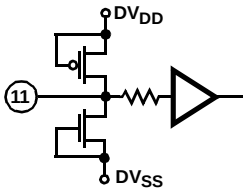
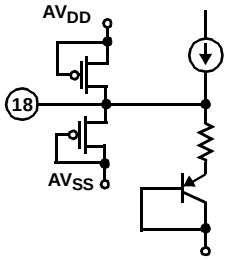
Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
30 to 32 1 to 7	D0 to D9		Digital Input.
10	BLK		Blanking pin. No signal (0V output) at high and output state at low.
14	VB		Connect a capacitor of approximately 0.1µF.
9	CLK		Clock pin.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
15, 27	DV_{SS}		Digital GND.
25	AV_{SS}		Analog GND.
17	I_{REF}		Connect resistance “16R” which is 16 times output resistance “R”.
19	V_{REF}		Sets output full scale value.
22	VG		Connect a capacitor of approximately 0.1µF.
20, 21	AV_{DD}		Analog V_{DD}.
24	IO		Current Output pin. Output can be retrieved by connecting resistance. The standard is 200Ω.
23	$\overline{IO}$		Inverted Current Output pin. Connect to GND normally.
13, 28	DV_{DD}		Digital V_{DD}.
11	$\overline{CE}$		Chip Enable pin. No signal (0V output) at high makes power consumption minimum.
18	S_{REF}		Independent Constant-Voltage Source Output pin using band gap reference. Stable voltage independent of the fluctuation for supply voltage can be obtained by connecting to V_{REF}. See Application Circuit 2 for details.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}) . . . . . V_{SS} -0.5V to V_{DD} + 0.5V
Output Voltage (I_{OUT}) . . . . . 0mA to 15mA

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . 5.0V ±±0.25V
DV_{DD}, DV_{SS} . . . . . 5.0V ±±0.25V
Reference Input Voltage (V_{REF}) . . . . . 0.5V to 2.0V
Clock Pulse Width (t_{PW1}, t_{PW0}) . . . . . 6.25ns (Min)
Temperature Range (T_{OPR}) . . . . . -20^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (MQFP Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, f_{CLK} = 80MHz, V_{DD} = 5V, R = 200Ω, V_{REF} = 2.0V, 16R = 3.3kΩ

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	10	-	Bit
Maximum Conversion Rate		f_{MAX}		80	-	-	MHz
Linearity Error		EL		-1.5	-	1.5	LSB
Differential Linearity Error		ED		-0.5	-	0.5	LSB
Output Full-Scale Voltage		V_{FS}		1.8	1.94	2.0	V
Output Full-Scale Current		I_{FS}		9.0	9.7	10	mA
Output Off-Set Voltage		V_{OS}		-	-	1	mV
Output Impedance				-	300	-	kΩ
Supply Current		I_{DD}		-	-	30	mA
Digital Input Current	High Level	I_{IH}		-	-	5	µA
	Low Level	I_{IL}		-5	-	-	µA
Digital Input Voltage	High Level	V_{IH}		2.45	-	-	V
	Low Level	V_{IL}		-	-	0.85	V
Accuracy Guarantee Output Voltage Range		V_{OC}		1.8	1.94	2.0	V
Setup Time		t_S		3.0	-	-	ns
Hold Time		t_H		3.0	-	-	ns
Rise Time		t_r		5.0	-	-	ns
Propagation Delay Time		t_{PD}		-	5	-	ns
Glitch Energy		GE	R_{OUT} = 200Ω, $2V_{P-P}$	-	-	30	pV/s
Differential Gain		DG		-	-	1.0	%
Differential Phase		DP		-	-	1.0	Degrees
S_{REF} Output Voltage		S_{REF}	$T_A = 25^oC$	1.0	1.2	1.4	V

Test Circuits

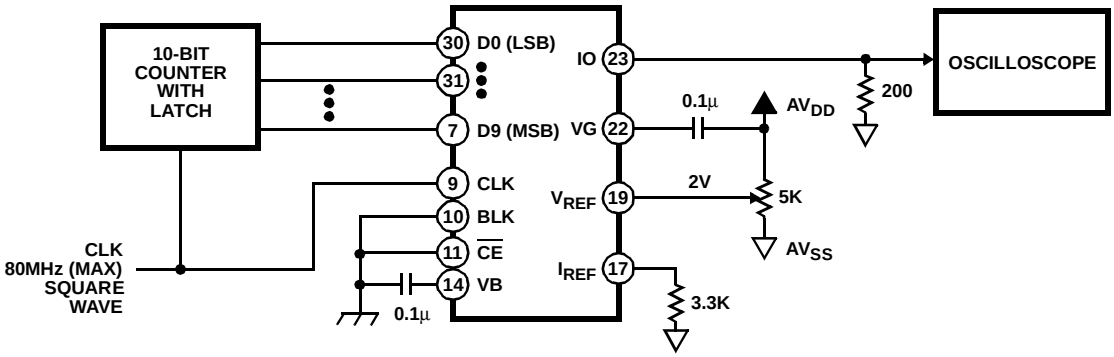


FIGURE 1. MAXIMUM CONVERSION RATE TEST CIRCUIT

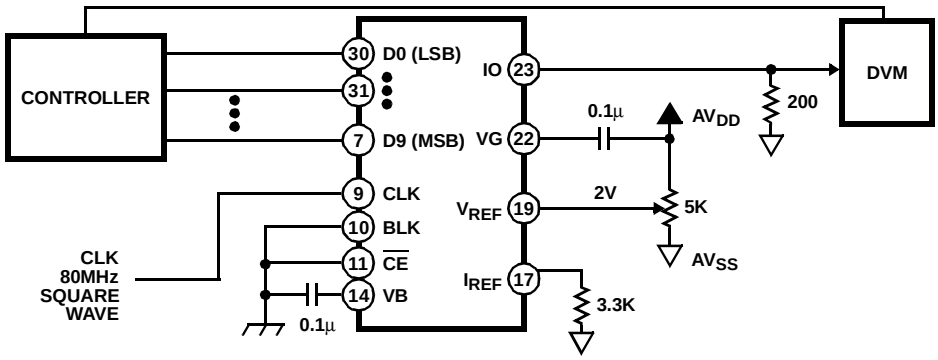


FIGURE 2. DC CHARACTERISTICS TEST CIRCUIT

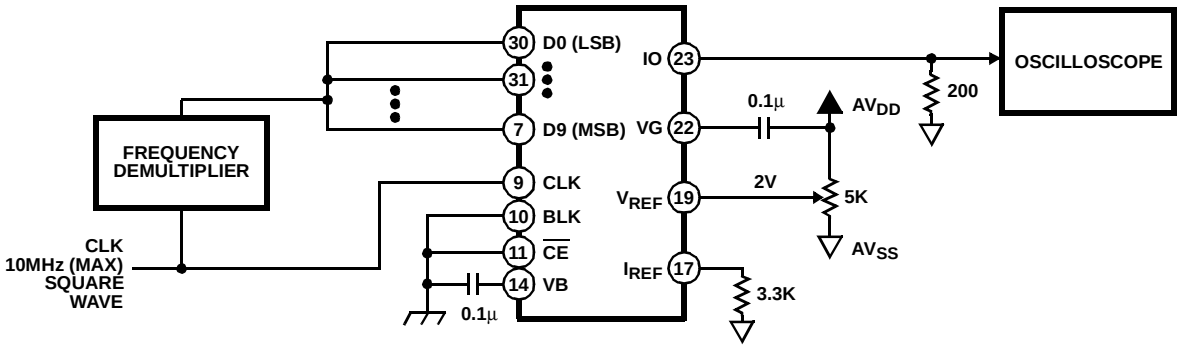


FIGURE 3. PROPAGATION DELAY TIME TEST CIRCUIT

Test Circuits (Continued)

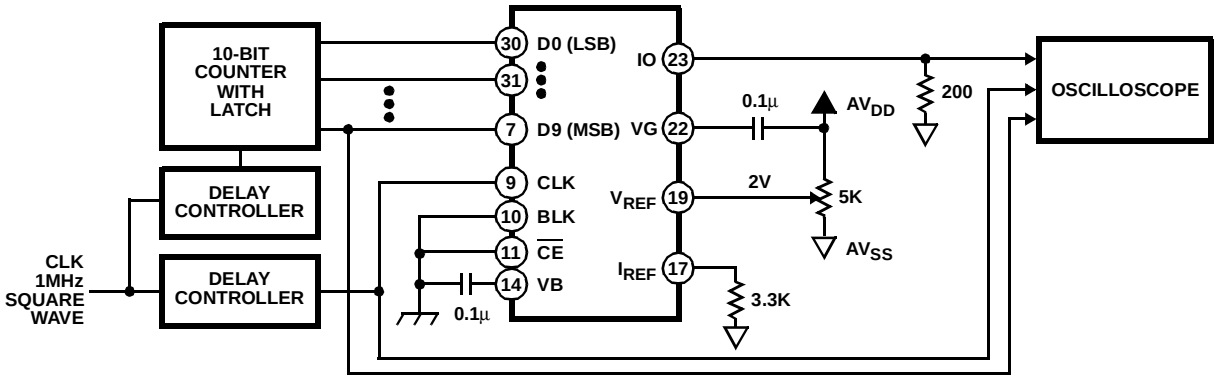


FIGURE 4. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

Timing Diagram

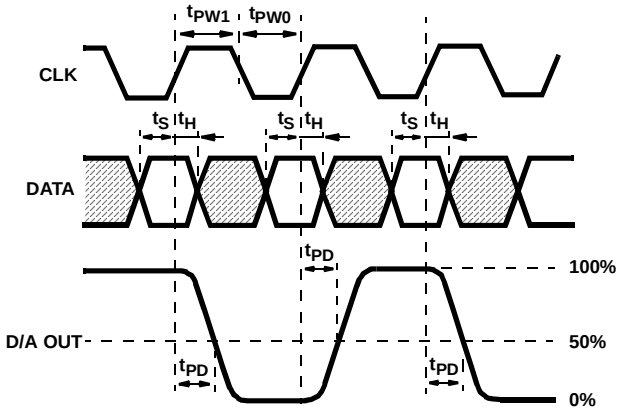
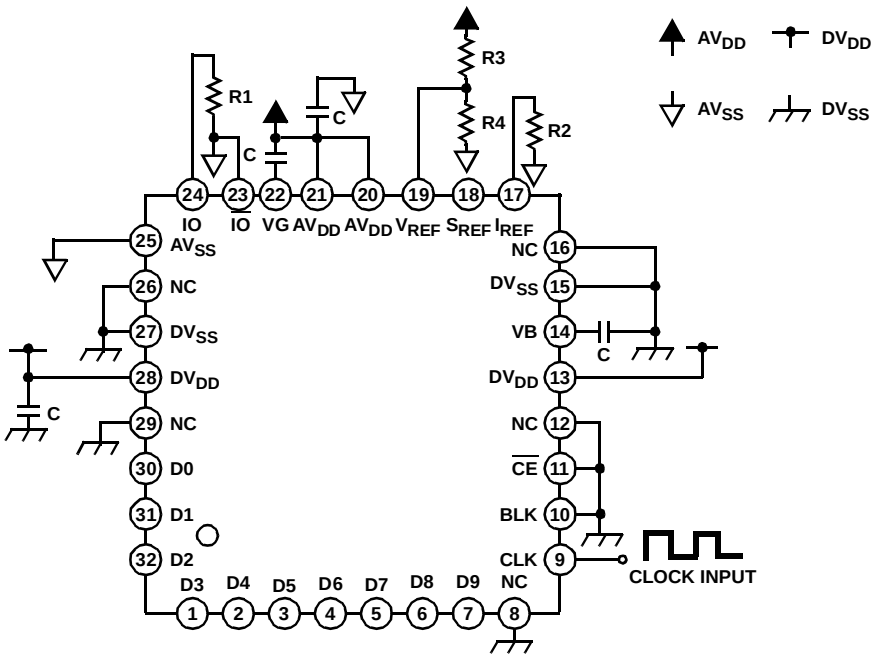


TABLE 1. I/O CORRESPONDENCE TABLE
(2.00V Output Full Scale Voltage)

INPUT CODE	OUTPUT VOLTAGE
MSB ... LSB	
1 1 1 1 1 1 1 1 1 1	2.0V
⋮	
1 0 0 0 0 0 0 0 0 0	1.0V
⋮	
0 0 0 0 0 0 0 0 0 0	0V

Typical Application Circuits

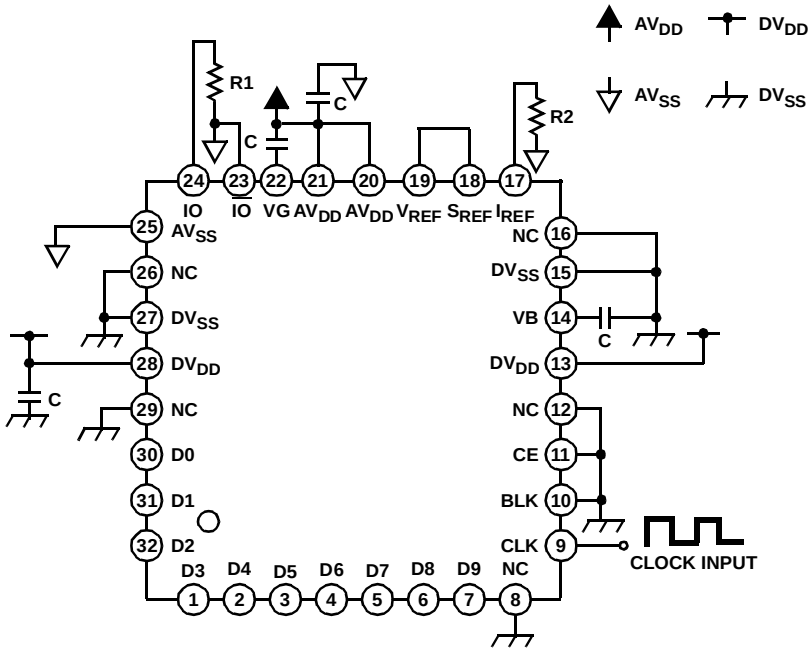


NOTE:

2. When 5.0V supply voltage (DV_{DD} and AV_{DD}). Digital input from pins 30 to 32 and pins 1 to 7. Pin 18 is Left Open When Using Normally. R1 = 200Ω, R2 = 3.3Ω (Resistance 16 Times R1), R3 = 3.0kΩ, R4 = 2.0kΩ, C = 0.1μF.

FIGURE 5. APPLICATION CIRCUIT 1

Typical Application Circuits (Continued)



NOTE:

3. When 5.0V supply voltage (DV_{DD} and AV_{DD}). Digital input from pins 30 to 32 and pins 1 to 7. R1 = 200Ω, R2 = 2.0kΩ, C = 0.1µF.

FIGURE 6. APPLICATION CIRCUIT 2

Typical Performance Curves

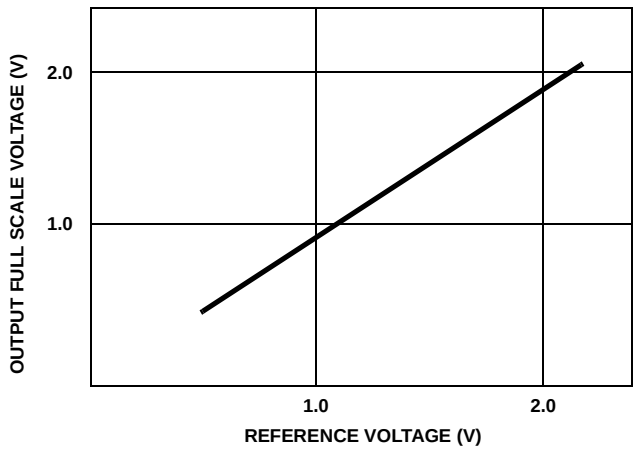


FIGURE 7. OUTPUT FULL SCALE VOLTAGE (V_{FS}) vs REFERENCE VOLTAGE (V_{REF})

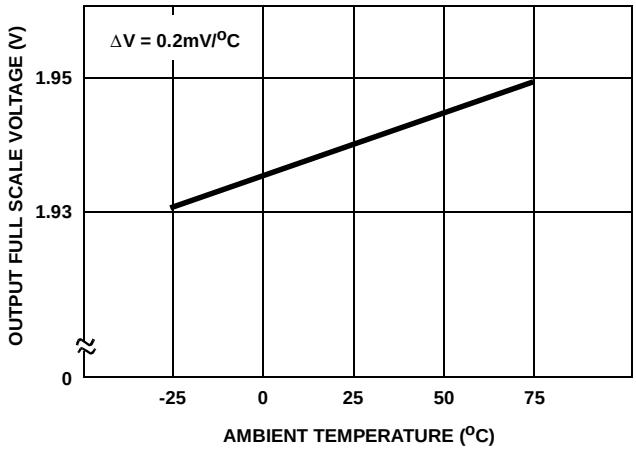


FIGURE 8. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

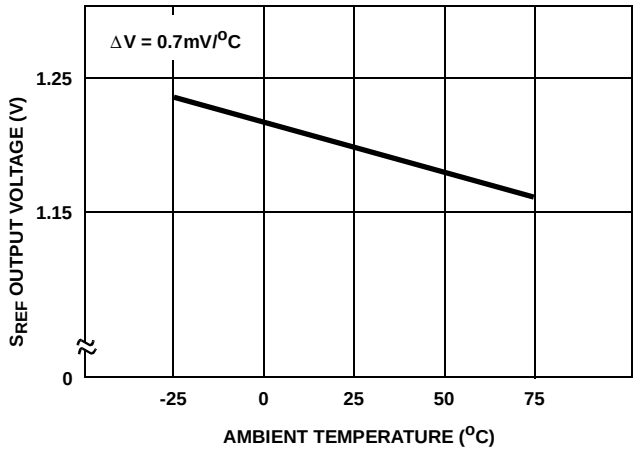


FIGURE 9. S_{REF} vs AMBIENT TEMPERATURE

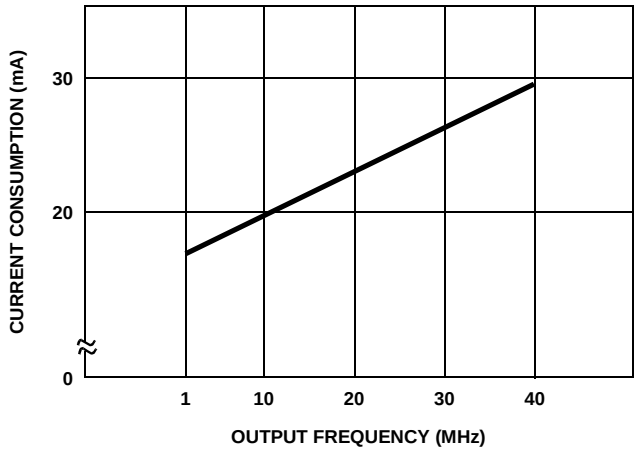


FIGURE 10. OUTPUT FREQUENCY vs CURRENT CONSUMPTION

NOTE:

4. Standard Measurement Conditions and Description: V_{DD} = 5.0V, V_{REF} = 2.0V, R = 200Ω, 16R - 3.3kΩ, T_A = 25°C. The temperature characteristics of external input data in Figure 10 = all “0” and “1” of rectangular wave; clock frequency = 80MHz.

GE (Glitch Energy)

GE, as described in the HI2315, is a spike noise which appears synchronizing with the clock falling edge when the input data (for 1 to 1024 input) changes to 128, 256, 384, 512, 640, 768, 896, and 1024. Figure 11 shows the change state of GE for the staircase wave output, and Figure 12 shows the repetitive output waveform where the GE appears. These figures exhibit the difference of this IC from the convention device.

The HI2315 reduces the GE as shown in Figures 11 and 12.

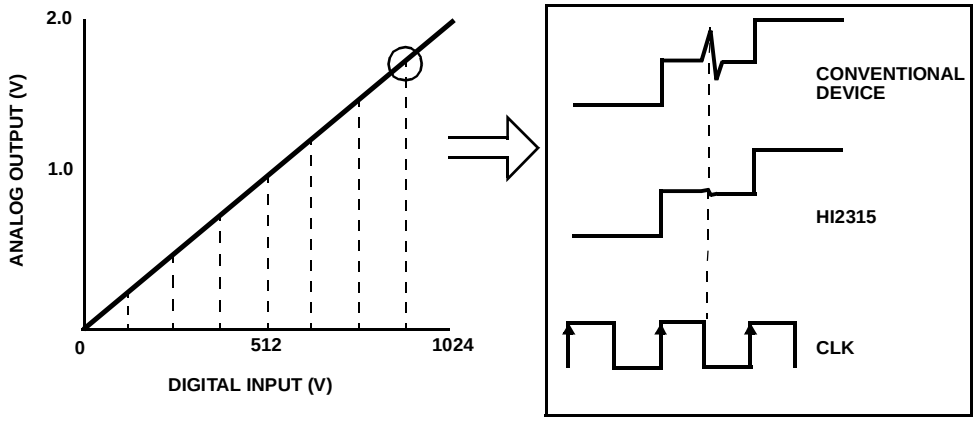


FIGURE 11. CHANGE OF GE FOR STAIRCASE WAVE OUTPUT

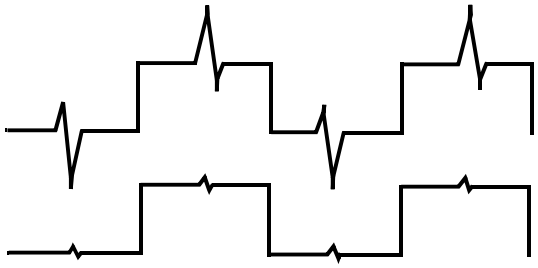


FIGURE 12. REPETITIVE OUTPUT WAVEFORM WHERE GE APPEARS (FOR 200Ω, $2V_{P-P}$ OUTPUT)

Notes On Operation

- Selecting the Output Resistance
  - HI2315 is a current output type D/A converter. To create the output voltage, connect the resistor to the current output pin.

    Specifications:
    Output full-scale voltage V_{FS} (Max) = 2.0V
    Output full-scale current I_{FS} (Max) = 10mA
  - Calculate the output resistance from $V_{FS} = I_{FS} \times R$. Connect a resistance sixteen times the output resistance to the reference current pin I_{REF}. In some cases, as this value may not exist, a similar value can be used instead.

    Note that the V_{FS} will be the following:

    $V_{FS} = V_{REF} \times 16\ R/R'$.
  - R is the resistor to be connected to the IO and R' is the resistor to be connected to the I_{REF}. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the glitch energy and data settling time. Set the best values according to the purpose of use.
- Correlation between Data and Clock
  - For the HI2315 to display the desired performance as a D/A converter, the data transmitted form outside and the clock must be synchronized properly. Adjust the setup time (t_S) and hold time (t_H) as specified in "Electrical Characteristics."
- V_{DD}, V_{SS}
  - Separate the analog and digital signals around the device to reduce noise effects. By-pass the V_{DD} pin to each GND with a 0.1µF ceramics capacitor as near to the pin as possible for both the digital and analog signals.
- Latch up
  - The AV_{DD} and DV_{DD} pins must be able to share the same power supply of the board. This is prevent latch up caused by potential difference between the two pins when the power is turned on.
- I_{REF} pin
  - The I_{REF} pin is very sensitive to improve the AC characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.
- VG Pin
  - It is recommended to use a 1µF capacitor to improve the AC characteristics though the typical capacitance value externally connected to the VG pin is 0.1µF.
- S_{REF}
  - The S_{REF} is independent regulated current source. By connecting it to the V_{REF}, stable output amplitudes that do not depend on fluctuations in the power supply can be obtained.
  - In this case, as $V_{FS} = S_{REF} \times 16R/R'$, set the V_{FS} according to R'.
  - Do not use this pin as a reference power supply for other ICs because this is dedicated for the D/A converter.