OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT

HSP50307

October 2000

Burst QPSK Modulator

Features

- **256 KBPS Data Rate and 128 KBPS Baud Rate**
- **Burst QPSK Modulation**
- **Programmable Carrier Frequency from 8MHz to 15MHz With a Frequency Step Size of 32kHz**
- **α = 0.5 Root Raised Cosine (RRC) Filtering For Spectrum Shaping**
- **On-Board Synthesizer**
- **Programmable Output Level From 22 to 62dBmV in 1dB Steps**
- **Programmable Charge Pump Current Control**
- **62dBmV Differential Output Driver for 75Ω Cable**

Applications

- **Burst QPSK Modulator**
- **HSP50307EVAL1 Evaluation Board Is Available**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50307SC	0 to 70	28 Ld SOIC	M28.3

Description

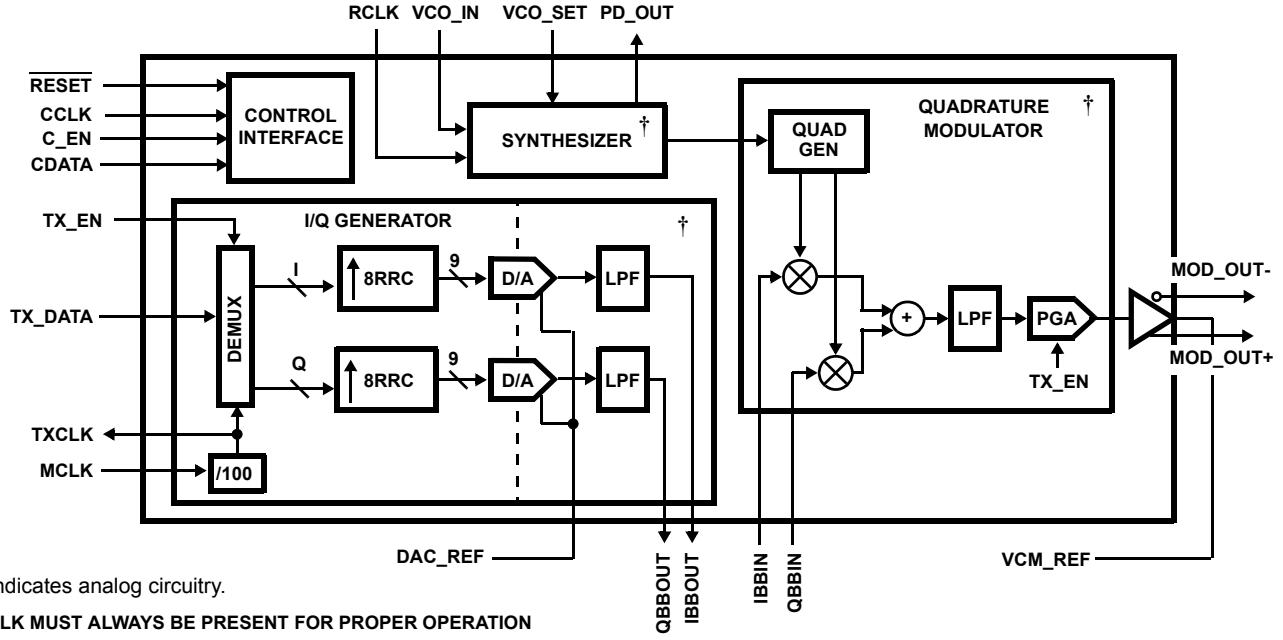
The HSP50307 is a mixed signal burst QPSK Modulator for upstream CATV Applications. The HSP50307 demultiplexes and modulates a serial data stream onto an RF Carrier centered between 8 and 15MHz. The signal spectrum is shaped with α = 0.5 root raised cosine (RRC) digital filters. On-chip filtering limits spurs and harmonics to levels below -35dBc during transmissions. The output power level is adjustable over a 40dB range in 1dB steps. The maximum differential output level is +62dBmV into 75Ω. A transmitter inhibit function disables the RF output outside the burst interval. The differential output amplifier int7-erfaces to the cable via a transformer.

The Block Diagram of the HSP50307 QPSK Modulator is shown below. The HSP50307 consists of a digital control interface, an I/Q generator, a synthesizer, and a quadrature modulator.

The data clock is derived from the master clock. The HSP50307 demultiplexes the input data bits into in-phase (I) and quadrature (Q) data streams. The first bit and subsequent alternating bits of the burst are in-phase data. The two data streams are filtered, converted from digital to analog, and low pass filtered to produce the baseband I and Q analog signals.

The baseband signals are up-converted to RF in the Quadrature Modulation Section. The synthesizer provides the local oscillator (LO) for the quadrature modulator. The frequency is programmable via the control interface with a resolution of 32kHz. The output of the quadrature modulator is low pass filtered to remove harmonic distortion.

Block Diagram

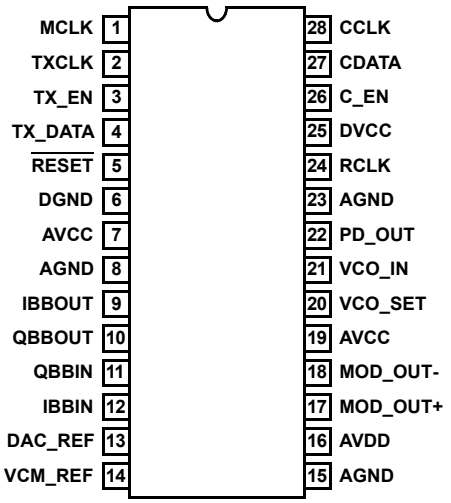


† Indicates analog circuitry.

MCLK MUST ALWAYS BE PRESENT FOR PROPER OPERATION

Pinout

28 LEAD SOIC
TOP VIEW



Pin Description

SYMBOL	TYPE	DESCRIPTION
MCLK	I	Master clock input (25.6MHz). (D)
TXCLK	O	PSK data clock (256kHz) for PSK_DATA_IN. (D)
TX_EN	I	Transmit Enable. When high, the modulator output is enabled. This pin should be high for the entire burst. The signal is extended internally until data has fully exited the part before turning off for spurious free turn on and turn off. (D)
TX_DATA	I	256 KBPS serial data input. (D)
$\overline{\text{RESET}}$	I	Digital Reset Pin (active low). The part is reset immediately on assertion of the reset pin. The output of the part is disabled on the assertion of reset. The part will come out of reset 2 master clock periods after the reset is de-asserted. Reprogramming (see Control Interface Section) is needed after deassertion of reset for proper operation. (D)
DGND	I	Negative supply for the digital filters and control. (P)
AVCC	I	Positive supply for the quadrature modulator. AVCC should be tied to +5V analog. (P)
AGND	I	Negative supply for the quadrature modulator. AGND is tied to GND. (P)
IBBOUT	O	I baseband filtered output. (A)
QBBOUT	O	Q baseband filtered output. (A)
QBBIN	I	Q baseband modulator input. (A)
IBBIN	I	I baseband modulator input. (A)
DAC_REF	O	D/A reference node. A 0.1µF capacitor to ground is suggested. (A)
VCM_REF	O	Modulator common mode reference node. A 0.1µF capacitor to ground is suggested. (A)
AGND	I	Negative supply for the cable interface. (P)
AVDD	I	Positive supply for the cable interface (+9V analog). (P)
MOD_OUT+	O	Positive output drive pin for the cable interface. (A)
MOD_OUT-	O	Negative output drive pin for the cable interface. (A)

Pin Description (Continued)

SYMBOL	TYPE	DESCRIPTION
AVCC	I	Positive supply for the synthesizer (+5V analog). (P)
VCO_SET	I/O	VCO free running frequency set resistor (normally 6.25kΩ). (D)
VCO_IN	I	Voltage-controlled oscillator control voltage. (D)
PD_OUT	O	Phase/frequency detector output. (D)
AGND	I	Negative supply for the synthesizer. (P)
RCLK	I	Synthesizer reference clock input (2.048MHz). (D)
DVCC	I	Positive supply for the digital filters and control (+5V digital). (P)
C_EN	I	Control interface enable for 3 wire interface. See Control Interface Section. (D)
CDATA	I	Serial data input for 3 wire interface. See Control Interface Section. (D)
CCLK	I	3 wire interface clock. See Control Interface Section. (D)

NOTE: (A) = analog, (D) = digital, (P) = power.

Functional Description

The HSP50307 is designed to transmit 256 KBPS data using QPSK modulation on a programmable carrier over 75Ω cable lines. The incoming 256 KBPS data is first demultiplexed into in-phase (I) and quadrature (Q) data streams. The burst QPSK modulator shapes the two 128 KBPS demultiplexed data streams using interpolate-by-8 root-raised cosine (RRC) filters with α = 0.5. The resulting 1.024MHz data streams are sent through D/A converters and are then sent through low-pass reconstruction filters for over 40dB image rejection. The baseband analog output and input pins allow the signals to be AC coupled. The returning analog signal is upconverted by an analog quadrature modulator. The control section is configured by loading 23 bits of information via a three-wire interface. These bits configure the DSP filter section, the carrier frequency, the analog synthesizer, and the output driver sections.

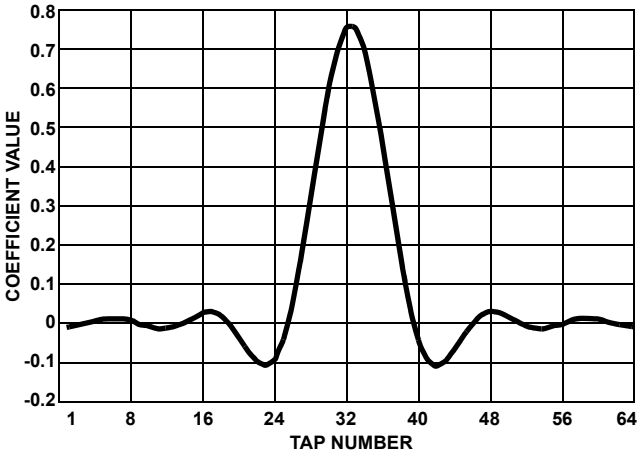


FIGURE 1. NORMALIZED IMPULSE RESPONSE OF THE RRC INTERPOLATION FILTER WITH α = 0.5

Digital Filters

The burst QPSK modulator uses an interpolate-by-8 digital RRC filter on both the I and Q data streams. The shaping factor is set to α = 0.5. The FIR order of the digital RRC filter is 64. Figure 1 shows the impulse response of the RRC filter.

Figure 2 is a spectrum analyzer plot of the modulator output for a baud rate of 128 kbaud and a pseudorandom data pattern. The 128kHz 3dB bandwidth and 192kHz stopband edges are readily apparent.

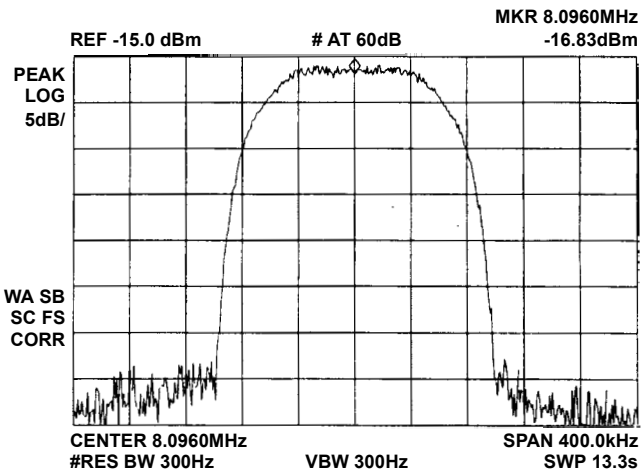


FIGURE 2. SPECTRUM OF 8.096MHz RANDOM DATA MODULATED CARRIER

Control Interface

The QPSK modulator is configured via a serial three wire interface. When C_EN is high, 23 bits are shifted in at the CDATA pin on the falling edge of CCLK. Figure 3 shows the timing diagram for loading the serial configuration data. Table 1 describes the 23-bit serial configuration data. See the Synthesizer Section for more details on the frequency control bits.

TABLE 1. 23-BIT SERIAL DATA CONTROL INTERFACE DESCRIPTION

BIT POSITION	FUNCTION	DESCRIPTION
D0-D2 (Note)	Synthesizer Control Bits	Pre-scaler control register. A = (0 to 5), D2 is the MSB.
D3-D9	Synthesizer Control Bits	Feedback Counter Control Register. M = (41 to 103) D9 is the MSB.
D10	Synthesizer Enable	Active high. This bit activates chip bias networks for normal operation. D10 = 0 places part in low power mode.
D11	Charge Pump Current Control	D11 = 0 sets charge pump current to 500µA. D11 = 1 sets charge pump current to 1mA.
D12	Three-State Control	D12 = 0 three-states the charge pump output when a pump up and down command occur simultaneously. D12 = 1 disables three-state.
D13-D18	Attenuation Control	Controls output power level. The binary value of the register corresponds to an attenuation amount. For example, 000100 corresponds to 4dB attenuation from the maximum 62dBmV level. D18 is the MSB.
D19-D21	Reserved	Used for test/diagnostic purposes. Set to 000.
D22	DSP Shut Down	Test mode; D22 = 0 sets the burst QPSK modulator in normal mode. D22 = 1 disables the digital filter.

NOTE: D0 is the first bit shifted into the part.

Synthesizer

The synthesizer generates the quadrature LO's for modulating the baseband data to RF. The carrier frequency is phase locked to the reference clock (RCLK). The carrier frequency, F_C, has a frequency range of 8MHz to 15MHz with a resolution of 32kHz. Equation 1 gives the relationship between F_C and the frequency of RCLK and the frequency control bits, M and A.

$$F_C = \frac{6(M+1)+A}{64} F_{REF}, \quad \text{(EQ. 1)}$$

where F_{REF} equals the frequency of RCLK. Also, M and A can be determined by

$$M + \frac{A}{6} = \left[\frac{64}{6}\right]\left[\frac{F_C}{F_{REF}}\right] - 1. \quad \text{(EQ. 2)}$$

"A" ranges from 0 to 5 and "M" ranges from 41 to 103. A and M are programmed via control bits D0-D2 and D3-D9, respectively. Values outside these ranges are invalid.

I/Q Generator

The I/Q Generator Section demultiplexes and time aligns the 256 KBPS input data into two data streams, I and Q. The first data bit following the assertion of the TX_EN signal is the I data of the first I/Q pair. Each I/Q pair determines the phase angle of the QPSK transmission signal. The relationship between I/Q pairs and phase angles is shown in Table 2. Since the QPSK encoding requires a pair of I and Q information to transmit one symbol, an even number of data bits must be provided for each burst.

TABLE 2. QPSK ENCODING

I	Q	PHASE
0	0	45^o
0	1	135^o
1	0	-45^o
1	1	-135^o

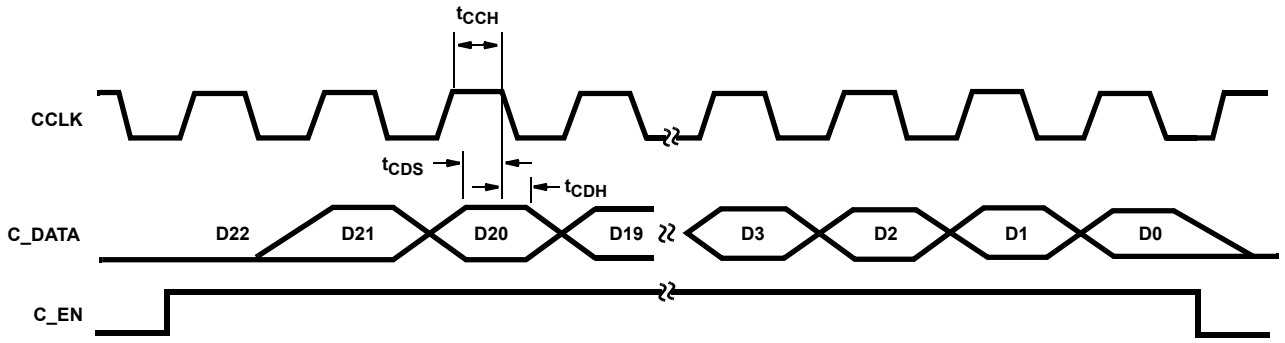


FIGURE 3. CONTROL INTERFACE TIMING DIAGRAM

Applications Example

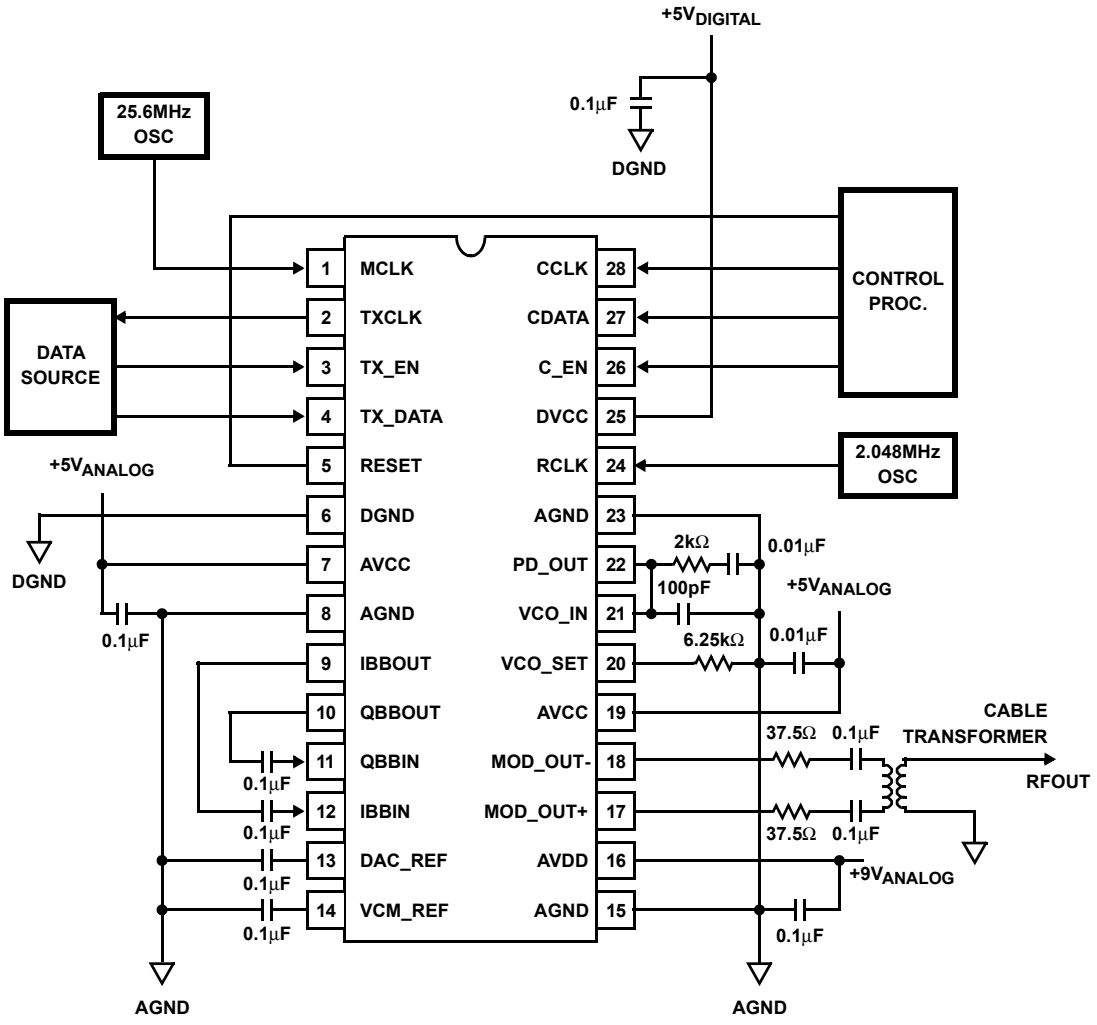


FIGURE 4. APPLICATIONS EXAMPLE OF THE HSP50307

Figure 4 shows an applications example of the HSP50307. The MCLK source operates at 25.6MHz, and the RCLK operates at 2.048MHz. 0.1µF capacitors are connected from the IBBOUT to IBBIN and the QBBOUT to QBBIN, providing AC coupling to the Analog Upconverter Section of the HSP50307.

The control processor sends the 23-bit control word via the three-wire interface. The data source receives the 256kHz TXCLK from the HSP50307 and transmits data and enable signal at the 256kHz rate.

The DAC_REF and VCM_REF are connected to 0.1µF capacitors to ground. Each of the differential drivers are loaded with a 37.5Ω resistor and a 0.1µF capacitor. The 37.5Ω resistors provide matching to the 75Ω cable. The capacitors perform AC coupling. The drive paths are sent to the cable transformer for data transmissions.

Table 3 shows the general functional specifications for the applications example shown in Figure 4. It gives an overview of what is being accomplished but does not specify an exact carrier frequency or other programmable functions. These specifications are met given a valid control word combination and the applications circuit shown in Figure 4. Table 4 summarizes the performance of the applications example shown in Figure 4. Again, these specifications are met given a valid programmed mode.

NOTE: The HSP50307 is sensitive to layout. Users must make sure the input signals do not couple back into the output signals. The performance of the HSP50307 is also sensitive to the decoupling capacitors between 1) QBBOUT and QBBIN and 2) IBBOUT and IBBIN. The values shown in Figure 4 are recommended.

TABLE 3. GENERAL FUNCTIONAL SPECIFICATIONS

AVCC, DVCC = +5V, AVDD = +9V; RCLK = 2.048MHz; MCLK = 25.6MHz; $T_A = 0^oC$ to 70^oC

PARAMETER	MIN	TYP	MAX	UNIT
QPSK Carrier Frequency	8.0	-	15 (Note)	MHz
QPSK Carrier Frequency Step Size	-	32	-	kHz
Modulation Bandwidth	-	192	-	kHz
Raised Cosine Filter Response Excess Bandwidth (α)	-	0.5	-	-
Transmit Level Adjust	-	40	-	dB
Data Rate	-	256	-	KBPS
Baud Rate	-	128	-	KBPS

NOTE: May operate up to 20MHz.

TABLE 4. QPSK PERFORMANCE SPECIFICATIONS

AVCC, DVCC = +5V, AVDD = +9V; RCLK = 2.048MHz; MCLK = 25.6MHz; $T_A = 0^oC$ to 70^oC

PARAMETER	MIN	TYP	MAX	UNITS
Output Spurious Signals Less Than 54MHz	-	-40	-35	dBc
Output Spurious Signals Greater Than 54MHz	-	-60	-50	dBc
Off Mode Spurs	-	-	-30	dBmV
Transmit Level (D18-D13 = 000000)	59	62	65	dBmV
Output Gain Adjust Relative Accuracy	-0.5	0.2	0.5	dB
Absolute Output Accuracy at Any Step	-3.0	$\pm$2	3.0	dB
QPSK Carrier Phase Noise at 10kHz Offset	-	-	-75	dBc/Hz
QPSK Carrier Phase Noise at 1kHz Offset	-	-	-60	dBc/Hz
QPSK Modulator Carrier Suppression	35	40	-	dBc
QPSK I/Q Amplitude Imbalance	-	-	0.5	dB
QPSK I/Q Phase Imbalance	-	-	2.0	Degree
QPSK Passband Amplitude Ripple	-0.3	-	0.3	dB

Absolute Maximum Ratings

5V Supply Voltage 6.0V
9V Supply Voltage 11.0V
ESD Classification . . . . . Class 1, HBM

Operating Conditions

Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70
Maximum Junction Temperature	150^oC
Maximum Storage Temperature Range	-65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

RCLK = 2.048MHz; MCLK = 25.6MHz; $T_A = 0^oC$ to 70^oC

PARAMETER	SYMBOL/PIN	MIN	TYP	MAX	UNIT
5V Supply Voltage	AVCC, DVCC	4.75	5.0	5.25	V
9V Supply Voltage	AVDD	8.55	9.0	9.45	V
5V Supply Current	I_{AVCC}, I_{DVCC}	-	55	-	mA_{DC}
9V Supply Current	I_{AVDD}	-	60	-	mA_{DC}
Logical One Input Voltage	V_{IH}	3.325	-	-	V
Logical Zero Input Voltage	V_{IL}	-	-	1.575	V
Output High Voltage	V_{OH}	2.6	-	-	V
Output Low Voltage	V_{OL}	-	-	0.4	V

AC Electrical Specifications

AVCC, DVCC = +5V, AVDD = +9V; RCLK = 2.048MHz; MCLK = 25.6MHz; $T_A = 0^oC$ to 70^oC

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESET Pulse Width	t_{RES}	500	-	-	ns
MCLK Period (25.6MHz)	t_{MCP}	-	39.1	-	ns
RCLK Period (2.048MHz)	t_{RCP}	-	488	-	ns
RCLK High	t_{RCH}	98	-	-	ns
RCLK Low	t_{RCL}	98	-	-	ns
CCLK Period (5MHz)	t_{CCP}	200	-	-	ns
CCLK High	t_{CCH}	150	-	-	ns
CCLK Low	t_{CCL}	150	-	-	ns
CDATA Setup to CCLK	t_{CDS}	50	-	-	ns
CDATA Hold from CCLK	t_{CDH}	-	-	50	ns
C_EN Strobe Edge to CCLK	t_{CES}	-100	-	100	ns
TXCLK Period (256kHz)	t_{DCP}	-	3910	-	ns
TXCLK High	t_{DCH}	195	-	-	ns
TXCLK Low	t_{DCL}	195	-	-	ns
TX_DATA Setup to TXCLK	t_{DIS}	150	-	-	ns
TX_DATA Hold from TXCLK	t_{DIH}	0	-	-	ns

Waveforms

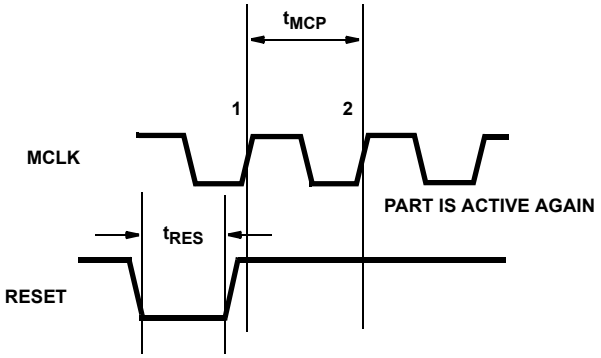


FIGURE 5. RESET AND MCLK WAVEFORMS

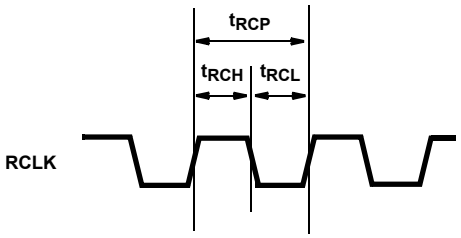


FIGURE 6. RCLK WAVEFORM

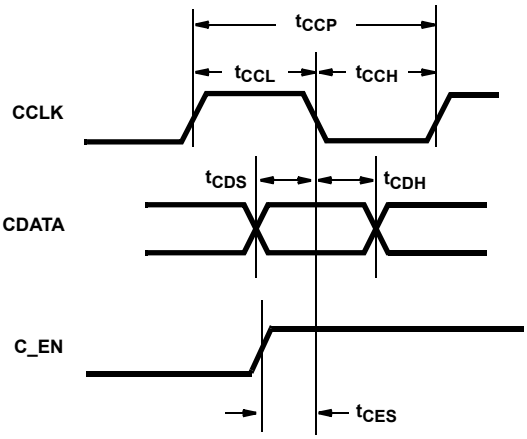


FIGURE 7. CONFIGURATION WAVEFORMS

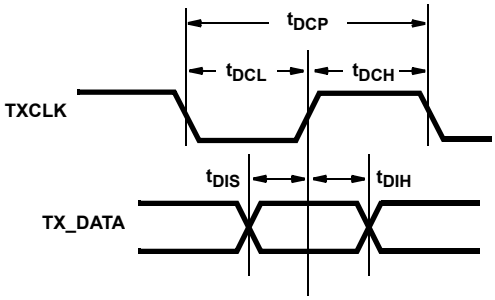


FIGURE 8. TRANSMIT DATA WAVEFORMS