INITIAL RELEASE

Inrush Limiter/Circuit Breaker/Hotswap Controller IC

(No External Parts Required)

Features

- ❑ No External Parts Required
- ❑ On Board 80V, 2A MOSFET
- ❑ No Rsense Needed
- ❑ ±8.0V to ±80V Input Voltage Range
- ❑ Two Level Current Limiting
  - ❍ 1.2A Initial Inrush Limit
  - ❍ 2.0A Second Inrush Limit/Circuit Breaker Triggers Servo Limit to 1.2A for T_{oc}
- ❑ Fast Response Current Limit when Over Current or Step Voltage at Input Supply (eg. Diode 'OR'ing)
- ❑ UVLO/ENABLE & POR Supervisory Circuits
- ❑ Programmable UVLO
- ❑ Over Current Protection
- ❑ 9.0sec Auto Retry
- ❑ Built in Thermal Shutdown with Hysteresis
- ❑ 80V Open Drain PWRGD Flag
- ❑ Thermally Rugged DPAK5 Package

Applications

- ❑ Power Ethernet Systems
- ❑ Routers, Switches
- ❑ Chargers
- ❑ Security Peripherals & Cameras
- ❑ Automotive Protection
- ❑ Negative Supply Rail Breaking Applications
- ❑ Networking Line Cards
- ❑ Telecom Line Cards

Description

The HV111 is a complete power management solution for switched or pluggable backplane applications up to 1.65A, running from –8.0 to -80V*, requiring no external components or programming in many applications.

An internally programmed supervisor UVLO/ ENABLE may be overridden with external resistors for custom settings. Satisfying this supervisor will begin a POR phase to ensure de-bouncing. Thereafter, a servo loop controls an internal 80V, 2A pass element to limit current. The circuit uses internal mirrors to measure current eliminating the need for a sense resistor.

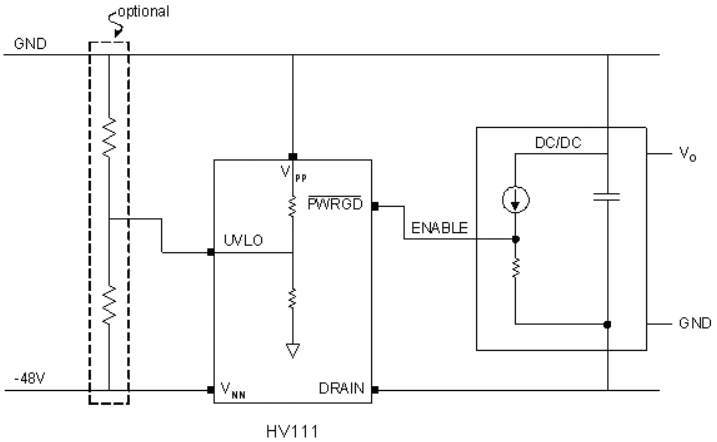
The HV111 includes two current modes: i) initial current limit mode limits the current to 1.2A during turn on; ii) thereafter a 2A monitor circuit will re-trigger the servo mechanism back to 1.2A limit if it is tripped. An on-board thermal supervisor ensures that the device can never be damaged by over current conditions.

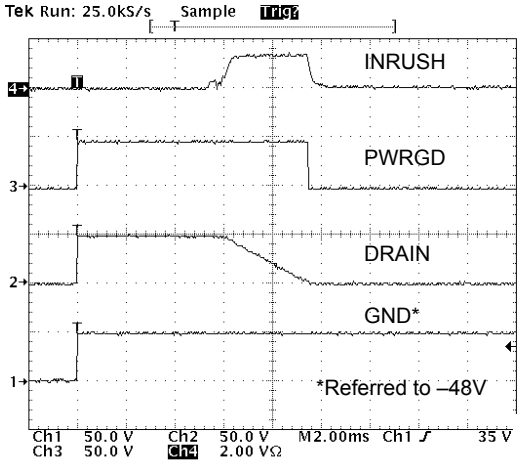
Circuit breaker functionality is obtained through a either a current limit timeout or a PWM current limiter for severe faults. If the servo limits for more than 75ms then the part will shut down the pass element, and initiate a 9sec timer after which the turn on sequence will restart.

The HV111 is available in a thermally rugged DPAK-5 package which provides improved thermal resist-ance when compared to SO-8 based solutions.

***The HV111 may also be used in +6.5 to +80V systems.**

Typical Schematic and Waveforms





Ordering Information

DEVICE	Package Options
	DPAK-5
HV111	HV111K4

Absolute Maximum Ratings

Supply Voltage*, V_{pp}	-0.5V to 90V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65° to +150°C
5 Pin DPAK Thermal Resistance $R_{\phi JA}$	80°C/W
5 Pin DPAK Thermal Resistance $R_{\phi JC}$	11°C/W

*Relative to V_{NN}

Electrical Characteristics (* means -20°C< T_A < +85°C)

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{IN}	Supply Voltage	-80		-8.0	V	*	
I_{IN}	Supply Current			1	mA		V_{PP} = -48V, Standby Mode
V_{UVLO}	Internal UVLO Threshold (High to Low ie. Turning Off)	-23.5	-26.0	-28.5	V	*	Subtract V_{HYS} for Low-to-High
V_{HYS}	Internal UVLO Hysteresis HV110	1.5	2.5	3.5	V	*	
V_{UV}	UVLO Comparator Threshold	1.10	1.20	1.30	V	*	Referenced to VNN
V_{UVHYS}		60	100	140	mV	*	
R_{UVLO}	UVLO Input Resistance (2.5M || 116k)	90	120	150	kΩ		
R_{DS}	MOSFET On Resistance		1	1.5	Ω	*	
I_{LEAK}	Output Leakage Current			10	uA	*	MOSFET is off
I_{INRUSH}	Inrush Current Limit HV111	1.15	1.40	1.65	A	*	
I_{CB}	Circuit Breaker Trip Current	1.65	2.00	2.35		*	Trips then limits to I_{LIMIT} until toc expires.
I_{LIMIT}	Over Load Current Limiting		1.2		A	*	
I_{SC}	Shorted Circuit PWM Average Current		230		mA		V_{PP}-V_{DS} < ~1V
VOL_{PWRGD}	PWRGD Output Low Voltage			0.4	V		I=1mA; Reference to VNN
IOH_{PWRGD}	PWRGD Output leakage Current			10	uA	*	V=5V; Reference to VNN
t_{SC}	Shorted-Circuit Timer (1) (4)	40	75	110	ms	*	
t_{OC}	Over-Current Timer (2) (4)	40	75	110	ms	*	
t_{LIMIT}	Current Limit Delay Time (3)		10		us	*	Limits within 10us. May take up to 100us to reach final level.
t_{POR}	POR Timer	2.5	4.5	6.5	ms	*	
$t_{RESTART}$	Restart Timer (4)		9		Sec	*	
T_{OVER}	Temperature False	120	135	150	°C	*	Low to High
T_{RESET}	Temperature Reset	70		100	°C	*	High to Low

(1) Shorted-circuit timer starts after POR timer. If V_{DRAIN} does not drop at least 3/4 Vin before t_{SC} then a shorted-circuit condition exists.
(2) If the output current is in an overload condition then the output immediately goes to current limit and starts the over-current timer. If I_{OUT} does not drop back below I_{LIMIT} before the timer expires then an over current condition exists. The timer is immediately reset when a fault is cleared.
(3) Time for fast return to limit circuit to react.
(4) Guaranteed by design.

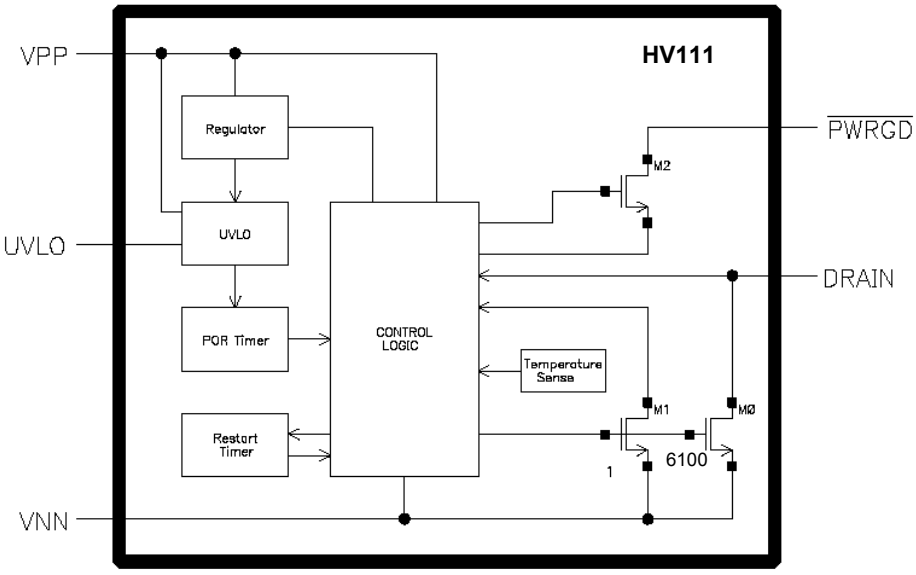


Figure 1 – Internal Blocks of HV111

Pin Description

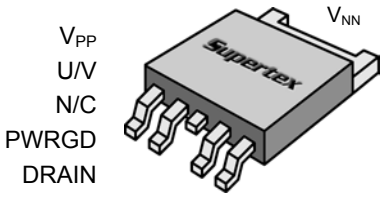
V_{PP} – Positive voltage supply input.

V_{NN} – Negative voltage power supply input.

DRAIN – Internal N-Channel MOSFET drain output.

UV/ENABLE - Under Voltage Lockout Input or Enable

PWRGD - Active Low Power Good Output



Functional Description

Many systems include front end capacitance to provide low impedance energy and filtering to power systems. These systems include hot pluggable live-backplane systems, such as –48V telecom systems and switched systems such as battery connected backed-up loads.

This filter capacitance, usually implemented as large electrolytic capacitors, looks like a low impedance connected directly across the power supply terminals and causes high inrush currents which could damage connectors, traces or components (such as the capacitors themselves). These high currents may also cause localized glitching of the backplane or EMI that could reset or interrupt surrounding circuit cards.

The HV111 is a single chip solution that provides bullet-proof power management control for systems with loads less than 1.65A. The HV111 does not require the use of any external components or programming and eliminates the need for a sense resistor. Where desired, however, internal set points may be overridden with external components – for example an external resistor divider may be used to set the UVLO/ENABLE threshold.

High Voltage Regulator

The HV111 includes a high voltage regulator capable of operation with V_{PP}-V_{NN}=6.5V to 90V. The regulator provides an internal voltage to operate circuitry and drive the internal 1Ω MOSFET pass element.

Turn on Protection
(UVLO/POR for Debounce + PWM limit)

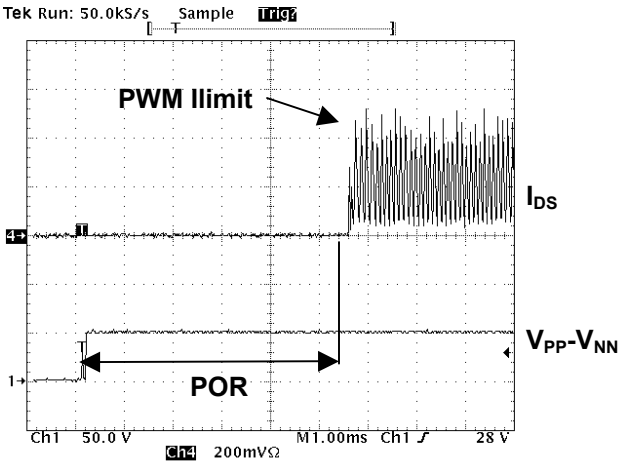


Figure 2 – UVLO & POR + Dead Short Protection

The second subsystem is the UVLO/POR that work together to debounce. Leave the UVLO input open to use the default setting of –26V with 2.5V hysteresis. This default setting can be over driven with an external resistive divider. The comparator threshold is 1.2V with respect to V_{NN}. The HV111 is capable of operation down to 8.0V for automotive applications to 80V for the most rugged telecom applications.

The third subsystem, PWM limit, is protection for turning on into a short (or a later dead short). In this case the HV111 helps avoid the dumping of large currents into the load by pulse width modulating (PWM) the current to limit Inrush current to <250mA average if V_{pp}-V_{DRAIN}<~1V.

Programming UVLO

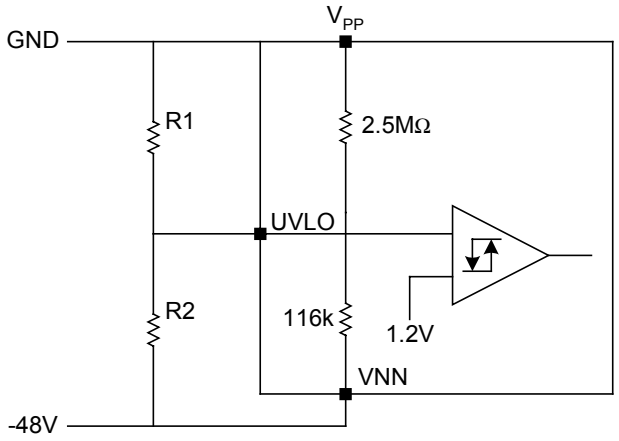


Figure 3 – Programming UVLO

The UVLO/ENABLE pin makes it easy to override the internal 26V nominal under voltage. The 26V nominal setting is produced by a resistor divider of 2.5MΩ and 116k. These are 20% resistors, however, 1% accurate relative to one another. To override there are two options. The first is to simply use a much lower impedance divider, for example 200k, and largely ignore the internal divider. Alternatively, the internal impedance may be taken into a account in the network and the UVLO calculated as:

VPP*(R2||116k) / (R1||2.5MΩ+R2||116k)

Keep in mind, however, that the 20% variation on the internal resistors will reduce the accuracy of the UVLO set point using this approach.

Note that the UVLO/ENABLE pin may also be used as an enable with a nominal 1.20V trip point and 10% of hysteresis.

PWRGD Active High or Active Low (for DC/DC HV Interface / Enable)

The PWRGD pin is an open drain active low MOSFET which is enabled when the gate voltage on the internal power MOSFET reaches its full on voltage. The PWRGD is nominally ACTIVE LOW, however, the simple circuit shown below can convert it to active high operation.

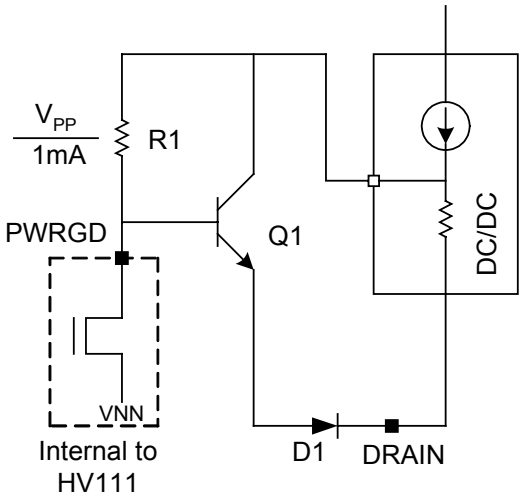


Figure 4 – PWRGD Active High

The above circuit works as follows for ACTIVE HIGH operation. If the PWRGD is low, then the current sourced by the DC/DC pullup is pulled to V_{NN} and the BJT, Q1, is starved for base drive current and remains off. The reverse Vbe voltage is protected by the series diode, D1. If PWRGD is open, then the current has no alternative but to flow into the base and thus connects the DC/DC ENABLE pin to the DC/DC ground reference (DRAIN pin of the HV111). As the clamp is inverting, therefore proper ACTIVE high polarity is established.

The resistor, R1, should be sized as V_{PP}/1mA to ensure that the maximum PWRGD transistor current is not exceeded (remember to use the maximum possible V_{PP} your circuit will see rather than the nominal value of V_{PP}). Further, Q1 must be rated for operation to maximum expected V_{PP} and have a beta large enough that the minimum VPPmin/VPPmax*1mA*β_{min} > Ipullupmax of the DC/DC converter (or external resistor if used).

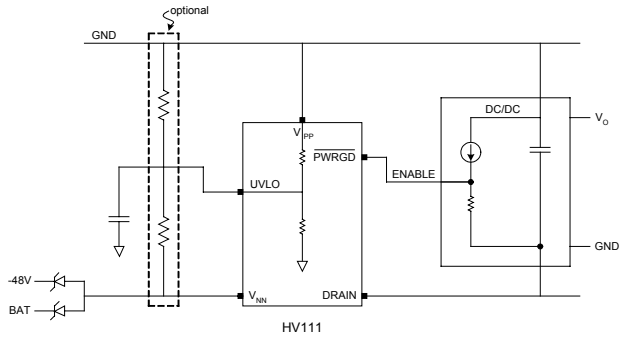


Figure 5 – PWRGD Enable

Also shown in the above figure is a capacitor connected to UVLO/ENABLE. Although this decoupling capacitor is not strictly required, a fast dv/dt on PWRGD can result in coupling that can glitch the UVLO pin. This decoupling capacitor ensures that glitches will be eliminated.

Thermal Shutdown

In addition to the above parameters, the HV111 will shutdown if the temperature on the die reaches ~135°C and it will not restart until the temperature drops to 100°C or less (could be significantly less). The thermal sensor is key in providing a bullet proof power management solution because it ensures that the device will turn off long before damage can occur. This is a significant advantage over solutions that do not contain an integral FET as then the temperature cannot be easily sensed quickly and accurately.

Thermal engineering using the HV111 is key to proper system operation. The 1Ω MOSFET pass element may reach a value as high as 1.5Ω at high temperatures. There are numerous methods to reduce the thermal resistance of the $R_{\phi JA}$. The following table describes some options:

Method	$R_{\phi JA}$	Description
FR4	70-80˚C/W	Straight Convection
FR4 Heat Sink	40˚C/W	10cm^2 PCB H/S
FR4+H/S	13˚C/W	External Sink+Holes
IMS (40cm^2)	9˚C/W	Floating in Air
IMS* w/H/S	4.5˚C/W	External Heatsink

*IMS is a metal substrate board

To determine your required thermal impedance, $R_{\phi JA}$, is quite simple. In a parallel to Ohms law, Power x $R_{\phi JA}$ = ΔT. Junction temperature, which is limited to 120˚C minimum, is Tmaxambient + ΔT. For example, if the highest operating ambient temperature were 55˚C as with many networking applications, and the power were 1.6A, then the required thermal resistance would be calculated as follows:

1. Determine maximum ambient = 55˚C.
2. Determine max junction temp. = 120˚C[1].
3. Determine max operating current = 1.6A.
4. Therefore ΔT = 120-55˚C = 65˚C.
5. Max. Power[2] = 1.6A^2*1.5=3.84W.
6. Now ΔT / Power = $R_{\phi JA}$ = 65/3.84 = 20˚C/W.
7. To achieve a $R_{\phi JA}$ of 20˚C/W the table above shows that it will be necessary to use a DPAK external heatsink or IMS substrate.

[1]This is the minimum value of the low to high thermal shutdown according to the electrical specifications on pg. 2.
[2]This is the maximum MOSFET on resistance at high temperature.

Note that in the case of a large input capacitance that the thermal calculations may be dominated by the I*Vds thermal dissipation of the FET as it is modulated to limit current. In this case the instantaneous power dissipation is much higher than in the case above. For more information on calculating the thermal requirements in this case please call your local Supertex field applications engineer.

Auto-Retry

Any fault condition will cause an automatic 9sec automatic retry to occur. This retry will occur indefinitely (as long as the thermal supervisor is satisfied). Figure 3 shows typical waveforms for the auto-retry.

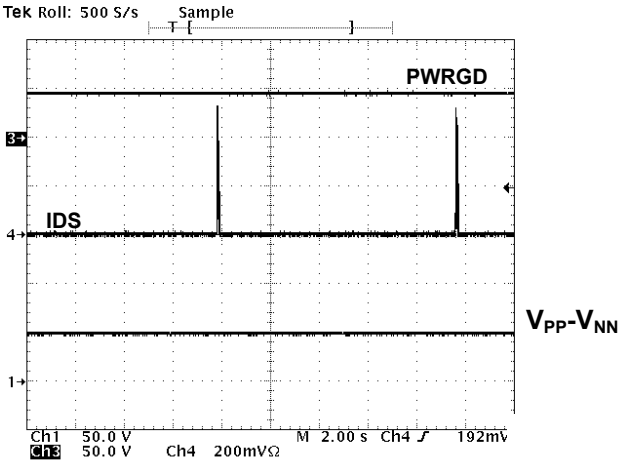


Figure 6 – Auto-Retry

Timers

The timer subsystems are critical to successful operation of the HV111. Timers are as follows:

Timer	Duration	Units
Power-on-Reset[1]	4.5	ms
Initial Inrush Timeout[2]	75	ms
Shorted Inrush PWM	10	µs
Shorted Circuit Timer	75	ms
Second Inrush (Diode 'OR'ing):		
❒ Return to Limit	10 (100[3])	µs
❒ Timeout	75	ms
Auto-Retry	9	S

[1]This is the time from satisfying the undervoltage comparator. Each "bounce" will reset this timer & therefore observed delay may be higher than this "ideal" delay.
[2]This timer is unique because it looks to ensure that the drain drops at least ¼ of input voltage (to make sure there is no fault) within a t_{sc}=75ms period.
[3]Limit within 10us, but may take up to 100us to settle.

Current Sensing – No Rsense Required

The HV111 uses an internal 6000:1 current mirror to eliminate the need for a sense resistor. This saves energy and eliminates the need for a power component. The current mirror used by Supertex is unique in that it utilizes special circuitry to normalize for the variations in Vds between the primary pass element and the internal element which would otherwise cause current mismatch – and forces competitors to use internal sense resistors in similar applications. This algorithm also provides the shorted circuit PWM functionality which can help protect systems in the case of severe short circuits.

Fast Clamp

Any MOSFET includes parasitic capacitances Ciss and Cfb. Until power is available and the HV111 initializes, these parasitic capacitances form a capacitor divider which will apply to the gate the ratio of Cfb/(Ciss+Cfb)*Vin until the chip is initialized. To combat this the HV111 includes a fast acting clamp which will hold off the pass

element if it sees voltage applied on the gate of the internal pass element even before the HV111 has initialized.

PWM Current Limit (PWM Ilimit)

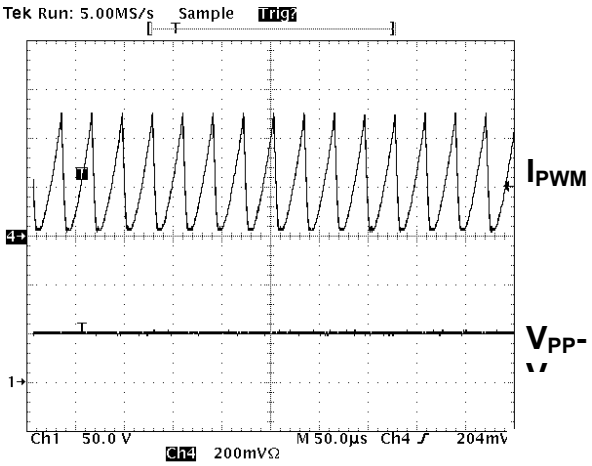


Figure 7 – Shorted PWM Ilimit

The HV111 includes a unique protection mode not found in other hotswap controllers. This protection mode is directed towards severe faults – faults in which the DRAIN voltage is unable to move more than ~1V from V_{PP}.

If such a shorted condition exists then the current will be limited as shown in Figure 7 above (where the upper waveform is the ~230mA PWM current & the lower waveform is the input voltage). Reducing the current under severe shorts overcomes thermal cycling in which the HV111 turns on and off as it heats up and cools down in a severe fault (limiting the current successively to 1.2A until overheat). It also protects downstream systems by relieving them of the requirement to handle the 1.2A.

Although this protection is extremely helpful in the case of a severe fault condition, it does put a limit on the charging current available for non-enabled loads. If using a non-enabled load the load must be kept above 1V/230mA by an amount which will provide enough current to the system to charge the capacitor to through both the 1V and thereafter through the remaining maximum 1/4∆V with full inrush current.

For example, if the capacitor were a 100uF capacitor and the maximum V_{PP} were 57V, then one would determine the minimum non-enabled load as follows:

1. V_{PP}-1V = 56V.
2. Total time is 230mA, 1V charge time plus 1.2A, 56V charge time = –RC*ln(1-1/(230e-3*R))+C*13/1.2 < 40ms; where R is the non-enabled load resistance, C is the non-enabled load capacitance & the average PWM current is 230mA.

Time if the load were enabled:

I=C*dv/dt => dt=C*dv/Inrush; 100u*13/1.2+ 100u*1*230mA~1.083ms+0.023ms~1ms. For total time until end of inrush add 100u*43/1.2 = 3.583ms for a total of 4.69ms.

Description of Operation

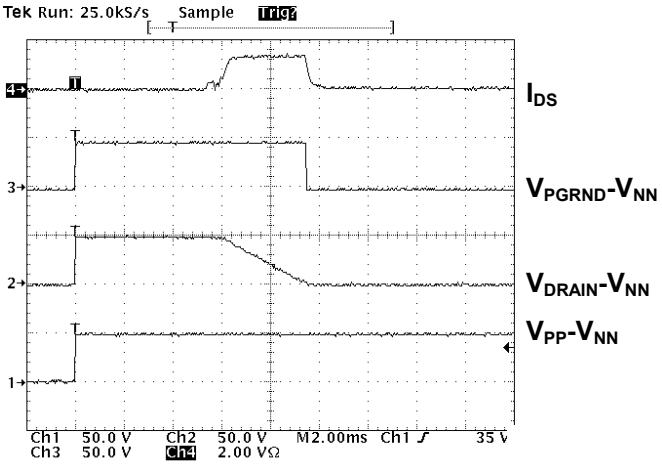


Figure 8 – Turn on Waveforms

Referring to the figure above, the operation of the HV111 may be illustrated. On initial power application (waveform 1 in Fig. 8) the HV111 provides a regulated supply for the internal circuitry. Until the proper internal voltage is achieved all circuits are held reset, the N-channel MOSFET is off and the PWRGD pin is open (INACTIVE). Once the internal regulator is safe to operate, the under voltage lock out (UVLO) senses the input voltage. The UVLO will hold the pass element off until it is satisfied. At any time during the start up cycle or thereafter, the input voltage falling below the UVLO threshold will turn off the N-channel MOSFET and reset all internal circuitry. The IC also includes a clamp for the spurious inrush through Cload and the Cfb of the MOSFET pass element. A normal restart sequence will be initiated once the input voltage rises above the UVLO threshold.

The UVLO supervisor works in conjunction with a power on reset (POR) timer. The timer is approximately 4.5ms to overcome contact bounce. During the contact bounce if input voltage falls below the UVLO threshold voltage then the POR timer will reset. In this way the card will be held off until bouncing ends. The POR timer will restart again when the input voltage rises above the UVLO threshold once again. After a full POR period is satisfied, the N-channel MOSFET begins to turn on to charge the output capacitor with a current source limited to ~1.2A (illustrated by Waveform 4 in Fig. 8). Note the PWM protection at the leading edge of the current rise in Waveform 4; this is the PWM protection limiting current because it cannot discern between a dead short and the time during which VPP-Vds<~1V. Waveform 2 shows the Vds or DRAIN pin.

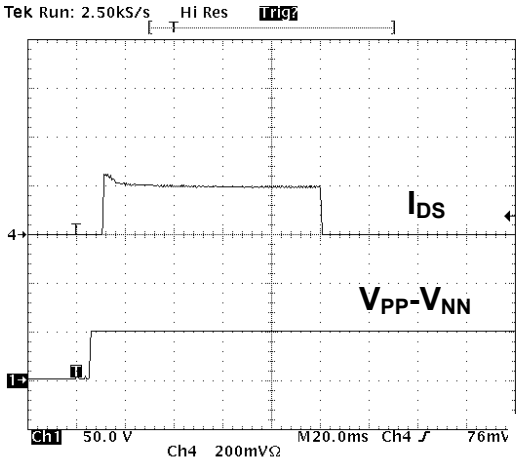


Figure 9 – Limit Timeout

Initial Inrush Timeout

The HV111 monitors the drain voltage and the output current. During hotswap if the drain does not drop below 1/4 of input voltage within a shorted-circuit timer period (tSC = 75ms), then the part will conclude that a short circuit condition exists, will turn off the internal FET and auto-retry with a period of 9.0sec. This case is illustrated in Fig. 9 above (where waveform 4 is DRAIN current and waveform 1 is VPP). Note that if the short circuit is low enough impedance to hold the DRAIN voltage within ~1V of VPP then the PWM current limit will engage as shown in Fig. 7. Further, the PWM current limit will remain until VPP- VDS >~1V.

After the hotswap period is finished successfully, the internal FET is turned fully on & the PWRGD is pulled low (ACTIVE). PWRGD operation (connected to a pullup) is illustrated by Waveform 3 in Fig. 8.

Circuit Breaker/Fast Return to Limit (Diode 'OR'ing)

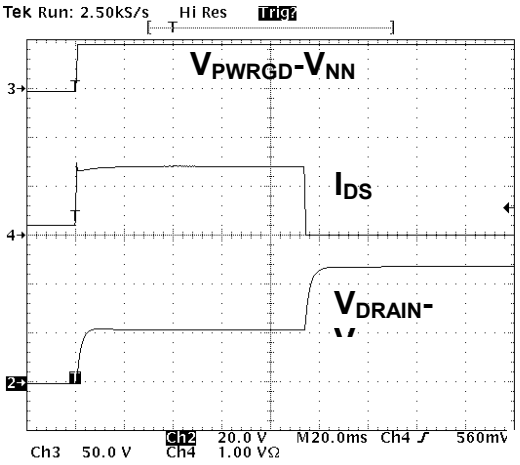


Figure 10 – Fast Return to Limit

A current monitor continually examines the current level (waveform 4 in Fig. 9 & 10) and if it exceeds 2A at any time, the FET changes to a fixed 1.2A current source. The FET will remain in this state until the expiration of an over-current timer (t_{OC} = 75ms), whereafter the FET gate will be turned off and auto-retry will begin (see DRAIN waveform 2 in Fig. 10, waveform 3 is V_{PP}). In the event that the over-current is cleared before the over-current timer has expired, then the over-current timer will be reset. The 2A breaker will react and begin to limit current in under 10us, however, it may take up to 100us for the system to stabilize at the limit level (1.2A).

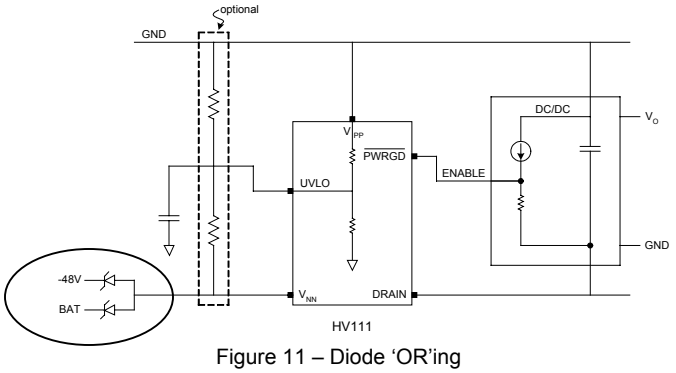
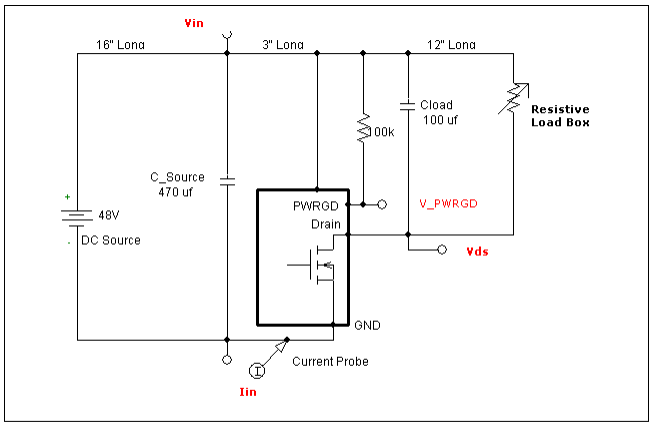


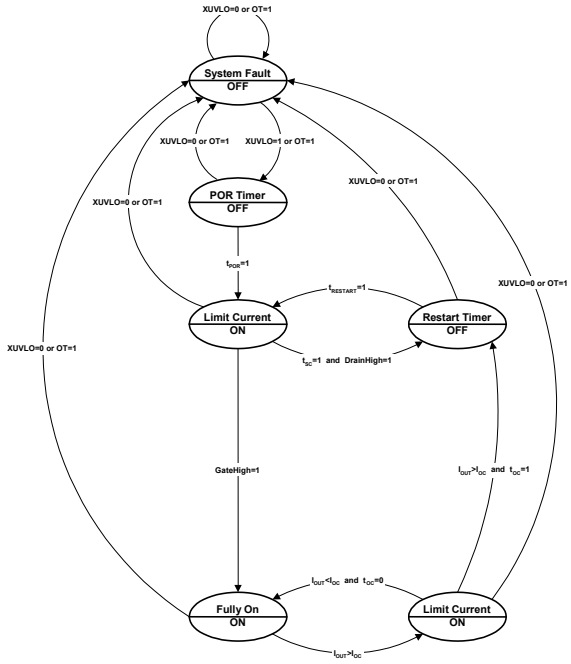
Figure 11 – Diode 'OR'ing

Fast return to limit also acts as a circuit breaker with delay, in that large currents will be limited and then the system shut down if it does not recover. Keep in mind, however, that severe faults which bring V_{DRAIN} within ~1V of V_{PP} will be limited with the PWM Ilimit function. Fast return to limit also overcomes the problem of "second inrush" or "diode 'OR'ing which is illustrated in Fig. 10 above. To understand this phenomenon, consider what happens when the system has been operating from the battery from a length of time. The battery voltage has dropped perhaps ten volts or more. Suddenly power is restored and the voltage suddenly jumps from the battery voltage to the fully regulated input voltage. This voltage jump puts a dv/dt upon the filter capacitances that creates a second inrush. This second inrush can cause damage if not limited, which is the purpose of the second inrush fast return to limit.

Test Setup



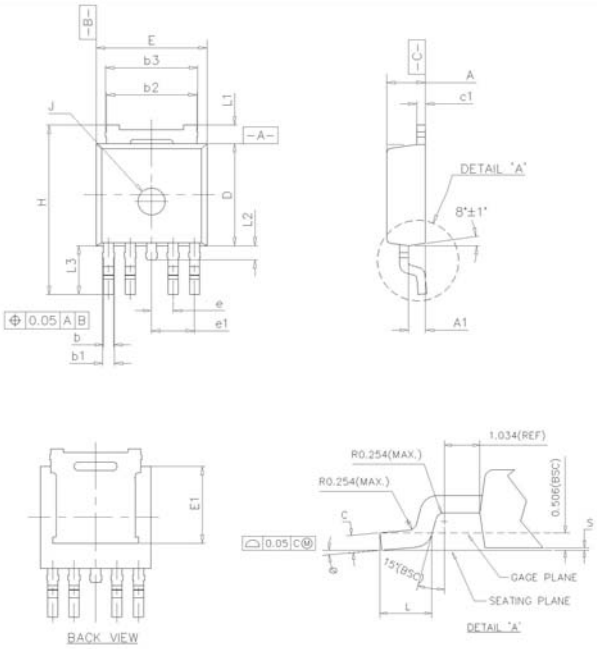
State Diagram



xUVLO=0 VIN<V_{UVLO}
OT=1 Over Temerature
DrainHigh=0 VDS<(Vin/4)
GateHigh=0 VGS<3V
t_{SC}=1 Shorted circuit timer is done
t_{OC}=1 Over current timer is done

State
N-Channel

Package Information



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